



# S905Y2

## Quick Reference Manual

---

Version 0.7

**Confidential for Radxa**

Amlogic, Ltd.

**COPYRIGHT**

© 2017 Amlogic, Ltd.

All rights reserved. No part of this document may be reproduced, transmitted, transcribed, or translated into any language in any form or by any means with the written permission of Amlogic, Ltd.

**TRADEMARKS**

AMLOGIC is a trademark of Amlogic, Ltd. All other trademarks and registered trademarks are property of their respective companies.

**DISCLAIMER**

Amlogic Ltd. may make improvements and/or changes in this document or in the product described in this document at any time.

This product is not intended for use in medical, life saving, or life sustaining applications.

Circuit diagrams and other information relating to products of Amlogic Ltd. are included as a means or illustrating typical applications. Consequently, complete information sufficient for production design is not necessarily given. Amlogic makes no representations or warranties with respect to the accuracy or completeness of the content presented in this document.

**REVISION HISTORY**

Revision Number	Revision Date	Changes
0.1	2017/11/2	Draft version release
0.2	2017/11/10	Update 3.1, 3.2, 3.3 and 3.4, update 4.4.1, 4.4.2 and 4.9, update 5.
0.3	2017/12/1	Update 4.9
0.4	2018/1/18	Update VDDQ current to 100mA, update VDDOV8_AO to VDDAO_OV8, update VDD_DDR, update PCIe pin description, add PCIe IO multifunction information, update PWM Interface Signal Description, optimize the figure quality in 4.6, update 4.3, update DVSS_AMPLL to DVSS, update 4.9, updated Feature Summary
0.5	2018/1/26	Update Table 10.
0.6	2018/3/6	Update 4.4.2, 4.4.1, 4.4.2, 4.8.
0.7	2018/4/3	Add PDM timing information

**Application Scope**

TBD

**CONTACT INFORMATION**

Amlogic, Ltd.  
2518 Mission College Blvd, Suite 120  
Santa Clara, CA 95054  
U.S.A.  
[www.amlogic.com](http://www.amlogic.com)

## Contents

1.	General Description .....	4
2.	Features Summary .....	5
3.	Pin Out Specification .....	9
3.1	Pin-Out Diagram (top view) .....	9
3.1	Pin Order .....	10
3.2	Pin Description .....	13
3.3	Pin Multiplexing Tables .....	19
3.4	Signal Descriptions .....	22
4.	Operating Conditions .....	27
4.1	Absolute Maximum Ratings .....	27
4.2	Recommended Operating Conditions .....	27
4.3	Thermal Operating Specifications .....	28
4.4	DC Electrical Characteristics .....	28
4.4.1	Normal GPIO Specifications (For DIO) .....	28
4.4.2	Open Drain GPIO Specifications (For DIO_OD) .....	28
4.4.3	DDR3/DDR3L/DDR4/LPDDR3/LPDDR4 SDRAM Specifications .....	28
4.5	Recommended Oscillator Electrical Characteristics .....	29
4.6	Timing Information .....	31
4.6.1	I2C Timing Specification .....	31
4.6.2	EMMC/SD Timing Specification .....	32
4.6.3	NAND Timing Specification .....	35
4.6.4	SPICC Timing Specification .....	37
4.6.5	SPIFC Timing Specification .....	37
4.6.6	Ethernet Timing Specification .....	39
4.6.7	Audio Timing Specification .....	41
4.6.8	PDM Timing Specification .....	42
4.7	Power On Config .....	44
4.8	Recommended Power on Sequence .....	45
4.9	Power Consumption .....	46
4.10	Storage and Baking Conditions .....	46
5.	Mechanical Dimensions .....	47

# 1. General Description

S905Y2 is an advanced application processor designed for Dongle/OTT/IP Set Top Box(STB) applications. It integrates a powerful CPU/GPU subsystem, a secured 4K video CODEC engine and a best-in-class HDR image processing pipeline with all major peripherals to form the ultimate low power multimedia AP.

The main system CPU is a quad-core ARM Cortex-A53 CPU with unified L2 cache to improve system performance. In addition, the Cortex-A53 CPU includes the NEON SIMD co-processor to improve software media processing capability.

The graphic subsystem consists of two graphic engines and a flexible video/graphic output pipeline. The ARM G31 MP2 GPU handles all OpenGL ES 3.2 Vulkan 1.0 and OpenCL 2.0 graphic programs, while the 2.5D graphics processor handles additional scaling, alpha, rotation and color space conversion operations. Together, the CPU and GPU handle all operating system, networking, user-interface and gaming related tasks. The video output pipeline includes Dolby Vision <sup>Optional</sup>, Dynamic HDR10, HDR10, HLG and PRIME HDR processing, REC709/BT2020 processing, motion adaptive edge enhancing, deblocking, flexible programmable scalar, and many picture enhancement filters before passing the enhanced image to the video output ports.

Amlogic Video Engine (AVE-10) offloads the Cortex-A53 CPUs from all video CODEC processing. It includes dedicated hardware video decoder and encoder. AVE-10 is capable of decoding 4Kx2K resolution video at 75fps with complete Trusted Video Path (TVP) for secure applications and supports full formats including MVC, MPEG-1/2/4, H.264, H.265, AVS, AVS+, AVS2, RealVideo, MJPEG streams, H.264, H265-10, VP9 and also JPEG pictures with no size limitation. The independent encoder is able to encode in JPEG or H.265/H.264 up to 1080p at 60fps.

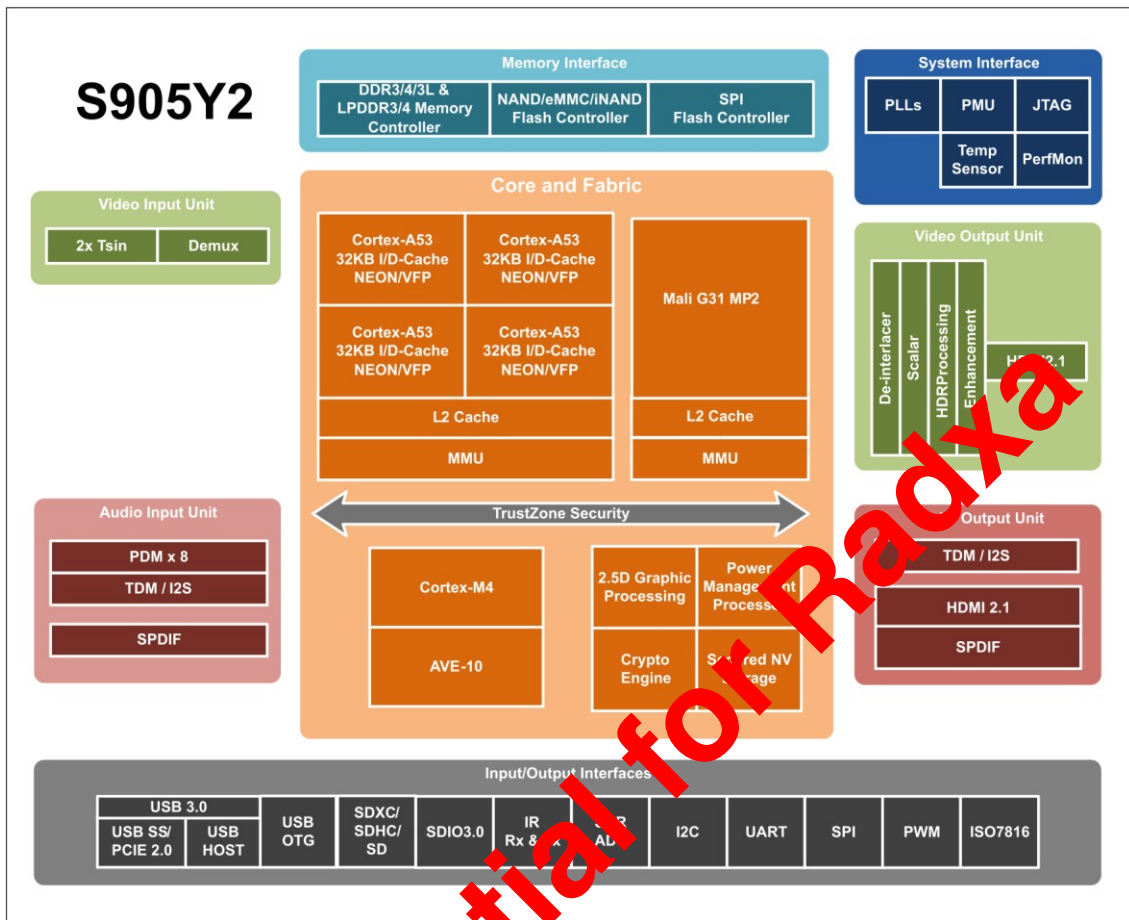
S905Y2 integrates all standard audio/video input/output interfaces including a HDMI2.1 transmitter with 3D, Dynamic HDR, CEC and HDCP 2.2 support, multiple TDM, PCM, I2S and SPDIF digital audio input/output interfaces, and 8 channel far-field PDM digital microphone (DMIC) inputs.

S905Y2 also integrates a set of functional blocks for digital TV broadcasting streams. The built-in two demux can process the TV streams from the serial transport stream input interface, which can connect to external tuner/demodulator.

The processor has rich advanced network and peripheral interfaces, including, dual USB 2.0 high-speed ports (one OTG and one HOST), one USB3.0 and PCIE 2.0 combo interface and multiple SDIO/SD card controllers, UART, I2C, high-speed SPI and PWMs.

Standard development environment utilizing Google's Android tool chain is supported. Please contact your AMLOGIC sales representative for more information.

## 2. Features Summary



### CPU Sub-system

- Quad core ARM Cortex-A53 CPU
- ARMv8-A architecture with Neon and Crypto extensions
- 8-stage in-order full dual-issue pipeline
- Unified system L2 cache
- Build-in Cortex-M4 core for always on processing
- Build-in Cortex-M5 core for system control processing
- Advanced TrustZone security system
- Application based traffic optimization using internal QoS-based switching fabrics

### 3D Graphics Processing Unit

- ARM G31 MP2 GPU
- 4-wide warps, dual texture pipe, 2x 4-wide execution engines (EE)
- Concurrent multi-core processing
- OpenGL ES 3.2, Vulkan 1.0 and OpenCL 2.0 support
- 

### 2.5D Graphics Processor

- Fast bitblt engine with dual inputs and single output
- Programmable raster operations (ROP)
- Programmable polyphase scaling filter

- Supports multiple video formats 4:2:0, 4:2:2 and 4:4:4 and multiple pixel formats (8/16/24/32 bits graphics layer)
- Fast color space conversion
- Advanced anti-flickering filter

### Crypto Engine

- AES/ block cipher with 128/256 bits keys, standard 16 bytes block size and streaming ECB, CBC and CTR modes
- TDES block cipher with ECB and CBC modes supporting 64 bits key for DES and 192 bits key for 3DES
- Hardware crypto key-ladder operation and DVB-CSA for transport stream encryption
- Built-in hardware True Random Number Generator (TRNG), CRC and SHA-1/SHA-2/HMAC SHA engine

### Video/Picture CODEC

- Amlogic Video Engine (AVE) with dedicated hardware decoders and encoders
- Support multi-video decoder up to 4Kx2K@60fps+1x1080P@60fps
- Supports multiple “secured” video decoding sessions and simultaneous decoding and encoding
- Video/Picture Decoding
  - VP9 Profile-2 up to 4Kx2K@60fps
  - H.265 HEVC MP-10@L5.1 up to 4Kx2K@60fps
  - AVS2-P2 Profile up to 4Kx2K@60fps
  - H.264 AVC HP@L5.1 up to 4Kx2K@30fps
  - H.264 MVC up to 1080P@60fps
  - MPEG-4 ASP@L5 up to 1080P@60fps (ISO-14496)
  - WMV/VC-1 SP/MP/AP up to 1080P@60fps
  - AVS-P16(AVS+) /AVS-P2 JiZhun Profile up to 1080P@60fps
  - MPEG-2 MP/HL up to 1080P@60fps (ISO-13818)
  - MPEG-1 MP/HL up to 1080P@60fps (ISO-11172)
  - RealVideo 8/9/10 up to 1080P@60fps
  - Multiple language and multiple formats subtitle video support
  - MJPEG and JPEG unlimited pixel resolution decoding (ISO/IEC-10918)
  - Supports JPEG thumbnail, scaling, rotation and transition effects
  - Supports \*.mkv, \*.wmv, \*.mpeg, \*.mp4, \*.dat, \*.avi, \*.mov, \*.iso, \*.mp4, \*.rm and \*.jpg file formats
- Video/Picture Encoding
  - Independent JPEG and H.265/H.264 encoder with configurable performance/bit-rate
  - JPEG image encoding
  - H.265/H.264 video encoding up to 1080P@60fps with low latency

### 8<sup>th</sup> Generation Advanced Amlogic TruLife Image Engine

- Supports Dolby Vision<sup>Optional</sup>, Dynamic HDR10, HDR10, HLG and Technicolor HDR processing
- Motion compensated noise reduction and 3D digital noise reduction for random noise
- Block noise, mosquito noise, spatial noise, contour noise reduction
- Motion compensated and motion adaptive de-interlacer
- Edge interpolation with low angle protection and processing
- 3:2/2:2 pulldown and Video on Film (VOF) detection and processing
- Smart sharpness with SuperScaler technology including de-contouring, de-ring, LTI, CTI, de-jaggy, peaking
- Dynamic non-Linear contrast enhancement
- All dimension multiple regions smart color management including blue/green extension, flesh-tone correction, wider gamut for video
- 2 video planes and 3 graphics planes
- Independent HDR re-mapping of video and graphic layer

### Video Output

- Built-in HDMI 2.1 transmitter including both controller and PHY with CEC, Dynamic HDR and HDCP 2.2, 4Kx2K@75 max resolution output

### Audio Decoder and Input/Output

- Supports MP3, AAC, WMA, RM, FLAC, Ogg, Dolby Digital <sup>Optional</sup>, Dolby Digital Plus <sup>Optional</sup>, DTS <sup>Optional</sup> and programmable with 7.1/5.1 down-mixing
- Built-in serial digital audio SPDIF/IEC958 input and output
- 2 built-in TDM/PCM/I2S ports with TDM/PCM mode up to 384kHz x32bits x 8ch or 96kHz x 32bits x 32ch and I2S mode up to 384kHz x 32bits x 8ch
- Digital microphone PDM input with programmable CIC, LPF & HPF, support up to 8 DMICs

### Memory and Storage Interface

- 32-bit DRAM memory interface with dual ranks and max 4GB total address space
- Compatible with JEDEC standard DDR3-2133 /DDR3L-2133 /DDR4-2666 /LPDDR3-2133, LPDDR4-3200 SDRAM
- Supports SLC/MLC/TLC NAND Flash with 60-bit ECC, compatible to Toshiba toggle mode in addition to ONFI 2.2
- SDSC/SDHC/SDXC card and SDIO interface with 1-bit and 4-bit data bus width supporting spec version 2.x/3.x/4.x DS/HS modes up to UHS-I SDR104
- eMMC and MMC card interface with 1/4/8-bit data bus width fully supporting spec version 5.0 HS400
- Supports serial 1, 2 or 4-bit NOR Flash via SPI interface
- Built-in 4k bits One-Time-Programming memory for key storage

### Network Interface

- WiFi/IEEE802.11 & Bluetooth supporting via PCIE/SDIO/USB/UART/PCM
- Network interface optimized for mixed WIFI and BT traffic

### Digital Television Interface

- Two serial Transport stream (TS) input interfaces with built-in demux processor for connecting to external digital TV tuner/demodulator
- Built-in PWM, I2C and SPI interfaces to control tuner and demodulator
- Integrated ISO 7816 smart card controller

### Integrated I/O Controllers and Interfaces

- Dual USB 2.0 high-speed USB I/O, one USB Host and one USB OTG
- One USB SS and PCIe 3.0 combo interface up to 5Gbps, supporting 2 configurations:
  - 1 USB2.0 OTG + 1 USB 2.0 Host + 1 PCIe
  - 1 USB2.0 OTG + 1 USB3.0 (No PCIe)
- Multiple PWM, UART, I2C and SPI interface with slave select
- Programmable IR remote input/output controllers
- Built-in 10bit SAR ADC with 2 input channels
- A set of General Purpose IOs with built-in pull up and pull down

### System, Peripherals and Misc. Interfaces

- Integrated general purpose timers, counters, DMA controllers
- 24 MHz crystal input
- Embedded debug interface using ICE/JTAG

### Power Management

- Multiple internal power domains controlled by software
- Multiple sleep modes for CPU, system, DRAM, etc.
- Multiple internal PLLs for DVFS operation
- Multi-voltage I/O design for 1.8V and 3.3V
- Power management auxiliary processor in a dedicated always-on (AO) power domain for system standby

**Security**

- Trustzone based Trusted Execution Environment (TEE)
- Secured boot, encrypted OTP, encrypted DRAM with memory integrity checker, hardware key ladder and internal control buses and storage
- Separated secure/non-secure Entropy true RNG
- Pre-region/ID memory security control and electric fence
- Hardware based Trusted Video Path (TVP) , video watermarking and secured contents (needs SecureOS software)
- Secured IO and secured clock

**Package**

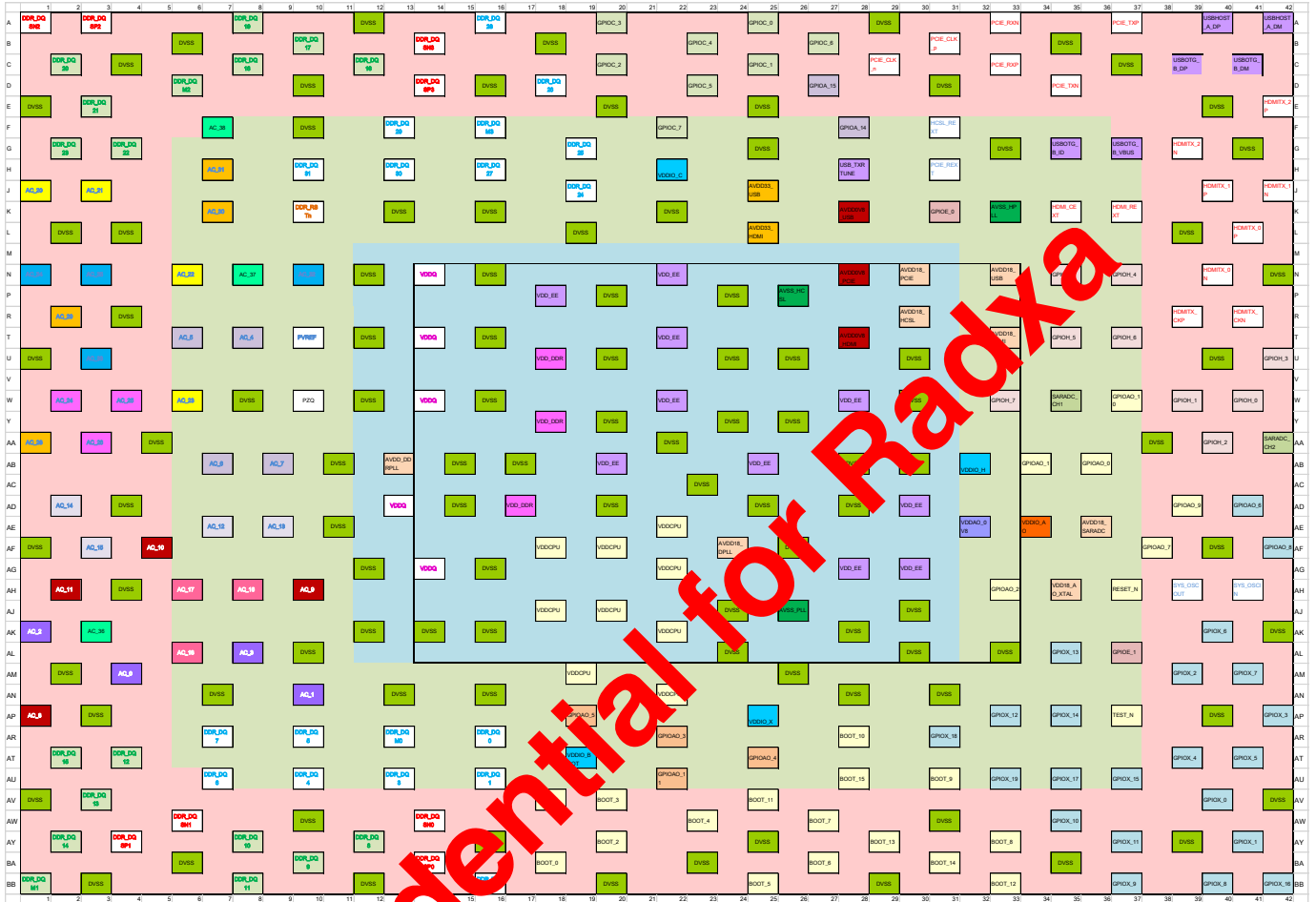
- FCBGA, 10.9mm\*10.9mm, 0.5mm pitch, RoHS compliant

**Confidential for Radxa**



# 3. Pin Out Specification

## 3.1 Pin-Out Diagram (top view)



### 3.1 Pin Order

Table 1. Pin Order

BALL #	NET NAME	BALL #	NET NAME	BALL #	NET NAME
A1	DDR_DQSN2	E25	DVSS	L4	DVSS
A3	DDR_DQSP2	E40	DVSS	L19	DVSS
A8	DDR_DQ19	E42	HDMITX_2P	L25	AVDD33_HDMI
A12	DVSS	F7	AC_38	L39	DVSS
A16	DDR_DQ28	F10	DVSS	L41	HDMITX_OP
A20	GPIOC_3	F13	DDR_DQ29	N1	AC_34
A25	GPIOC_0	F16	DDR_DQM3	N3	AC_35
A29	DVSS	F22	GPIOC_7	N6	AC_32
A33	PCIE_RXN	F28	GPIOA_14	N8	AC_37
A37	PCIE_TXP	F31	HCSL_REXT	N10	AC_32
A40	USBHOST_A_DP	G2	DDR_DQ23	N12	DVSS
A42	USBHOST_A_DM	G4	DDR_DQ22	N14	VDDQ
B6	DVSS	G19	DDR_DQ25	N16	DVSS
B10	DDR_DQ17	G25	DVSS	N22	VDD_EE
B14	DDR_DQSN3	G33	DVSS	N28	AVDD0V8_PCIE
B18	DVSS	G35	USBOTG_B_ID	N30	AVDD18_PCIE
B23	GPIOC_4	G37	USBOTG_B_VBU	N33	AVDD18_USB
B27	GPIOC_6	G39	HDMITX_2N	N35	GPIOH_8
B31	PCIE_CLK_p	G41	DVSS	N37	GPIOH_4
B35	DVSS	H7	AC_31	N40	HDMITX_ON
C2	DDR_DQ20	H10	DDR_DQ1	N42	DVSS
C4	DVSS	H13	DDR_DQ30	P18	VDD_EE
C8	DDR_DQ18	H16	DDR_DQ27	P20	DVSS
C12	DDR_DQ16	H22	VDDIO_C	P24	DVSS
C20	GPIOC_2	H25	USB_TXRTUNE	P26	AVSS_HCSL
C25	GPIOC_1	J31	PCIE_REXT	R2	AC_29
C29	PCIE_CLK_n	J1	AC_20	R4	DVSS
C33	PCIE_RXP	J3	AC_21	R30	AVDD18_HCSL
C37	DVSS	J19	DDR_DQ24	R39	HDMITX_CKP
C39	USBOTG_B_DP	J25	AVDD33_USB	R41	HDMITX_CKN
C41	USBOTG_B_DM	J40	HDMITX_1P	T6	AC_5
D6	DDR_DQM2	J42	HDMITX_1N	T8	AC_4
D10	DVSS	K7	AC_30	T10	PVREF
D14	DDR_DQSP3	K10	DDR_RSTn	T12	DVSS
D16	DVSS	K13	DVSS	T14	VDDQ
D18	DDR_DQ26	K16	DVSS	T16	DVSS
D23	GPIOC_5	K22	DVSS	T22	VDD_EE
D27	GPIOA_15	K28	AVDD0V8_USB	T28	AVDD0V8_HDMI
D31	DVSS	K31	GPIOE_0	T33	AVDD18_HDMI
D35	PCIE_TXN	K33	AVSS_HPLL	T35	GPIOH_5
E1	DVSS	K35	HDMI_CEXT	T37	GPIOH_6
E3	DDR_DQ21	K37	HDMI_REXT	U1	DVSS
E20	DVSS	L2	DVSS	U3	AC_33

BALL #	NET NAME	BALL #	NET NAME	BALL #	NET NAME
U18	VDD_DDR	AB36	GPIOAO_0	AJ18	VDDCPU
U20	DVSS	AC23	DVSS	AJ20	VDDCPU
U24	DVSS	AD2	AC_14	AJ24	DVSS
U26	DVSS	AD4	DVSS	AJ26	AVSS_PLL
U30	DVSS	AD13	VDDQ	AJ30	DVSS
U40	DVSS	AD15	DVSS	AK1	AC_2
U42	GPIOH_3	AD17	VDD_DDR	AK3	AC_36
W2	AC_24	AD20	DVSS	AK12	DVSS
W4	AC_25	AD25	DVSS	AK14	DVSS
W6	AC_23	AD28	DVSS	AK16	DVSS
W8	DVSS	AD30	VDD_EE	AK22	VDDCPU
W10	PZQ	AD39	GPIOAO_9	AK28	DVSS
W12	DVSS	AD41	GPIOAO_6	AK40	GPIOX_6
W14	VDDQ	AE7	AC_12	AK42	DVSS
W16	DVSS	AE9	AC_13	AL6	AC_18
W22	VDD_EE	AE11	DVSS	AL8	AC_3
W28	VDD_EE	AE22	VDDCPU	AL12	DVSS
W30	DVSS	AE32	VDDAO_OV8	AL24	DVSS
W33	GPIOH_7	AE34	VDDIO_AO	AL30	DVSS
W35	SARADC_CH1	AE36	AVDD18_SARAD	AL33	DVSS
W37	GPIOAO_10	AF1	DVSS	AL35	GPIOX_13
W39	GPIOH_1	AF3	AC_15	AL37	GPIOE_1
W41	GPIOH_0	AF5	AC_16	AM2	DVSS
Y18	VDD_DDR	AF18	VDDCPU	AM4	AC_0
Y20	DVSS	AF20	VDDCPU	AM19	VDDCPU
Y24	DVSS	AF24	AVDD18_DPLL	AM26	DVSS
Y26	DVSS	AF26	DVSS	AM39	GPIOX_2
AA1	AC_28	AF28	GPIOAO_7	AM41	GPIOX_7
AA3	AC_26	AF40	DVSS	AN7	DVSS
AA5	DVSS	AF42	GPIOAO_8	AN10	AC_1
AA22	DVSS	AG12	DVSS	AN13	DVSS
AA38	DVSS	AG14	VDDQ	AN16	DVSS
AA40	GPIOH_5	AG16	DVSS	AN22	VDDCPU
AA42	SARADC_CH2	AG22	VDDCPU	AN28	DVSS
AB7	AC_6	AG28	VDD_EE	AN31	DVSS
AB9	AC_7	AG30	VDD_EE	AP1	AC_8
AB11	DVSS	AH2	AC_11	AP3	DVSS
AB13	AVDD_DDRPLL	AH4	DVSS	AP19	GPIOAO_5
AB15	DVSS	AH6	AC_17	AP25	VDDIO_X
AB17	DVSS	AH8	AC_16	AP33	GPIOX_12
AB20	VDD_EE	AH10	AC_9	AP35	GPIOX_14
AB25	VDD_EE	AH33	GPIOAO_2	AP37	TEST_N
AB28	DVSS	AH35	VDD18_AO_XTAL	AP40	DVSS
AB30	DVSS	AH37	RESET_N	AP42	GPIOX_3
AB32	VDDIO_H	AH39	SYS_OSCOUT	AR7	DDR_DQ7
AB34	GPIOAO_1	AH41	SYS_OSCIN	AR10	DDR_DQ5

BALL #	NET NAME	BALL #	NET NAME	BALL #	NET NAME
AR13	DDR_DQM0	AV18	BOOT_1	AY39	DVSS
AR16	DDR_DQ0	AY37	GPIOX_11	AY41	GPIOX_1
AR22	GPIOAO_3	AV20	BOOT_3	BA6	DVSS
AR28	BOOT_10	AV25	BOOT_11	BA10	DDR_DQ9
AR31	GPIOX_18	AV40	GPIOX_0	BA14	DDR_DQSP0
AT2	DDR_DQ15	AV42	DVSS	BA18	BOOT_0
AT4	DDR_DQ12	AW6	DDR_DQSN1	BA23	DVSS
AT19	VDDIO_BOOT	AW10	DVSS	BA27	BOOT_6
AT25	GPIOAO_4	AW14	DDR_DQSN0	BA31	BOOT_14
AT39	GPIOX_4	AW23	BOOT_4	BA35	DVSS
AT41	GPIOX_5	AW27	BOOT_7	BB1	DDR_DQM1
AU7	DDR_DQ6	AW31	DVSS	BB3	DVSS
AU10	DDR_DQ4	AW35	GPIOX_10	BB8	DDR_DQ11
AU13	DDR_DQ3	AY2	DDR_DQ14	BB12	DVSS
AU16	DDR_DQ1	AY4	DDR_DQSP1	BB16	DDR_DQ2
AU22	GPIOAO_11	AY8	DDR_DQ10	BB20	DVSS
AU28	BOOT_15	AY12	DDR_DQ8	BB24	BOOT_5
AU31	BOOT_9	AY16	DVSS	BB29	DVSS
AU33	GPIOX_19	AY20	BOOT_2	BB33	BOOT_12
AU35	GPIOX_17	AY25	DVSS	BB37	GPIOX_9
AU37	GPIOX_15	AY29	BOOT_13	BB40	GPIOX_8
AV1	DVSS	AY33	BOOT_	BB42	GPIOX_16
AV3	DDR_DQ13				

Confidential for Paduka

## 3.2 Pin Description

The S905Y2 application processor pin assignment is described in the following table.

**Table 2. Pin Name assignments**

Net Name	Type	Default Pull UP/DN	Description	Power Domain	If Unused
<b>GPIOX-</b> Refer to Table 3 for functional multiplex information.					
GPIOX_0	DIO	UP	General purpose input/output bank X signal 0	VDDIO_X	-
GPIOX_1	DIO	UP	General purpose input/output bank X signal 1	VDDIO_X	-
GPIOX_2	DIO	UP	General purpose input/output bank X signal 2	VDDIO_X	-
GPIOX_3	DIO	UP	General purpose input/output bank X signal 3	VDDIO_X	-
GPIOX_4	DIO	UP	General purpose input/output bank X signal 4	VDDIO_X	-
GPIOX_5	DIO	UP	General purpose input/output bank X signal 5	VDDIO_X	-
GPIOX_6	DIO	DOWN	General purpose input/output bank X signal 6	VDDIO_X	-
GPIOX_7	DIO	UP	General purpose input/output bank X signal 7	VDDIO_X	-
GPIOX_8	DIO	UP	General purpose input/output bank X signal 8	VDDIO_X	-
GPIOX_9	DIO	UP	General purpose input/output bank X signal 9	VDDIO_X	-
GPIOX_10	DIO	UP	General purpose input/output bank X signal 10	VDDIO_X	-
GPIOX_11	DIO	UP	General purpose input/output bank X signal 11	VDDIO_X	-
GPIOX_12	DIO	UP	General purpose input/output bank X signal 12	VDDIO_X	-
GPIOX_13	DIO	UP	General purpose input/output bank X signal 13	VDDIO_X	-
GPIOX_14	DIO	UP	General purpose input/output bank X signal 14	VDDIO_X	-
GPIOX_15	DIO	UP	General purpose input/output bank X signal 15	VDDIO_X	-
GPIOX_16	DIO	UP	General purpose input/output bank X signal 16	VDDIO_X	-
GPIOX_17	DIO	DOWN	General purpose input/output bank X signal 17	VDDIO_X	-
GPIOX_18	DIO	UP	General purpose input/output bank X signal 18	VDDIO_X	-
GPIOX_19	DIO	Z	General purpose input/output bank X signal 19	VDDIO_X	-
VDDIO_X			Power supply for GPIO bank X	VDDIO_X	-
<b>GPIOA-</b> Refer to Table 4 for functional multiplex information.					
GPIOA_14	DIO	UP	General purpose input/output bank A signal 14	VDDIO_AO	-
GPIOA_15	DIO	UP	General purpose input/output bank A signal 15	VDDIO_AO	-
VDDIO_AO	P	-	Power supply for GPIO bank A and AO	-	-
<b>GPIOC-</b> Refer to Table 5 for functional multiplex information.					
GPIOC_0	DIO	UP	General purpose input/output bank C signal 0	VDDIO_C	-
GPIOC_1	DIO	UP	General purpose input/output bank C signal 1	VDDIO_C	-
GPIOC_2	DIO	UP	General purpose input/output bank C signal 2	VDDIO_C	-
GPIOC_3	DIO	UP	General purpose input/output bank C signal 3	VDDIO_C	-
GPIOC_4	DIO	UP	General purpose input/output bank C signal 4	VDDIO_C	-
GPIOC_5	DIO	UP	General purpose input/output bank C signal 5	VDDIO_C	-
GPIOC_6	DIO	UP	General purpose input/output bank C signal 6	VDDIO_C	-
GPIOC_7	OD3.3V	Z	General purpose input/output bank C signal 7	VDDIO_C	-
VDDIO_C	P	-	Power supply for GPIO bank C	-	-
<b>BOOT</b> - Refer to Table 6 for functional multiplex information.					
BOOT_0	DIO	UP	General purpose input/output bank BOOT signal 0	VDDIO_BOOT	-
BOOT_1	DIO	UP	General purpose input/output bank BOOT signal 1	VDDIO_BOOT	-
BOOT_2	DIO	UP	General purpose input/output bank BOOT signal 2	VDDIO_BOOT	-
BOOT_3	DIO	UP	General purpose input/output bank BOOT signal 3	VDDIO_BOOT	-

Net Name	Type	Default Pull UP/DN	Description	Power Domain	If Unused
BOOT_4	DIO	UP	General purpose input/output bank BOOT signal 4	VDDIO_BOOT	-
BOOT_5	DIO	UP	General purpose input/output bank BOOT signal 5	VDDIO_BOOT	-
BOOT_6	DIO	UP	General purpose input/output bank BOOT signal 6	VDDIO_BOOT	-
BOOT_7	DIO	UP	General purpose input/output bank BOOT signal 7	VDDIO_BOOT	-
BOOT_8	DIO	UP	General purpose input/output bank BOOT signal 8	VDDIO_BOOT	-
BOOT_9	DIO	UP	General purpose input/output bank BOOT signal 9	VDDIO_BOOT	-
BOOT_10	DIO	UP	General purpose input/output bank BOOT signal 10	VDDIO_BOOT	-
BOOT_11	DIO	UP	General purpose input/output bank BOOT signal 11	VDDIO_BOOT	-
BOOT_12	DIO	DOWN	General purpose input/output bank BOOT signal 12	VDDIO_BOOT	-
BOOT_13	DIO	DOWN	General purpose input/output bank BOOT signal 13	VDDIO_BOOT	-
BOOT_14	DIO	UP	General purpose input/output bank BOOT signal 14	VDDIO_BOOT	-
BOOT_15	DIO	UP	General purpose input/output bank BOOT signal 15	VDDIO_BOOT	-
VDDIO_BOOT	P	-	Power supply for GPIO bank BOOT	-	-
<b>GPIOH</b> - Refer to Table 7 for functional multiplex information.					
GPIOH_0	OD5V	Z	General purpose input/output bank H signal 0	VDDIO_H	-
GPIOH_1	OD5V	Z	General purpose input/output bank H signal 1	VDDIO_H	-
GPIOH_2	OD5V	Z	General purpose input/output bank H signal 2	VDDIO_H	-
GPIOH_3	OD5V	Z	General purpose input/output bank H signal 3	VDDIO_H	-
GPIOH_4	DIO	DOWN	General purpose input/output bank H signal 4	VDDIO_H	-
GPIOH_5	DIO	DOWN	General purpose input/output bank H signal 5	VDDIO_H	-
GPIOH_6	DIO	DOWN	General purpose input/output bank H signal 6	VDDIO_H	-
GPIOH_7	DIO	DOWN	General purpose input/output bank H signal 7	VDDIO_H	-
GPIOH_8	OD5V	Z	General purpose input/output bank H signal 8	VDDIO_H	-
VDDIO_H	P	-	Power supply for GPIO bank H	-	-
<b>GPIOAO</b> - Refer to Table 8 for functional multiplex information.					
GPIOAO_0	DIO	UP	General purpose input/output bank AO signal 0	VDDIO_AO	-
GPIOAO_1	DIO	UP	General purpose input/output bank AO signal 1	VDDIO_AO	-
GPIOAO_2	DIO	DOWN	General purpose input/output bank AO signal 2	VDDIO_AO	-
GPIOAO_3	DIO	UP	General purpose input/output bank AO signal 3	VDDIO_AO	-
GPIOAO_4	DIO	DOWN	General purpose input/output bank AO signal 4	VDDIO_AO	-
GPIOAO_5	DIO	UP	General purpose input/output bank AO signal 5	VDDIO_AO	-
GPIOAO_6	DIO	DOWN	General purpose input/output bank AO signal 6	VDDIO_AO	-
GPIOAO_7	DIO	UP	General purpose input/output bank AO signal 7	VDDIO_AO	-
GPIOAO_8	DIO	UP	General purpose input/output bank AO signal 8	VDDIO_AO	-
GPIOAO_9	DIO	DOWN	General purpose input/output bank AO signal 9	VDDIO_AO	-
GPIOAO_10	DIO	UP	General purpose input/output bank AO signal 10	VDDIO_AO	-
GPIOAO_11	DIO	DOWN	General purpose input/output bank AO signal 11	VDDIO_AO	-
TEST_N	DIO	UP	SOC test pin and general purpose input/output bank AO signal 12. Should be pulled up during normal power-on.	VDDIO_AO	-
RESET_N	DI	DOWN	System reset input	VDDIO_AO	-
VDDIO_AO	P	-	Power supply for GPIO bank A and AO	VDDIO_AO	-
<b>GPIOE</b> - Refer to Table 9 for functional multiplex information.					
GPIOE_0		Z	General purpose input/output bank E signal 0	VDD18_AO_XTAL	-
GPIOE_1		Z	General purpose input/output bank E signal 1	VDD18_AO_XTAL	-

Net Name	Type	Default Pull UP/DN	Description	Power Domain	If Unused
VDD18_AO_XTAL	P	-	Power supply for Always On domain	-	-
<b>SARADC</b>					
SARADC_CH1	AI	-	ADC channel 1 input	AVDD18_SARADC	NC
SARADC_CH2	AI	-	ADC channel 2 input	AVDD18_SARADC	NC
AVDD18_SARADC	P	-	Analog power supply for SARADC	-	To 1.8V
<b>HDMI TX</b>					
HDMITX_0P	AO	-	HDMI TMDS data0 positive output	HDMITX_AVDD33	NC
HDMITX_0N	AO	-	HDMI TMDS data0 negative output	HDMITX_AVDD33	NC
HDMITX_1P	AO	-	HDMI TMDS data1 positive output	HDMITX_AVDD33	NC
HDMITX_1N	AO	-	HDMI TMDS data1 negative output	HDMITX_AVDD33	NC
HDMITX_2P	AO	-	HDMI TMDS data1 positive output	HDMITX_AVDD33	NC
HDMITX_2N	AO	-	HDMI TMDS data1 negative output	HDMITX_AVDD33	NC
HDMITX_CKP	AO	-	HDMI TMDS clock positive output	HDMITX_AVDD33	NC
HDMITX_CKN	AO	-	HDMI TMDS clock negative output	HDMITX_AVDD33	NC
HDMI_REXT	A	-	HDMI output strength setting resistor	HDMI_AVDD18	NC
HDMI_CEXT	A	-	HDMI TX external filter cap	HDMI_AVDD18	NC
AVDD33_HDMI	P	-	Analog power supply 3.3V for HDMI	-	To 3.3V
AVDD18_HDMI	P	-	Analog power supply 1.8V for HDMI	-	To 1.8V
AVDD0V8_HDMI	P	-	Power supply 0.8V for HDMI	-	To VDD_EE
<b>DRAM</b>					
AC_0	DO	-	DDR PHY address/command/control signal bit 0	VDDQ	-
AC_1	DO	-	DDR PHY address/command/control signal bit 1	VDDQ	-
AC_2	DO	-	DDR PHY address/command/control signal bit 2	VDDQ	-
AC_3	DO	-	DDR PHY address/command/control signal bit 3	VDDQ	-
AC_4	DO	-	DDR PHY address/command/control signal bit 4	VDDQ	-
AC_5	DO	-	DDR PHY address/command/control signal bit 5	VDDQ	-
AC_6	DO	-	DDR PHY address/command/control signal bit 6	VDDQ	-
AC_7	DO	-	DDR PHY address/command/control signal bit 7	VDDQ	-
AC_8	DO	-	DDR PHY address/command/control signal bit 8	VDDQ	-
AC_9	DO	-	DDR PHY address/command/control signal bit 9	VDDQ	-
AC_10	DO	-	DDR PHY address/command/control signal bit 10	VDDQ	-
AC_11	DO	-	DDR PHY address/command/control signal bit 11	VDDQ	-
AC_12	DO	-	DDR PHY address/command/control signal bit 12	VDDQ	-
AC_13	DO	-	DDR PHY address/command/control signal bit 13	VDDQ	-
AC_14	DO	-	DDR PHY address/command/control signal bit 14	VDDQ	-
AC_15	DO	-	DDR PHY address/command/control signal bit 15	VDDQ	-
AC_16	DO	-	DDR PHY address/command/control signal bit 16	VDDQ	-
AC_17	DO	-	DDR PHY address/command/control signal bit 17	VDDQ	-
AC_18	DO	-	DDR PHY address/command/control signal bit 18	VDDQ	-
AC_20	DO	-	DDR PHY address/command/control signal bit 20	VDDQ	-
AC_21	DO	-	DDR PHY address/command/control signal bit 21	VDDQ	-
AC_22	DO	-	DDR PHY address/command/control signal bit 22	VDDQ	-
AC_23	DO	-	DDR PHY address/command/control signal bit 23	VDDQ	-
AC_24	DO	-	DDR PHY address/command/control signal bit 24	VDDQ	-
AC_25	DO	-	DDR PHY address/command/control signal bit 25	VDDQ	-

Net Name	Type	Default Pull UP/DN	Description	Power Domain	If Unused
AC_26	DO	-	DDR PHY address/command/control signal bit 26	VDDQ	-
AC_28	DO	-	DDR PHY address/command/control signal bit 28	VDDQ	-
AC_29	DO	-	DDR PHY address/command/control signal bit 29	VDDQ	-
AC_30	DO	-	DDR PHY address/command/control signal bit 30	VDDQ	-
AC_31	DO	-	DDR PHY address/command/control signal bit 31	VDDQ	-
AC_32	DO	-	DDR PHY address/command/control signal bit 32	VDDQ	-
AC_33	DO	-	DDR PHY address/command/control signal bit 33	VDDQ	-
AC_34	DO	-	DDR PHY address/command/control signal bit 34	VDDQ	-
AC_35	DO	-	DDR PHY address/command/control signal bit 35	VDDQ	-
AC_36	DO	-	DDR PHY address/command/control signal bit 36	VDDQ	-
AC_37	DO	-	DDR PHY address/command/control signal bit 37	VDDQ	-
AC_38	DO	-	DDR PHY address/command/control signal bit 38	VDDQ	-
DDR_RSTn	DO	-	DDR3/DDR4/LPDDR4 RSTn	VDDQ	-
DDR_DQ0	DIO	-	DRAM data bus bit 0	VDDQ	-
DDR_DQ1	DIO	-	DRAM data bus bit 1	VDDQ	-
DDR_DQ2	DIO	-	DRAM data bus bit 2	VDDQ	-
DDR_DQ3	DIO	-	DRAM data bus bit 3	VDDQ	-
DDR_DQ4	DIO	-	DRAM data bus bit 4	VDDQ	-
DDR_DQ5	DIO	-	DRAM data bus bit 5	VDDQ	-
DDR_DQ6	DIO	-	DRAM data bus bit 6	VDDQ	-
DDR_DQ7	DIO	-	DRAM data bus bit 7	VDDQ	-
DDR_DQ8	DIO	-	DRAM data bus bit 8	VDDQ	-
DDR_DQ9	DIO	-	DRAM data bus bit 9	VDDQ	-
DDR_DQ10	DIO	-	DRAM data bus bit 10	VDDQ	-
DDR_DQ11	DIO	-	DRAM data bus bit 11	VDDQ	-
DDR_DQ12	DIO	-	DRAM data bus bit 12	VDDQ	-
DDR_DQ13	DIO	-	DRAM data bus bit 13	VDDQ	-
DDR_DQ14	DIO	-	DRAM data bus bit 14	VDDQ	-
DDR_DQ15	DIO	-	DRAM data bus bit 15	VDDQ	-
DDR_DQ16	DIO	-	DRAM data bus bit 16	VDDQ	-
DDR_DQ17	DIO	-	DRAM data bus bit 17	VDDQ	-
DDR_DQ18	DIO	-	DRAM data bus bit 18	VDDQ	-
DDR_DQ19	DIO	-	DRAM data bus bit 19	VDDQ	-
DDR_DQ20	DIO	-	DRAM data bus bit 20	VDDQ	-
DDR_DQ21	DIO	-	DRAM data bus bit 21	VDDQ	-
DDR_DQ22	DIO	-	DRAM data bus bit 22	VDDQ	-
DDR_DQ23	DIO	-	DRAM data bus bit 23	VDDQ	-
DDR_DQ24	DIO	-	DRAM data bus bit 24	VDDQ	-
DDR_DQ25	DIO	-	DRAM data bus bit 25	VDDQ	-
DDR_DQ26	DIO	-	DRAM data bus bit 26	VDDQ	-
DDR_DQ27	DIO	-	DRAM data bus bit 27	VDDQ	-
DDR_DQ28	DIO	-	DRAM data bus bit 28	VDDQ	-
DDR_DQ29	DIO	-	DRAM data bus bit 29	VDDQ	-
DDR_DQ30	DIO	-	DRAM data bus bit 30	VDDQ	-
DDR_DQ31	DIO	-	DRAM data bus bit 31	VDDQ	-



Net Name	Type	Default Pull UP/DN	Description	Power Domain	If Unused
DDR_DQM0	DO	-	DRAM data mask 0	VDDQ	-
DDR_DQM1	DO	-	DRAM data mask 1	VDDQ	-
DDR_DQM2	DO	-	DRAM data mask 2	VDDQ	-
DDR_DQM3	DO	-	DRAM data mask 3	VDDQ	-
DDR_DQSP0	DIO	-	DRAM data strobe 0	VDDQ	-
DDR_DQSN0	DIO	-	DRAM data strobe 0 complementary	VDDQ	-
DDR_DQSP1	DIO	-	DRAM data strobe 1	VDDQ	-
DDR_DQSN1	DIO	-	DRAM data strobe 1 complementary	VDDQ	-
DDR_DQSP2	DIO	-	DRAM data strobe 2	VDDQ	-
DDR_DQSN2	DIO	-	DRAM data strobe 2 complementary	VDDQ	-
DDR_DQSP3	DIO	-	DRAM data strobe 3	VDDQ	-
DDR_DQSN3	DIO	-	DRAM data strobe 3 complementary	VDDQ	-
PZQ	A	-	DRAM reference pin for ZQ calibration	VDDQ	-
PVREF	A	-	DRAM reference voltage	VDDQ	-
AVDD18_DPLL	P	-	Analog 1.8V power supply for system PLL	-	-
AVDD_DDRPLL	P	-	Analog power supply for DDRPLL	-	-
<b>USB</b>					
USBHOST_A_DP	AIO	-	USB 2.0 Port A positive data signal (Host only)	AVDD33_USB	NC
USBHOST_A_DM	AIO	-	USB 2.0 Port A negative data signal (Host only)	AVDD33_USB	NC
USBOTG_B_DP	AIO	-	USB 2.0 Port B positive data signal (OTG)	AVDD33_USB	NC
USBOTG_B_DM	AIO	-	USB 2.0 Port B negative data signal (OTG)	AVDD33_USB	NC
USBOTG_B_ID	AIO	-	USB OTG mini-receiver identifier (Internal 12.8K $\Omega$ pull-up resistor to AVDD18)	AVDD18_USB	NC
USBOTG_B_VBUS	AIO	-	USB OTG cable power detection	AVDD18_USB	NC
USB_TXRTUNE	AIO	-	USB 2.0 Port B host output strength setting resistor	AVDD18_USB	NC
AVDD33_USB	P	-	3.3V Power supply for USB	-	To 3.3V
AVDD18_USB	P	-	1.8V Power supply for USB	-	To 1.8V
AVDD0V8_USB	P	-	Analog 0.8V power supply for USB	-	To VDD_EE
<b>PCIE</b>					
PCIE_CLK_n	AO	-	PCIE reference clock negative signal	AVDD18_PCIE	NC
PCIE_CLK_p	AO	-	PCIE reference clock positive signal	AVDD18_PCIE	NC
PCIE_REXT	AIO	-	PCIE output strength setting resistor	AVDD18_PCIE	NC
PCIE_RXN	AIO	-	PCIE or USB3.0 input negative signal	AVDD18_PCIE	NC
PCIE_RXP	AIO	-	PCIE or USB3.0 input positive signal	AVDD18_PCIE	NC
PCIE_TXN	AO	-	PCIE or USB3.0 output negative signal	AVDD18_PCIE	NC
PCIE_TXP	AO	-	PCIE or USB3.0 output positive signal	AVDD18_PCIE	NC
AVDD0V8_PCIE	AP	-	Analog 0.8V power supply for PCIE	-	To VDD_EE
AVDD18_PCIE	AP	-	Analog 1.8V power supply for PCIE	-	To 1.8V
HCSL_REXT	AIO	-	PCIE reference clock output strength setting resistor	-	<b>NC</b>
AVDD18_HCSL	AP	-	Analog 1.8V power supply for PCIE reference module clock	-	To 1.8V
AVSS_HCSL	AP	-	Analog ground for PCIE reference module clock	-	-
<b>System Clock &amp; PLL</b>					
SYS_OSCIN	AI	-	24MHz crystal oscillator input	VDD18_AO_XTAL	-
SYS_OSCOUT	AO	-	24MHz crystal oscillator output	VDD18_AO_XTAL	-
<b>Analog Power</b>					

Net Name	Type	Default Pull UP/DN	Description	Power Domain	If Unused
AVSS_HPLL	AP	-	Ground of HDMI PLL	-	-
AVSS_PLL	AP	-	Ground of System PLL	-	-
<b>Digital Power</b>					
VDDCPU	P	-	Power supply for CPU (Cortex A53)	-	-
VDD_DDR	P	-	Core Power supply for DDR PHY	-	-
VDDQ	P	-	DDR IO Power supply for DDR PHY	-	-
VDD_EE	P	-	Power supply for GPU and core logic	-	-
VDD18_AO_XTAL	P	-	1.8V Power supply for AO	-	-
VDDAO_0V8	P	-	0.8V power supply for AO for XTAL and M3/M4 CPU	-	-
<b>Digital Ground</b>					
DVSS	P	-	Digital power ground	-	-

## Abbreviations:

- DI = Digital input pin
- DO = Digital output pin
- DIO = Digital input/output pin
- OD3.3V = 3.3V input tolerant open drain (OD) output pin, need external pull up
- OD5V = 5V input tolerant open drain (OD) output pin, need external pull up
- A = Analog setting or filtering pin
- AI = Analog input pin
- AO = Analog output pin
- AIO = Analog input/output pin
- P = Power pin
- AP = Analog power pin
- NC = No connection
- UP = Pull-Up
- DOWN = Pull-down
- Z = Tri-State

Confidential for Radxa

### 3.3 Pin Multiplexing Tables

Multiple usage pins are used to conserve pin consumption for different features. The S905Y2 devices can be used in many different applications but each application will not utilize all the on chip features. As a result, some of the features share the same pin. Most of the multiple usage pins can be used as a GPIO pin as well.

**Table 3. GPIOX\_x Multi-Function Pin**

Pin Name	Func1	Func2	Func3	Func4	Func5	Func6	Func7
GPIOX_0	SDIO_D0	PDM_DIN0	TSIN_A_DIN0				
GPIOX_1	SDIO_D1	PDM_DIN1	TSIN_A_SOP				
GPIOX_2	SDIO_D2	PDM_DIN2	TSIN_A_VALID				
GPIOX_3	SDIO_D3	PDM_DIN3	TSIN_A_CLK	PWM_D			
GPIOX_4	SDIO_CLK	PDM_DCLK					
GPIOX_5	SDIO_CMD	MCLK_1		PWM_C			
GPIOX_6	PWM_A	UART_EE_B_TX		PWM_D			
GPIOX_7	PWM_F	UART_EE_B_RX		PWM_B			
GPIOX_8	TDMA_D1	TDMA_DIN1	TSIN_B_SOP	SPI_A_MOSI	PWM_C	ISO7816_CLK	
GPIOX_9	TDMA_D0	TDMA_DIN0	TSIN_B_VALID	SPI_A_MISO		ISO7816_DATA	
GPIOX_10	TDMA_FS	TDMA_SLV_FS	TSIN_B_DIN0	SPI_A_SS0	I2C_EE_M1_SDA		
GPIOX_11	TDMA_SCLK	TDMA_SLV_SCLK	TSIN_B_CLK	SPI_A_SCLK	I2C_EE_M1_SCL		
GPIOX_12	UART_EE_A_TX						
GPIOX_13	UART_EE_A_RX						
GPIOX_14	UART_EE_A_CTS						
GPIOX_15	UART_EE_A_RTS						
GPIOX_16	PWM_E						
GPIOX_17	I2C_EE_M2_SDA						
GPIOX_18	I2C_EE_M2_SCL						
GPIOX_19	PWM_B	WORLD_SYNC					GEN_CLK_EE

**Table 4. GPIOA\_x Multi-Function Pin**

Pin Name	Func1	Func2
GPIOA_14	WORLD_SYNC	I2C_EE_M3_SDA
GPIOA_15	IR_REMOTE_IN	I2C_EE_M3_SCL

**Table 5. GPIOC\_x Multi-Function Pin**

Pin Name	Func1	Func2	Func3	Func4	Func5
GPIOC_0	SDCARD_D0	JTAG_B_TDO		PDM_DIN0	SPI_A_MOSI
GPIOC_1	SDCARD_D1	JTAG_B_TDI		PDM_DIN1	SPI_A_MISO
GPIOC_2	SDCARD_D2	UART_AO_A_RX		PDM_DIN2	SPI_A_SS0
GPIOC_3	SDCARD_D3	UART_AO_A_TX		PDM_DIN3	SPI_A_SCLK
GPIOC_4	SDCARD_CLK	JTAG_B_CLK		PDM_DCLK	PWM_C
GPIOC_5	SDCARD_CMD	JTAG_B_TMS	I2C_EE_M0_SDA		ISO7816_CLK
GPIOC_6			I2C_EE_M0_SCL		ISO7816_DATA
GPIOC_7	PCIECK_REQN	WORLD_SYNC			

**Table 6. BOOT\_x Multi-Function Pin**

Pin Name	Func1	Func2	Func3
BOOT_0	EMMC_D0		
BOOT_1	EMMC_D1		
BOOT_2	EMMC_D2		
BOOT_3	EMMC_D3		NOR_HOLD
BOOT_4	EMMC_D4		NOR_D
BOOT_5	EMMC_D5		NOR_Q
BOOT_6	EMMC_D6		NOR_C

Pin Name	Func1	Func2	Func3
BOOT_7	EMMC_D7		NOR_WP
BOOT_8	EMMC_CLK	NAND_WEN_CLK	
BOOT_9		NAND_ALE	
BOOT_10	EMMC_CMD	NAND_CLE	
BOOT_11		NAND_CE0	
BOOT_12		NAND_REN_WR	
BOOT_13	EMMC_NAND_DQS		
BOOT_14		NAND_RB0	NOR_CS
BOOT_15		NAND_CE1	

Table 7. GPIOH\_x Multi-Function Pin

Pin Name	Func1	Func2	Func3	Func4	Func5	Func6
GPIOH_0	HDMITX_SDA	I2C_EE_M3_SDA	—			
GPIOH_1	HDMITX_SCL	I2C_EE_M3_SCL	—			
GPIOH_2	HDMITX_HPD_IN	I2C_EE_M1_SDA	—			
GPIOH_3	—	I2C_EE_M1_SCL	—	AO_CEC_A	AO_CEC_B	
GPIOH_4	SPDIF_OUT	UART_EE_C_RTS	SPI_B_MOSI			
GPIOH_5	SPDIF_IN	UART_EE_C_CTS	SPI_B_MISO	PWM_F	TDMB_D3	TDMB_DIN3
GPIOH_6	ISO7816_CLK	UART_EE_C_RX	SPI_B_SS0	I2C_EE_M1_SDA		
GPIOH_7	ISO7816_DATA	UART_EE_C_TX	SPI_B_SCLK	I2C_EE_M1_SCL		
GPIOH_8						

Table 8. GPIOAO\_x Multi-Function Pin

Pin Name	Func1	Func2	Func3	Func4	Func5	Func6	Func7
GPIOAO_0	UART_AO_A_TX						
GPIOAO_1	UART_AO_A_RX						
GPIOAO_2	I2C_AO_M0_SCL	UART_AO_B_TX	I2C_AO_S0_SDA				
GPIOAO_3	I2C_AO_M0_SDA	UART_AO_B_RX	I2C_AO_S0_SCL				
GPIOAO_4	IR_REMOTE_OUT	CLK_32K_IN	PWMAO_C	PWMAO_C_HIZ	TDMB_D0	TDMB_DIN0	
GPIOAO_5	IR_REMOTE_IN		PWMAO_D				
GPIOAO_6	JTAG_A_CLK	—	PWMAO_C	TSIN_A_SOP	TDMB_D2	TDMB_DIN2	
GPIOAO_7	JTAG_A_TMS	—		TSIN_A_DIN0	TDMB_FS	TDMB_SLV_FS	
GPIOAO_8	JTAG_A_TDI		UART_AO_B_TX	TSIN_A_CLK	TDMB_SCLK	TDMB_SLV_SCLK	
GPIOAO_9	JTAG_A_TDO		UART_AO_B_RX	TSIN_A_VALID	MCLK_0		
GPIOAO_10	AO_CEC_A	AO_CEC_B	PWMAO_D	SPDIF_OUT	TDMB_D1	TDMB_DIN1	CLK12_24
GPIOAO_11	—	PWMAO_A_HIZ	PWMAO_A	GEN_CLK_EE	GEN_CLK_AO		

Table 9 GPIOE\_x Multi-Function Pin

Pin Name	Func1	Func2	Func3	Func4
GPIOE_0	UART_AO_A_CTS	UART_AO_B_CTS	PWMAO_B	I2C_AO_M0_SCL
GPIOE_1	UART_AO_A_RTS	UART_AO_B_RTS	PWMAO_D	I2C_AO_M0_SDA

Table 10 DDR AC Multi-Function Pin

Pin Name	LPDDR3	LPDDR4	DDR3	DDR4
AC_0	CKEA0	CKEA0	CKE0	CKE0
AC_1	CKEA1	CKEA1	CKE1	CKE1
AC_2	CSA0	CSA0	CS_N0	CS_N0
AC_3	CSA1	CSA1	NC	NC
AC_4	CLKA_T	CLKA_T	CAS_N	A6
AC_5	CLKA_C	CLKA_C	BA2	A8

Pin Name	LPDDR3	LPDDR4	DDR3	DDR4
AC_6	NC	NC	A7	A2
AC_7	NC	NC	A5	A11
AC_8	CAA2	CAA2	A10	A10
AC_9	CAA7	CAA3	WE_N	BG1
AC_10	CAA1	CAA1	A0	A3
AC_11	CAA4	CAA0	A2	A12
AC_12	CAA5	CAA5	A9	A0
AC_13	CAA6	CAA4	A13	A4
AC_14	CAA0	NC	A14	A13
AC_15	CAA3	NC	A11	A9
AC_16	CAA9	NC	CLK0_T	CLK0_T
AC_17	CAA8	NC	CLK0_C	CLK0_C
AC_18	ODTA	NC	NC	NC
AC_20	NC	CKE0	CLK1_T	CLK1_T
AC_21	NC	CKE1	CLK1_C	CLK1_C
AC_22	NC	CSB1	NC	NC
AC_23	NC	CSB0	NC	NC
AC_24	NC	CLKB_T	A6	A5
AC_25	NC	CLKB_C	A6	BA1
AC_26	NC	NC	A1	A1
AC_28	NC	CAB1	A8	A7
AC_29	NC	CAB3	BA1	RAS_N/A16
AC_30	NC	CAB5	A15	ACT_N
AC_31	NC	CAA1	RAS_N	WE_N/A14
AC_32	NC	CAB4	NC	NC
AC_33	NC	CAB0	A12	CAS_N/A15
AC_34	NC	NC	A3	BA0
AC_35	NC	NC	BA0	BG0
AC_36	NC	NC	ODT0	ODT0
AC_37	NC	NC	ODT1	ODT1
AC_38	NC	NC	CS_N1	CS_N1
RESET_N	NC	RESET_N	RESET_N	RESET_N
PVREF	PVREF	PVREF	PVREF	PVREF
PZQ	PZQ	PZQ	PZQ	PZQ

Table 11. PCIE\_IO Multi-Function Pin

Pin Name	Func1	Func2
PCIE_RXP	PCIE_RXP	USB3.0_RXP
PCIE_RXN	PCIE_RXN	USB3.0_RXN
PCIE_TXN	PCIE_TXN	USB3.0_TXN

## 3.4 Signal Descriptions

**Table 12. SD Card Interface Signal Description**

Signal Name	Type	Description
SDCARD_D0	DIO	SD Card data bus bit 0 signal
SDCARD_D1	DIO	SD Card data bus bit 1 signal
SDCARD_D2	DIO	SD Card data bus bit 2 signal
SDCARD_D3	DIO	SD Card data bus bit 3 signal
SDCARD_CLK	DO	SD Card clock signal
SDCARD_CMD	DIO	SD Card command signal

**Table 13. SDIO Interface Signal Description**

Signal Name	Type	Description
SDIO_D0	DIO	SDIO data bus bit 0 signal
SDIO_D1	DIO	SDIO data bus bit 1 signal
SDIO_D2	DIO	SDIO data bus bit 2 signal
SDIO_D3	DIO	SDIO data bus bit 3 signal
SDIO_CLK	DO	SDIO clock signal
SDIO_CMD	DIO	SDIO command signal

**Table 14. Clock Interface Signal Description**

Signal Name	Type	Description
CLK_32K_IN	DI	32KHz clock input
CLK12_24	DO	12MHz/24MHz clock output

**Table 15. UART Interface Signal Description**

Signal Name	Type	Description
UART_AO_A_TX	DO	UART Port A data output in AO domain
UART_AO_A_RX	DI	UART Port A data input in AO domain
UART_AO_A_CTS	DI	UART Port A Clear To Send Signal in AO domain
UART_AO_A_RTS	DO	UART Port A Ready To Send Signal in AO domain
UART_AO_B_TX	DO	UART Port B data output in AO domain
UART_AO_B_RX	DI	UART Port B data input in AO domain
UART_AO_B_CTS	DI	UART Port B Clear To Send Signal in AO domain
UART_AO_B_RTS	DO	UART Port B Ready To Send Signal in AO domain
UART_EE_A_TX	DO	UART Port A data output in EE domain
UART_EE_A_RX	DI	UART Port A data input in EE domain
UART_EE_A_CTS	DI	UART Port A Clear To Send Signal in EE domain
UART_EE_A_RTS	DO	UART Port A Ready To Send Signal in EE domain
UART_EE_B_TX	DO	UART Port B data output in EE domain
UART_EE_B_RX	DI	UART Port B data input in EE domain
UART_EE_C_TX	DO	UART Port C data output in EE domain
UART_EE_C_RX	DI	UART Port C data input in EE domain
UART_EE_C_CTS	DI	UART Port C Clear To Send Signal in EE domain
UART_EE_C_RTS	DO	UART Port C Ready To Send Signal in EE domain

**Table 16. ISO7816 Interface Signal Description**

Signal Name	Type	Description
ISO7816_DATA	DIO	ISO7816 data signal

Signal Name	Type	Description
ISO7816_CLK	DO	ISO7816 clock signal

Table 17. TS In Interface Signal Description

Signal Name	Type	Description
TSIN_A_DINO	DI	Serial TS input port A data
TSIN_A_CLK	DI	TS input port A clock
TSIN_A_SOP	DI	TS input port A start of stream signal
TSIN_A_VALID	DI	TS input port A date valid signal
TSIN_B_DINO	DI	Serial TS input port B data
TSIN_B_CLK	DI	TS input port B clock
TSIN_B_SOP	DI	TS input port B start of stream signal
TSIN_B_VALID	DI	TS input port B date valid signal

Table 18. PWM Interface Signal Description

Signal Name	Type	Description
PWM_A	DO	PWM channel A output signal
PWM_B	DO	PWM channel B output signal
PWM_C	DO	PWM channel C output signal
PWM_D	DO	PWM channel D output signal
PWM_E	DO	PWM channel E output signal
PWM_F	DO	PWM channel F output signal
PWMAO_A / PWMAO_A_HIZ	DO	PWM A output signal in Always On domain, or extended HiZ function of PWMAO_A
PWMAO_B	DO	PWM B output signal in Always On domain
PWMAO_C / PWMAO_C_HIZ	DO	PWM C output signal in Always On domain, or extended HiZ function of PWMAO_C
PWMAO_D	DO	PWM D output signal in Always On domain

Table 19. I2C Interface Signal Description

Signal Name	Type	Description
I2C_AO_M0_SCL	DO	I2C bus port 0 clock output, Master mode, in AO domain
I2C_AO_M0_SDA	DIO	I2C bus port 0 data input/output, Master mode, in AO domain
I2C_AO_S0_SCL	DI	I2C bus port 0 clock input, Slave mode, in AO domain
I2C_AO_S0_SDA	DIO	I2C bus port 0 data input/output, Slave mode, in AO domain
I2C_EE_M0_SCL	DO	I2C bus port 0 clock output, Master mode, in EE domain
I2C_EE_M0_SDA	DIO	I2C bus port 0 data input/output, Master mode, in EE domain
I2C_EE_M1_SCL	DO	I2C bus port 1 clock output, Master mode, in EE domain
I2C_EE_M1_SDA	DIO	I2C bus port 1 data input/output, Master mode, in EE domain
I2C_EE_M2_SCL	DO	I2C bus port 2 clock output, Master mode, in EE domain
I2C_EE_M2_SDA	DIO	I2C bus port 2 data input/output, Master mode, in EE domain
I2C_EE_M3_SCL	DO	I2C bus port 3 clock output, Master mode, in EE domain
I2C_EE_M3_SDA	DIO	I2C bus port 3 data input/output, Master mode, in EE domain

Table 20. eMMC Interface Signal Description

Signal Name	Type	Description
EMMC_D0	DIO	eMMC/NAND data bus bit 0 signal
EMMC_D1	DIO	eMMC/NAND data bus bit 1 signal
EMMC_D2	DIO	eMMC/NAND data bus bit 2 signal
EMMC_D3	DIO	eMMC/NAND data bus bit 3 signal
EMMC_D4	DIO	eMMC/NAND data bus bit 4 signal

Signal Name	Type	Description
EMMC_D5	DIO	eMMC/NAND data bus bit 5 signal
EMMC_D6	DIO	eMMC/NAND data bus bit 6 signal
EMMC_D7	DIO	eMMC/NAND data bus bit 7 signal
EMMC_CLK	DO	eMMC clock signal
EMMC_CMD	DIO	eMMC command signal
EMMC_NAND_DQS	DIO	eMMC/NAND data strobe

Table 21. NAND Signal Description

Signal Name	Type	Description
NAND_RB0	DI	NAND ready/busy
NAND_ALE	DO	NAND address latch enable
NAND_CEO	DO	NAND chip enable 0
NAND_CE1	DO	NAND chip enable 1
NAND_CLE	DO	NAND command latch enable
NAND_REN_WR	DO	NAND read enable or write/read
NAND_WEN_CLK	DO	NAND write enable or clock

Table 22. NOR Interface Signal Description

Signal Name	Type	Description
NOR_CS	DO	SPI NOR chip select
NOR_C	DO	SPI NOR Serial Clock
NOR_D	DIO	SPI NOR 1bit mode Output, 2/4 bit mode data I/O 0
NOR_Q	DIO	SPI NOR 1bit mode Input, 2/4 bit mode data I/O 1
NOR_WP	DIO	SPI NOR Write protection output, 4 bit mode data I/O 2
NOR_HOLD	DIO	SPI bus hold output, 4 bit mode data I/O 3

Table 23. HDMI Interface Signal Description

Signal Name	Type	Description
HDMITX_SDA	DIO	HDMI TX DDC_I2C interface data signal
HDMITX_SCL	DO	HDMI TX DDC_I2C interface clock signal
HDMITX_HPD_IN	DI	HDMI TX hot plug in signal input
AO_CEC_A	DIO	Customer Electronics Control signal in AO domain
AO_CEC_B	DIO	2nd module of Customer Electronics Control signal in AO domain

Table 24. SPDIF Interface Signal Description

Signal Name	Type	Description
SPDIF_IN	DI	SPDIF input signal
SPDIF_OUT	DO	SPDIF output signal

Table 25. PCIE Interface Signal Description

Signal Name	Type	Description
PCIECK_REQN	DI	PCIE clock request input

Table 26. SPI Interface Signal Description

Signal Name	Type	Description
SPI_A_MOSI	DIO	SPI master output, slave input A
SPI_A_MISO	DIO	SPI master input, slave output A
SPI_A_SCLK	DIO	SPI clock A



Signal Name	Type	Description
SPI_A_SS0	DIO	SPI slave select 0 A
SPI_B_MOSI	DIO	SPI master output, slave input B
SPI_B_MISO	DIO	SPI master input, slave output B
SPI_B_SCLK	DIO	SPI clock B
SPI_B_SS0	DIO	SPI slave select 0 B

Table 27. Remote Interface Signal Description

Signal Name	Type	Description
IR_REMOTE_IN	DI	IR remote control input
IR_REMOTE_OUT	DO	IR remote control output

Table 28. Time Division Multiplexing Signal Description

Signal Name	Type	Description
MCLK_0	DO	Master clock output 0, for I2S master mode
MCLK_1	DO	Master clock output 1, for I2S master mode
TDMA_DIN0	DI	Data input 0 of TDM port A
TDMA_DIN1	DI	Data input 1 of TDM port A
TDMA_D0	DIO	Data input/output 0 of TDM port A
TDMA_D1	DIO	Data input/output 1 of TDM port A
TDMA_SCLK	DO	Bit clock output of TDM port A
TDMA_FS	DO	Frame sync output of TDM port A (Word clock of I2S)
TDMA_SLV_SCLK	DI	Bit clock input of TDM port A
TDMA_SLV_FS	DI	Frame sync input of TDM port A (Word clock of I2S)
TDMB_DIN0	DI	Data input 0 of TDM port B
TDMB_DIN1	DI	Data input 1 of TDM port B
TDMB_DIN2	DI	Data input 2 of TDM port B
TDMB_DIN3	DI	Data input 3 of TDM port B
TDMB_D0	DIO	Data input/output 0 of TDM port B
TDMB_D1	DIO	Data input/output 1 of TDM port B
TDMB_D2	DIO	Data input/output 2 of TDM port B
TDMB_D3	DIO	Data input/output 3 of TDM port B
TDMB_SCLK	DO	Bit clock output of TDM port B
TDMB_FS	DO	Frame sync output of TDM port B (Word clock of I2S)
TDMB_SLV_SCLK	DI	Bit clock input of TDM port B
TDMB_SLV_FS	DI	Frame sync input of TDM port B (Word clock of I2S)

Table 29. PDM Signal Description

Signal Name	Type	Description
PDM_DIN0	DI	Pulse-Density Modulation input data 0 signal
PDM_DIN1	DI	Pulse-Density Modulation input data 1 signal
PDM_DIN2	DI	Pulse-Density Modulation input data 2 signal
PDM_DIN3	DI	Pulse-Density Modulation input data 3 signal
PDM_DCLK	DO	Pulse-Density Modulation output clock signal

Table 30. JTAG Interface Signal Description

Signal Name	Type	Description
JTAG_A_TDO	DO	JTAG data output channel A
JTAG_A_TDI	DI	JTAG data input channel A
JTAG_A_TMS	DI	JTAG Test mode select input channel A
JTAG_A_CLK	DI	JTAG Test clock input channel A
JTAG_B_TDO	DO	JTAG data output channel B
JTAG_B_TDI	DI	JTAG data input channel B
JTAG_B_TMS	DI	JTAG Test mode select input channel B

Signal Name	Type	Description
JTAG_B_CLK	DI	JTAG Test clock input channel B

**Table 31. Other Signal Description**

Signal Name	Type	Description
WORLD_SYNC	DI	World clock sync input, to sync clock of multi devices
GEN_CLK_EE	DO	General clock output for EE domain clock, for debug
GEN_CLK_AO	DO	General clock output for AO domain clock, for debug

**Confidential for Radxa**

## 4. Operating Conditions

### 4.1 Absolute Maximum Ratings

The table below gives the absolute maximum ratings. Exposure to stresses beyond those listed in this table may result in permanent device damage, unreliability or both.

Characteristic	Value	Unit
VDDCPU Supply Voltage	1.1	V
VDD_EE Supply Voltage	1.0	V
VDDQ Supply Voltage	1.7	V
1.8V Supply Voltage	1.98	V
3.3V Supply Voltage	3.63	V
Input voltage, $V_I$	-0.3 ~ $V_{DDIO} + 0.3$	V
Junction Temperature	125	°C

### 4.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDDCPU	Voltage for Cortex A53 CPU	0.68 <sup>1</sup>		1.03 <sup>2</sup>	V
VDD_EE and other 0.8V domain	Voltage for GPU & core logic	0.68 <sup>1</sup>	0.8	0.9 <sup>2</sup>	V
VDDQ	DDR3/DDR3L/DDR4/LPDDR3/LPDDR4 IC Supply Voltage	1.05		1.6	V
AVDD18	1.8V AVDD for HDMI, SARADC, USB phy, PCIE, PLL module	1.71	1.80	1.89	V
AVDD18_AO_XTAL	1.8V VDD for GPIOE, XTAL, and OV108	1.71	1.80	1.89	V
AVDD_DDRPLL	Analog power supply for DDR PLL	1.05		1.89	V
AVDD33	3.3V AVDD for USB and HDMI TX module	3.15	3.3	3.45	V
VDDIO	LV mode	1.71	1.80	1.89	V
	HV mode	2.9/3.2 <sup>3</sup>	3.3	3.45	V
T <sub>J</sub>	Operating Junction Temperature	0		105 <sup>4</sup>	°C
T <sub>A</sub>	Operating Ambient Temperature	0		70	°C

Note:

- Minimal VDDCPU/VDD\_EE voltage is for sleep mode while system runs at very low speed. Higher clock will need higher voltage. Considering the power supply may have 2% deviation, the minimal voltage in actual application should not be set to lower than 0.7V (min spec + 0.02V).
- Likewise, maximum VDDCPU/VDD\_EE voltage in actual application should not be higher than (max spec -0.02V). Voltage of VDDCPU will affect CPU speed. Use lower voltage when CPU runs on lower speed to save power. Recommend to use +/-1.5% or higher precision DCDC.
- GPIO cannot work if VDDIO voltage is out of the spec of LV / HV mode. GPIO output at HV mode will be weaker & max operating speed will be lower if VDDIO are design to 3.0V. Do not design VDDIO to lower than 3.0V in HV mode, recommend to use +/-1.5% or higher precision DCDC to supply power for VDDIO, actual voltage supplies to VDDIO (HV mode) should not be lower than 2.9V.
- For operating temperature, good heat sink may be needed to guarantee T<sub>J</sub> < max spec.

## 4.3 Thermal Operating Specifications

Jedec 2P2S board 101.5mm\*114.5mm, natural convection, ambient temperature 25 °C.

Symbol	Parameter	Value.	Unit
$\Theta_{ja}$	Package junction-to-ambiance thermal resistance in nature convection	18.90	°C/Watt
$\Theta_{jb}$	Package junction-to-pcb thermal resistance in nature convection	9.97	°C/Watt
$\Theta_{jc}$	Package junction-to-case thermal resistance in nature convection	5.58	°C/Watt

## 4.4 DC Electrical Characteristics

### 4.4.1 Normal GPIO Specifications (For DIO)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{IH}(VDDIO=3.3V)$	High-level input voltage	IOVREF+0.37		VDDIO+0.3	V
$V_{IL}(VDDIO=3.3V)$	Low-level input voltage	-0.3		IOVREF-0.23	V
$V_{IH}(VDDIO=1.8V)$	High-level input voltage	IOVREF/2+0.3		VDDIO+0.3	V
$V_{IL}(VDDIO=1.8V)$	Low-level input voltage	-0.3		IOVREF/2-0.3	V
$R_{PU/PD}$	Built-in pull up/down resistor		100K		ohm
IoL/IoH(DS=0)	GPIO driving capability	0.5		1	
IoL/IoH(DS=1)	GPIO driving capability	2.5		4	
IoL/IoH(DS=2)	GPIO driving capability	3		5	
IoL/IoH(DS=3)	GPIO driving capability	4		6 <sup>2)</sup>	mA
VOH	Output high level with IoL/IoH loading	VDDIO-0.5			V
VOL	Output low level with IoL/IoH loading			0.4	V

Note:

- 1) Minimal driving capability applies when VDDIO LV 1.7V or VDDIO HV 3.0V, VOL<0.4V.
- 2) Maximal driving capability only applies to application such as driving LED when VOL<0.6V.
- 3) VDD18\_AO\_XTAL supplies power to IOVREF
- 4) PDM voltage requirement's should belong to GPIO spec.

### 4.4.2 Open Drain GPIO Specifications (For DIO\_OD)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{IH}(OD5V)$	High-level input voltage	1.5		5.5	V
$V_{IL}(OD5V)$	Low-level input voltage	-0.3		0.8	V
$V_{IH}(OD3.3V)$	High-level input voltage	1.5		3.6	V
$V_{IL}(OD3.3V)$	Low-level input voltage	-0.3		0.8	V
$R_{PU/PD}$	Built-in pull up/down resistor on OD IO	-	-	-	ohm
Io	OD IO driving low capability	4		6	mA
VOL	Output low level with min Io loading			0.4	V

### 4.4.3 DDR3/DDR3L/DDR4/LPDDR3/LPDDR4 SDRAM Specifications

#### Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDDQ	IO supply voltage(DDR3)	1.46	1.50	1.57	V
VDDQ	IO supply voltage(DDR3L)	1.31	1.35	1.45	V
VDDQ	IO supply voltage(DDR4)	1.14	1.20	1.30	V
VDDQ	IO supply voltage(LPDDR3)	1.14	1.2	1.3	

VDDQ	IO supply voltage(LPDDR4)	1.06	1.1	1.17	
Vref	Input reference supply voltage	0.49*VDDQ	0.5*VDDQ	0.51*VDDQ	V

Note: The minimal VDDQ voltage in sleep mode is defined by memory.

#### DC specifications - DDR3/DDR3L mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIH	DC input voltage high	Vref + 0.100		VDDQ	V
VIL	DC input voltage low	VSSQ		Vref-0.100	V
VOH	DC output logic high	0.8*VDDQ			V
VOL	DC output logic low			0.2*VDDQ	V
RTT	Input termination resistance to VDDQ/2	100	120	140	ohm
		54	60	66	
		36	40	44	

#### DC specifications - DDR4 mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
VdIVW_total	Rx Mask voltage-p-p total			136	mv
VOH	DC output logic high	0.9*VDDQ			V
VOL	DC output logic low			0.1*VDDQ	V
RTT	Input termination resistance to VDDQ	200	240	280	ohm
		100	120	140	
		67	80	93	
		50	60	70	
		42	48	56	
		34	40	46	
		28	34	40	

#### DC Specifications - LPDDR3 mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIH	DC input voltage high	Vref + 0.100		VDDQ	V
VIL	DC input voltage low	VSSQ		Vref-0.100	V
VOH	DC output logic high	0.9*VDDQ			V
VOL	DC output logic low			0.1*VDDQ	V
RTT	Input termination resistance to VDDQ	100	120	140	ohm
		200	240	280	

#### DC Specifications - LPDDR4 mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIH	DC input voltage high	TBD		TBD	V
VIL	DC input voltage low	TBD		TBD	V
VOH	DC output logic high	TBD			V
VOL	DC output logic low			TBD	V
RTT	Input termination resistance to VDDQ	TBD	TBD	TBD	ohm

## 4.5 Recommended Oscillator Electrical Characteristics

S905Y2 requires the 24MHz oscillator for generating the main clock source.

**Table 32. 24MHz Oscillator Specification**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$F_o$	Nominal Frequency		24		MHz	
$\Delta f/f_o$	Frequency Tolerance	-30		+30	ppm	At 25 °C
		-50		+50	ppm	At -20~85 °C
$C_L$	Load Capacitance	8	12	12	pF	
ESR	Equivalent Series Resistance			100	oHm	

Note: 10ppm Tolerance is preferred if 24MHz XTAL is also driving WIFI module.

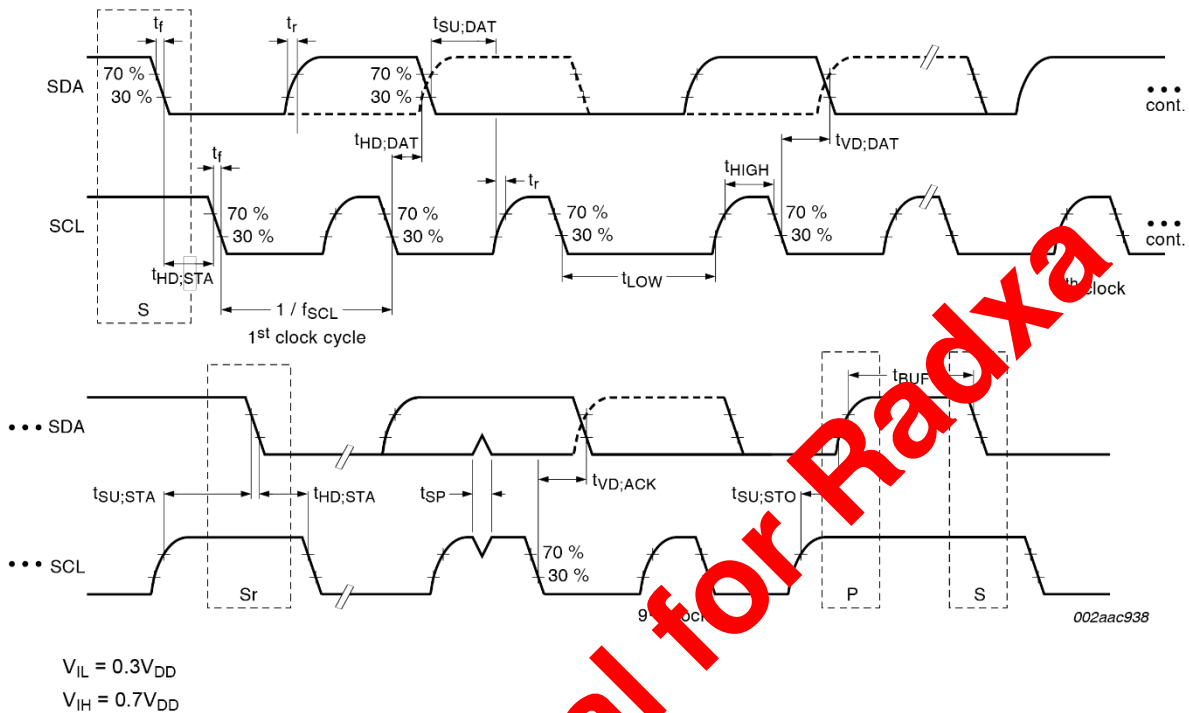
**Confidential for Radxa**

## 4.6 Timing Information

### 4.6.1 I2C Timing Specification

The I2C master interface Fast/Standard mode timing specifications are shown below.

**Figure 1 I2C Interface Timing Diagram, FS mode**



**Table 33. I2C Interface Timing Specification, SF mode**

Symbol	Parameter	Standard-mode		Fast-mode		Unit
		Min.	Max	Min	Max	
$t_R$	Rise time of SDA and SCL signals	—	1000	—	300	ns
$t_F$	Fall time of SDA and SCL signals	—	300	—	300	ns
$f_{SCL}$	SCL clock frequency	—	100	—	400	KHz
$t_{LOW}$	LOW period of the SCL clock	4.7	—	1.3	—	$\mu$ s
$t_{HIGH}$	HIGH period of the SCL clock	4.0	—	0.6	—	$\mu$ s
$t_{Su;STA}$	Setup time for START	4.7	—	0.6	—	$\mu$ s
$t_{Su;DAT}$	Setup time for SDA	250	—	100	—	ns
$t_{Su;STO}$	Setup time for STOP	4.0	—	0.6	—	$\mu$ s
$t_{Hd;STA}$	Hold time for START	4.0	—	0.6	—	$\mu$ s
$t_{Hd;DAT}$	Hold time for SDA	0	3.45	0	0.9	$\mu$ s
$t_{BuF}$	Bus free time between stop and start	4.7	—	1.3	—	$\mu$ s

### 4.6.2 EMMC/SD Timing Specification

Timing specification for EMMC and SD are shown as below.

Figure 2. EMMC HS400 Data Output Timing

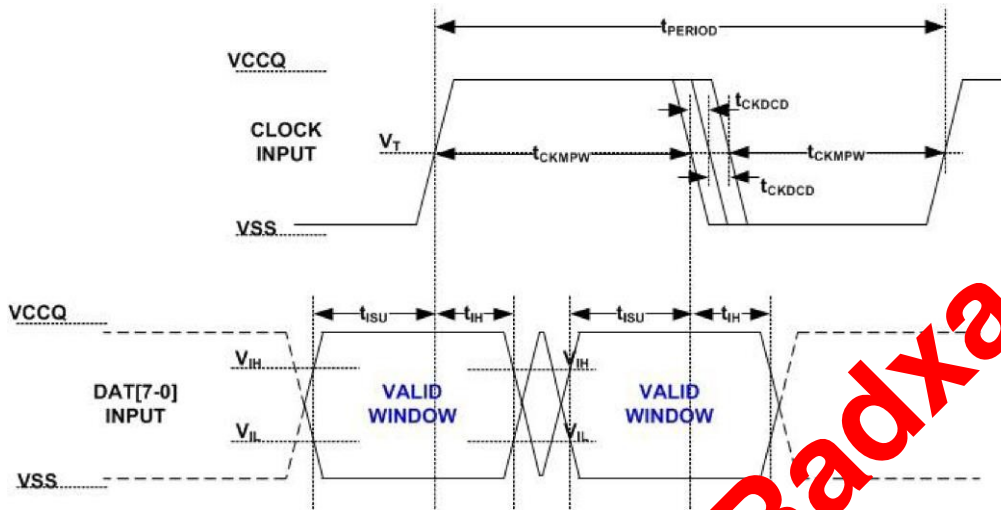


Table 34. HS400 Timing Specification

Symbol	Parameter	Min	Max	Unit
tPERIOD	Cycle time data transfer mode	5	-	ns
SR	Slew rate	1.125	-	V/ns
tCKDCD	Duty cycle distortion	0	0.3	ns
tCKMPW	Minimum pulse width	2.2	-	ns
tISU	input set-up time	1.4	-	ns
tIH	input hold time	0.8	-	ns
tISUddr	input set-up time	0.4	-	ns
tIHddr	input hold time	0.4	-	ns
SR	Slew rate	1.125	-	V/ns
tPH	Device output momentary phase from CLK input to CMD or DAT line output	0	10.02	ns
ΔTPH	Delay variation due to temperature change	-350(ΔT=-20deg.C)	1550(ΔT=90deg.C)	ps
tVW	Valid Data Output window	2.88075	-	ns
tPERIOD	Cycle time data transfer mode	5	-	ns
SR	Slew rate	1.125	-	V/ns
tCKDCD	Duty cycle distortion	0	0.2	ns
tCKMPW	Minimum pulse width	2	-	ns
tRQ	Output skew	-	0.4	ns
tRQH	Output hold skew	-	0.4	ns
SR	Slew rate	1.125	-	V/ns



Figure 3. EMMC HS200 Data Output Timing

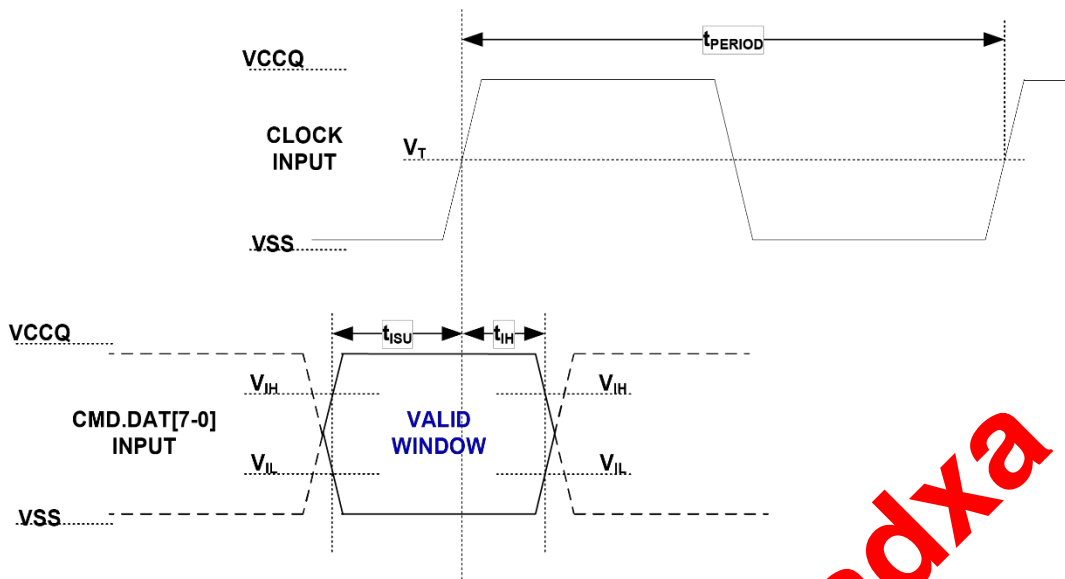
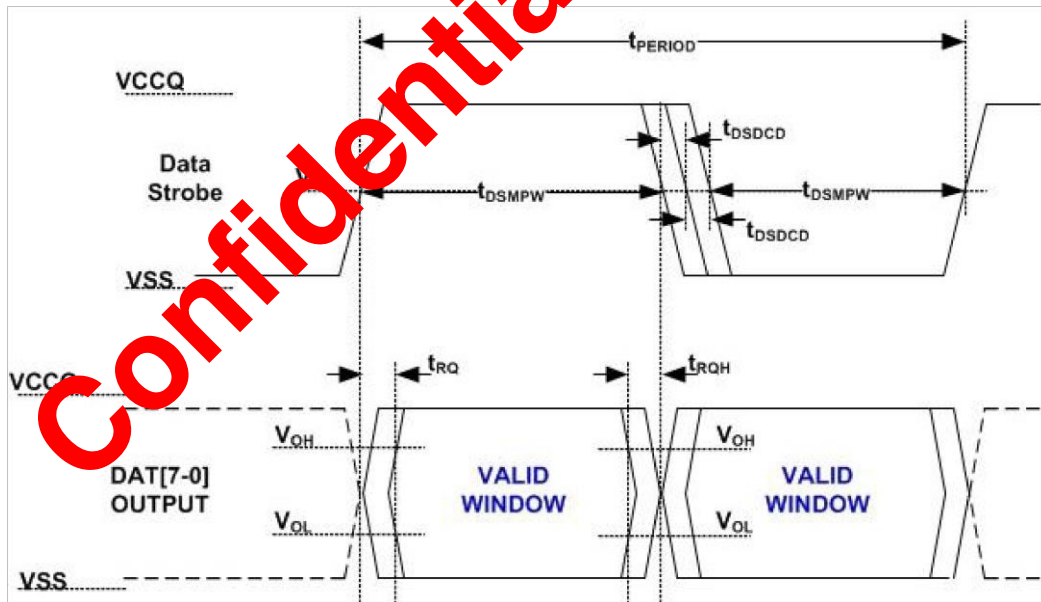


Table 35 HS200 Timing Specification

Symbol	Parameter	Min	Max	Unit
tPERIOD	Cycle time data transfer mode	5	-	ns
tISU	output set-up time	1.4	-	ns
tIH	output hold time	0.8	-	ns

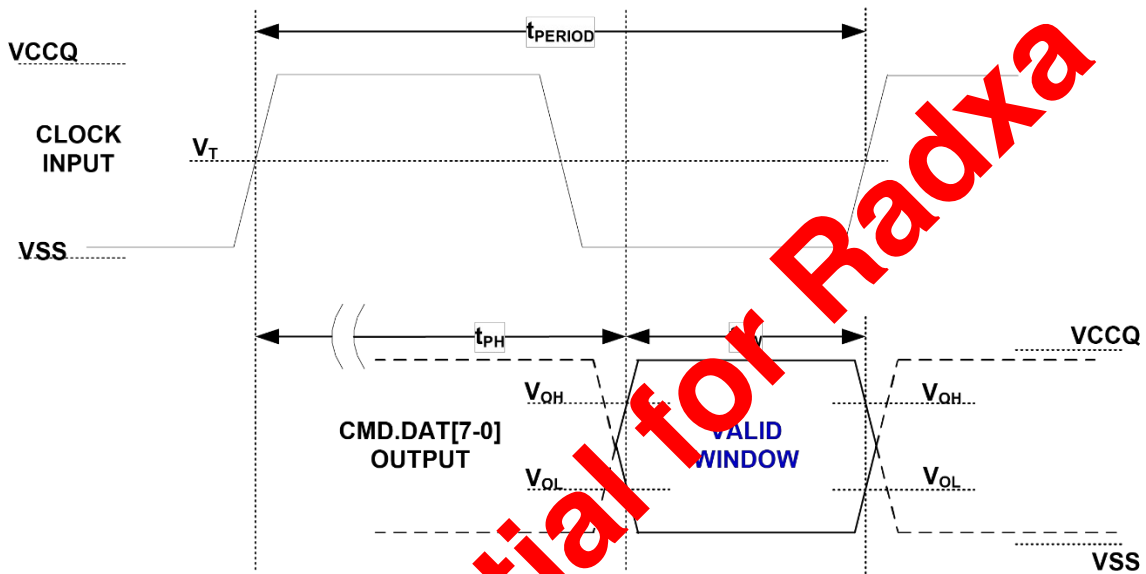
Figure 4. EMMC HS400 Data Input Timing



**Table 36 HS400 Data Input Timing Specification**

Symbol	Parameter	Min	Max	Unit
tPERIOD	Cycle time data transfer mode	5	-	ns
SR	Slew rate	1.125	-	V/ns
tCKDCD	Duty cycle distortion	0	0.2	ns
tCKMPW	Minimum pulse width	2	-	ns
tRQ	Input skew	-	0.4	ns
tRQH	input hold skew	-	0.4	ns

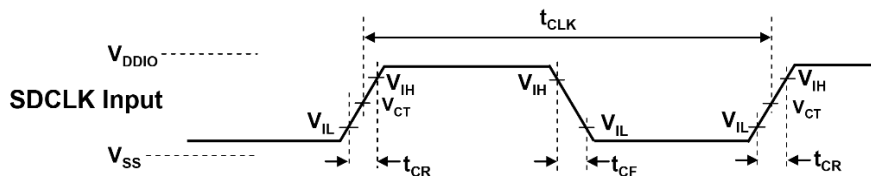
**Figure 5. EMMC HS200 Data Input Timing**



**Table 37 HS200 Timing Specification**

Symbol	Parameter	Min	Max	Unit
tPH	Device output momentary phase from CLK input to CMD or DAT line output. Does not include a long-term temperature drift.	0	2	UI
ΔTPH	Delay variation due to temperature change after tuning. Total output valid window (TVW) shift of output valid window (TVW) from last system tuning procedure Δ TPH is 2600ps for ΔT from -25 °C to +25 °C during operation.	-350(ΔT=-20deg.C)	1550(ΔT=90deg.C)	ps
tVW	Valid Data Simple window	0.575	-	UI

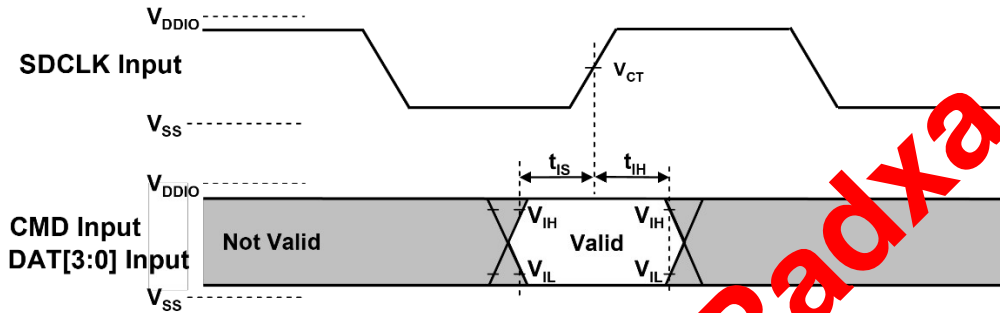
**Figure 6. SD Clock Signal Timing Diagram**



**Table 38 SD Clock Timing Specification**

Symbol	Parameter (SDR104 Mode)	Min	Max	Unit
tCLK	clock period Data Transfer Mode(PP)	4.8	-	ns
Duty	Clock Duty	30	70	%
tCR	clock rise time	-	0.96	ns
tCF	clock fall time	-	0.96	ns

**Figure 7. SD Card Output Timing Diagram**



**Table 39 SD Timing Specification**

Inputs CMD, DAT (referenced to CLK)				
Symbol	Parameter	Min	Max	Unit
tIS	input set-up time	1	-	ns
tIH	input hold time	0.8	-	ns

**4.6.3 NAND Timing Specification**

Nand timing specifications are shown as below:

**Figure 8 Async Waveform for Command/Address/Data Output Timing**

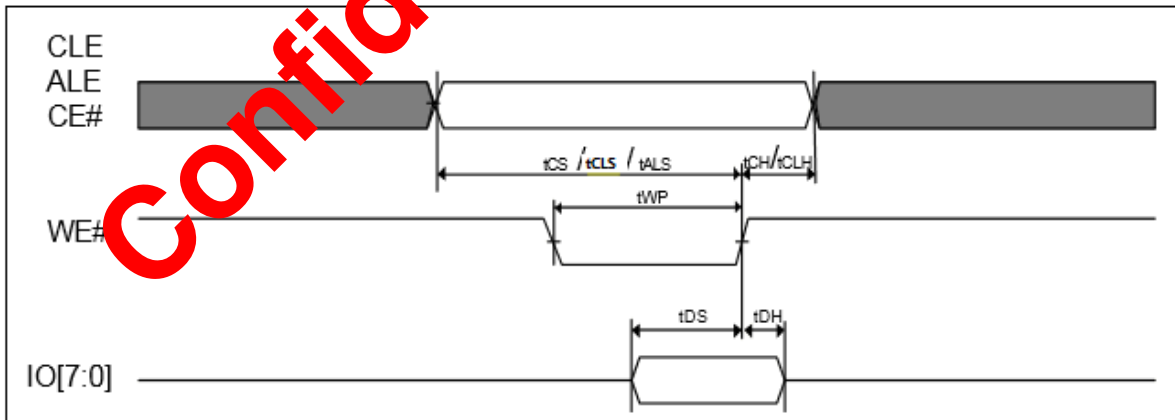


Figure 9 Async Waveform for Address Output Cycle

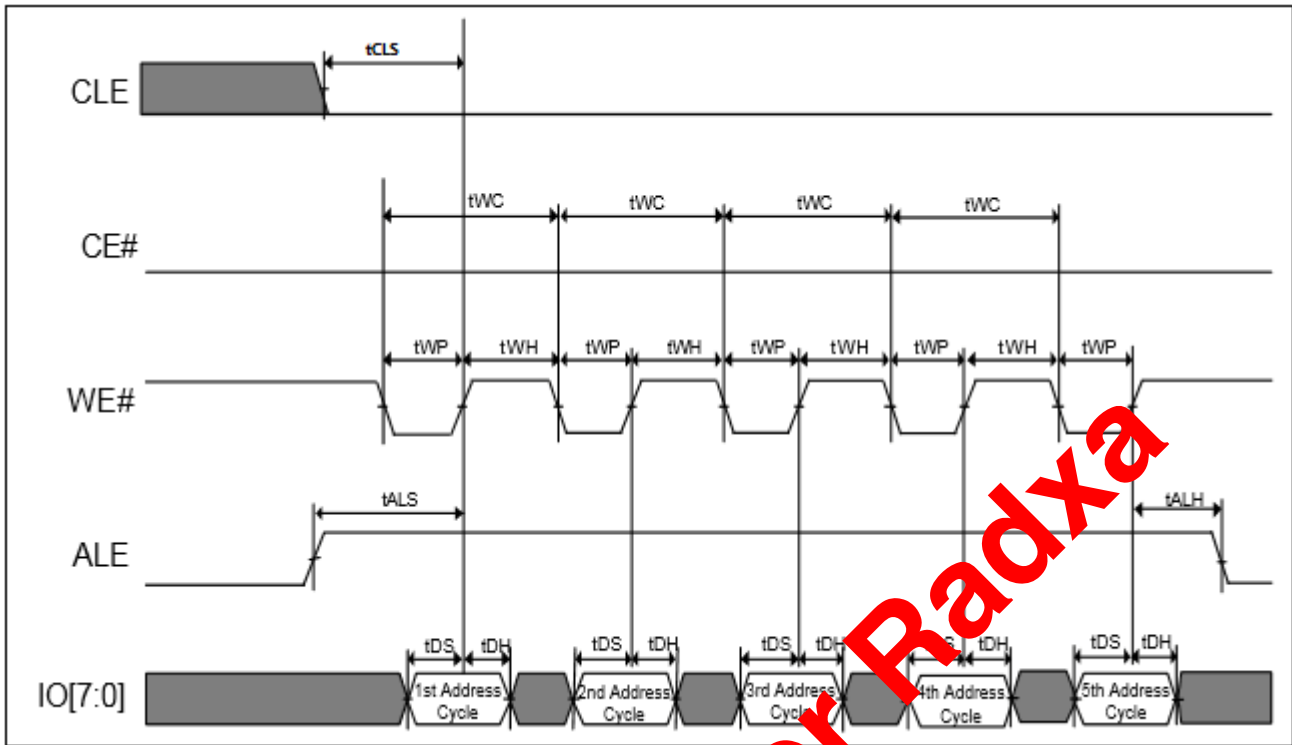


Figure 10 Async Waveform for Sequential Data Read Cycle (After Read)-EOD Mode

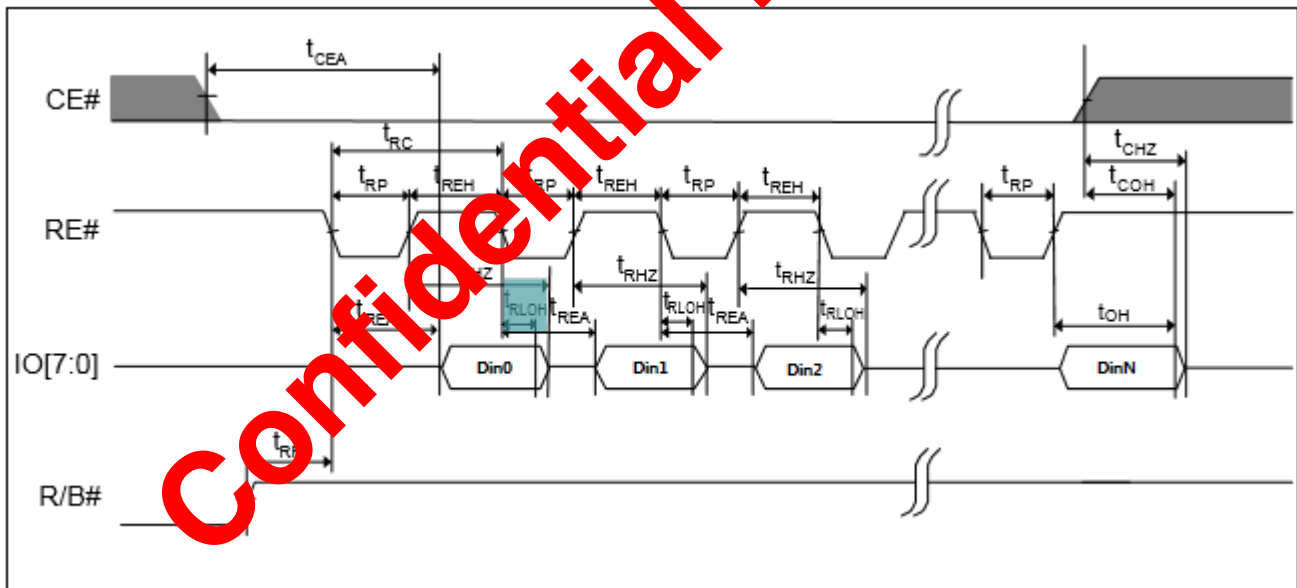


Table 40 Nand Timing Specifications

Symbol	Parameter(Asynchronous) (mode 5)	Min	Max	Unit
tCLS	CLE setup time	10	-	ns
tCLH	CLE hold time	5	-	ns
tALS	ALE setup	10	-	ns
tALH	ALE hold	5	-	ns
tDS	Data setup time	7	-	ns
tDH	Data hold time	5	-	ns

Symbol	Parameter(Asynchronous) (mode 5)	Min	Max	Unit
tWC	WE# cycle time	20	-	ns
tWP	WE# pulse width	10	-	ns
tWH	WE# high hold time	7	-	ns
tREA	RE# access time	-	16	ns
tOH	Data output hold time	15	-	ns
tRLOH	RE#-low to data hold time (EDO)	5	-	ns
tRP	RE# pulse width	10	-	ns
tREH	RE# high hold time	7	-	ns
tRC	RE# cycle time	20	-	ns

### 4.6.4 SPICC Timing Specification

Figure 11. SPICC Timing Diagram

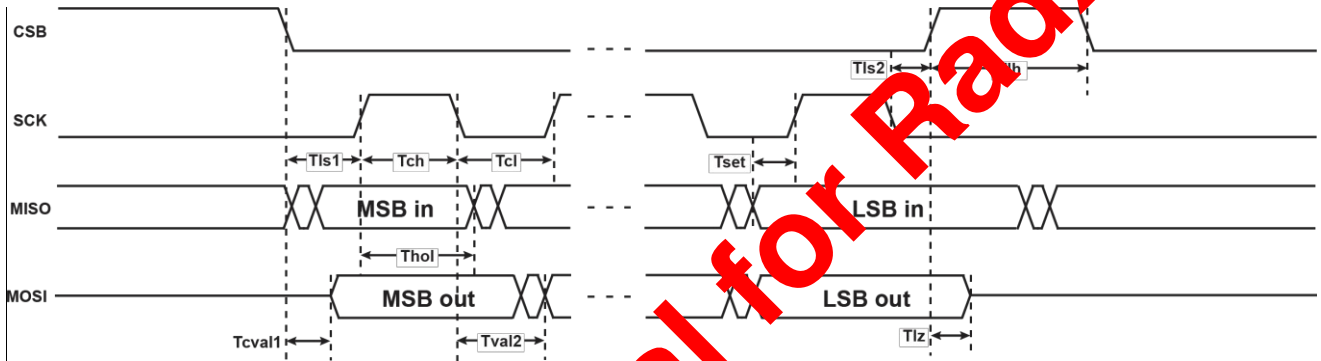


Table 41. SPICC Master Timing Specification

Symbol	Description	Min.	Max.	Unit
fCLK	Clock Frequency	1	80	MHz
TCH	Clock high time	5		ns
TCL	Clock low time	5		ns
TLS1	CS fall to First Rising CLK Edge	50		ns
TSET	Data input Setup Time	4		ns
THOL	Data input Hold Time	4		ns
TLH	Minimum idling time between transfers (minimum ss high time)	5		ns

### 4.6.5 SPIFC Timing Specification

Figure 12. SPIFC Serial Input Timing Diagram

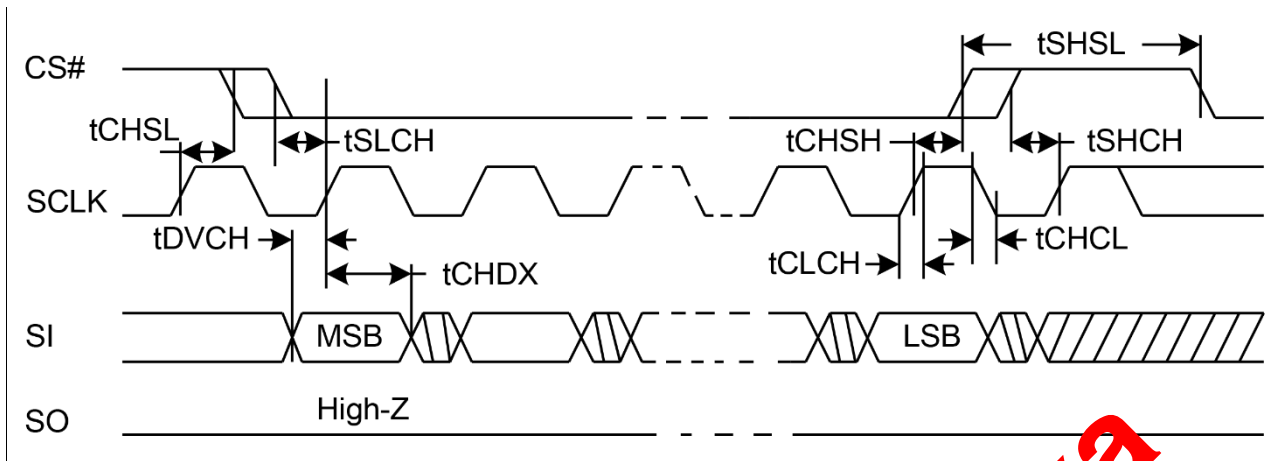


Figure 13. SPIFC Out Timing Diagram

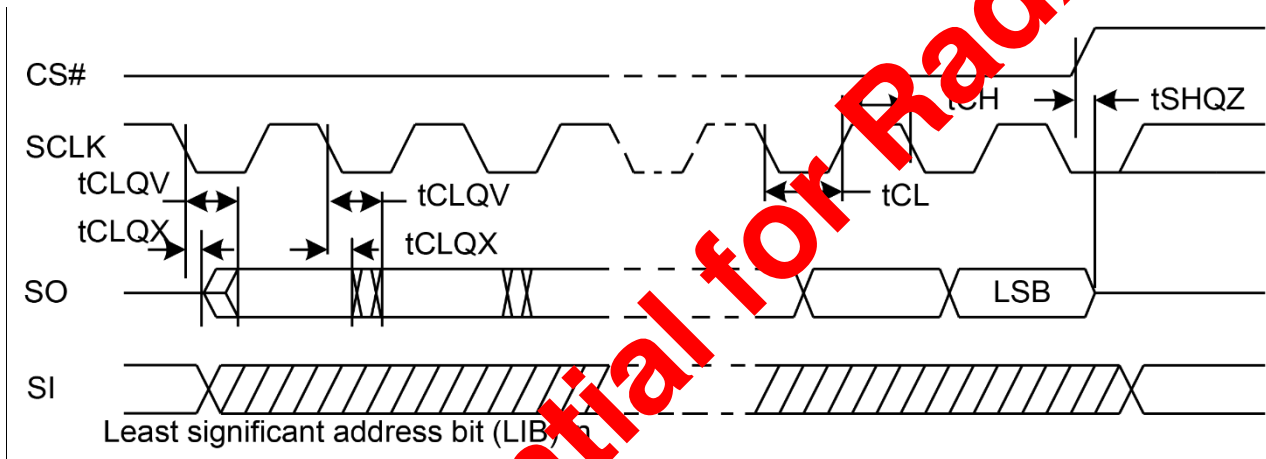


Table 4. SPIFC Master Timing Specification

Symbol	Parameter(Clock 41.7MHz)	Min	Max	Unit
fRSCLK	Clock Frequency for READ instructions		50	Mhz
tCH	Clock High Time	10		ns
tCL	Clock Low Time	10		ns
tCLCH	Clock Rise Time (peak to peak)	0.1		V/ns
tCHCL	Clock Fall Time (peak to peak)	0.1		V/ns
tSLCH	CS# Setup Time (relative to SCLK)	4	-	ns
tCHSH	CS# Active Hold Time (relative to SCLK)	4	-	ns
tDVCH	Data In Setup Time	2	-	ns
tCHDX	Data In Hold Time	3	-	ns
tSHQZ	Output Disable Time (relative to CS#)		8	ns
tCLQV	Clock Low to Output Valid		6	ns
tCLQX	Output Hold Time	1		ns

### 4.6.6 Ethernet Timing Specification

Figure 14. Management Data Timing Diagram

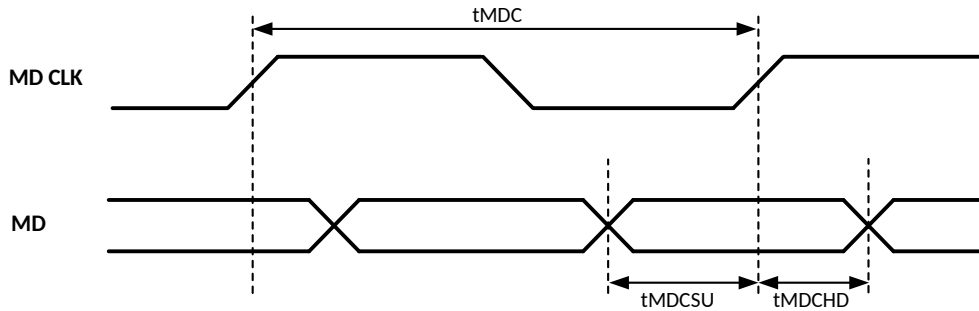


Table 43. Management Data Timing Specification

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
tMDC	MDC clock Period	400	500		ns	From MAC
tMDCSU	Setup time to rising edge of MDC	10			ns	
tMDCHD	Hold time to rising edge of MDC	10			ns	

Figure 15. RMII Timing Diagram

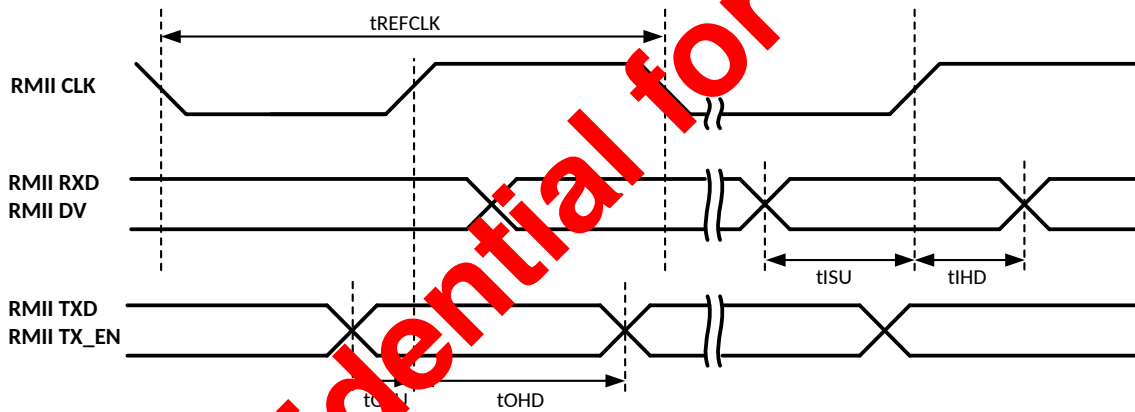


Table 44. RMII Timing Specification

Symbol	Description	Min.	Typ.	Max	Unit	Notes
tREFCLK	RMII clock period		20		ns	50MHz from PHY
tOSU	TXD & TX_EN setup time to rising edge of RMII clock	1.8	10		ns	To PHY
tOHD	TXD & TX_EN hold time to rising edge of RMII clock	1.4	10		ns	To PHY
tISU	RXD & DV setup time to rising edge of RMII clock	1.0	10		ns	From PHY
tIHD	RXD & DV hold time to rising edge of RMII clock	1.0	10		ns	From PHY

Figure 16. RGMII Receive Timing Diagram

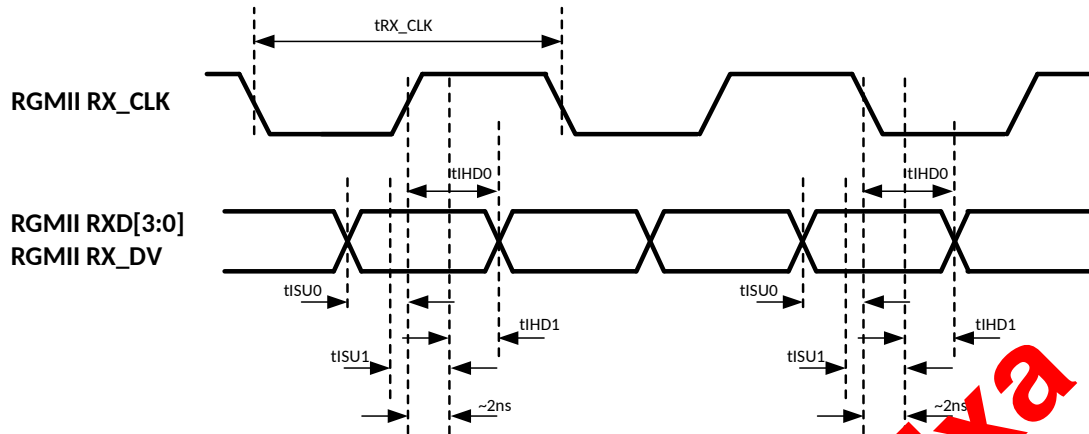


Table 45. RGMII Receive Timing Specification

Symbol	Description	Min.	Typ.	Max	Unit	Notes
tRX_CLK	RGMII RX_CLK clock period		8		ns	125MHz from PHY
tSETUP	RXD[3:0] & RX_DV setup time (PHY internal delay enabled)	1.2			ns	From PHY
tHOLD	RXD[3:0] & RX_DV hold time (PHY internal delay enabled)	1.2			ns	From PHY
tSKEW	RXD[3:0] & RX_DV skew between these 5 signals (PHY internal delay disabled)	-0.5		0.5	ns	From PHY

When PHY internal delay is enabled, check setup/hold timing.

When PHY internal delay is disabled, check signal skew.

Figure 17. RGMII Transmit Timing Diagram

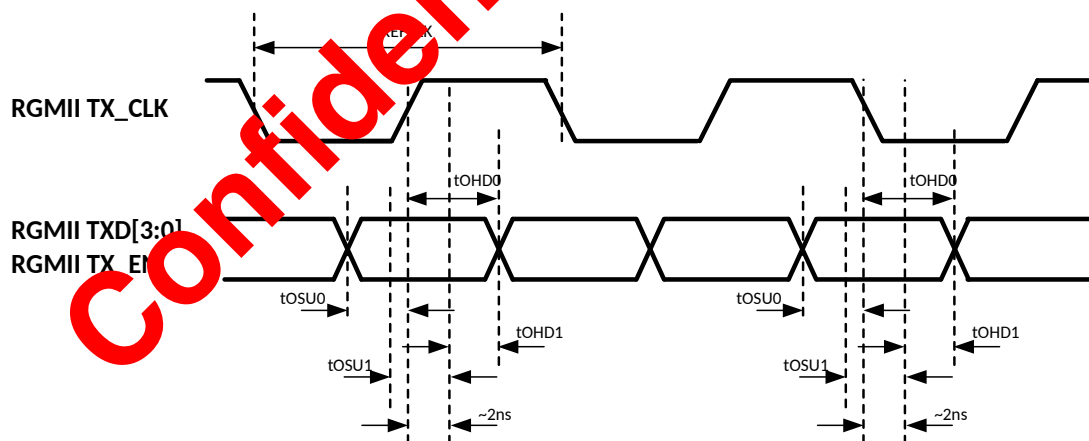


Table 46. RGMII Transmit Timing Specification

Symbol	Description	Min.	Typ.	Max	Unit	Notes
tTX_CLK	RGMII TX_CLK clock period		8		ns	125MHz to PHY
tOSU	TXD & TX_EN setup time to rising edge of RGMII clock (no clock delay added)	1			ns	From PHY
	TXD & TX_EN setup time to rising edge of RGMII clock (clock delay added)	-0.9			ns	From PHY



Symbol	Description	Min.	Typ.	Max	Unit	Notes
tOHD	RXD & DV hold time to rising edge of RGMII clock (no clock delay added)	0.8			ns	From PHY
	RXD & DV hold time to rising edge of RGMII clock (clock delay added)	2.7			ns	From PHY

### 4.6.7 Audio Timing Specification

There are two modes for the audio I2S/TDM interface: Master mode and Slave mode, as shown below.

Figure 18 I2S/TDM Timing Diagram, Master Mode

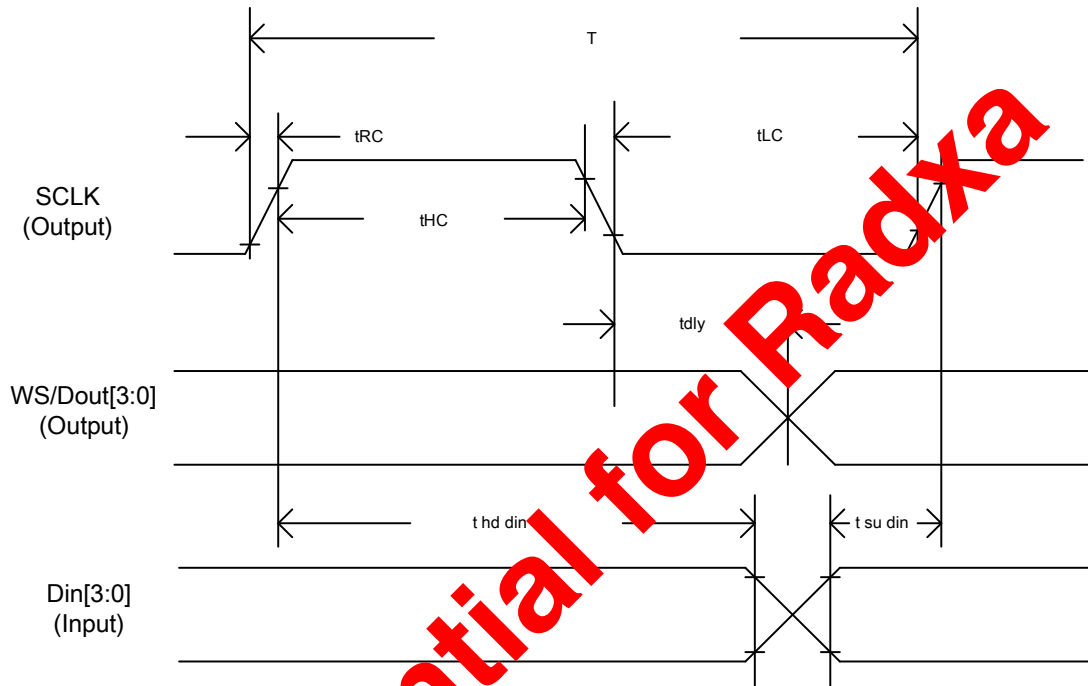


Table 47 Audio I2S/TDM Timing Specification, Transmitter, Master Mode

Transmitter (master mode)					
Symbol	Parameter	Min	Typ	Max	Unit
T	Clock period	10			ns
tHC	High level of SCLK	0.4			T
tLC	Low level of SCLK	0.4			T
tRC	Edge time of SCLK			0.8	ns
tdly	Delay from SCLK to WS	-2	3	5	
tsuin	Setup time of WS/Din	4			ns
thdin	Hold time of WS/Din	4			ns

Figure 19 I2S/TDM Timing Diagram, Slave Mode

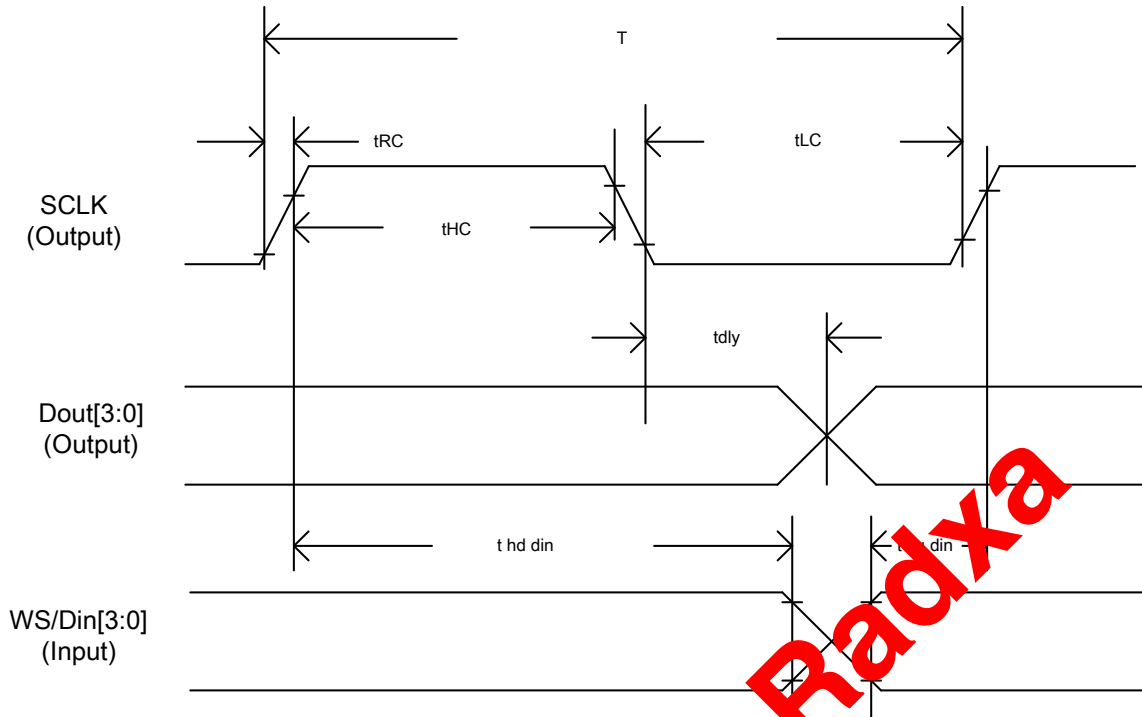


Table 48 Audio I2S/TDM Timing Specification, Transmitter, Slave Mode

Transmitter (slave mode)					
Symbol	Parameter	Min	Typ	Max	unit
T(out)	Clock period	40			ns
T(in)	Clock period	10			ns
tHC	High level of SCLK	0.4			T
tLC	Low level of SCLK	0.4			T
tRC	Edge time of SCLK			0.8	ns
tsu in	Setup time of WS/Din	4			ns
thd in	Hold time of WS/Din	4			ns
tdly	Delay between SCLK and Dout	2	7	10	ns

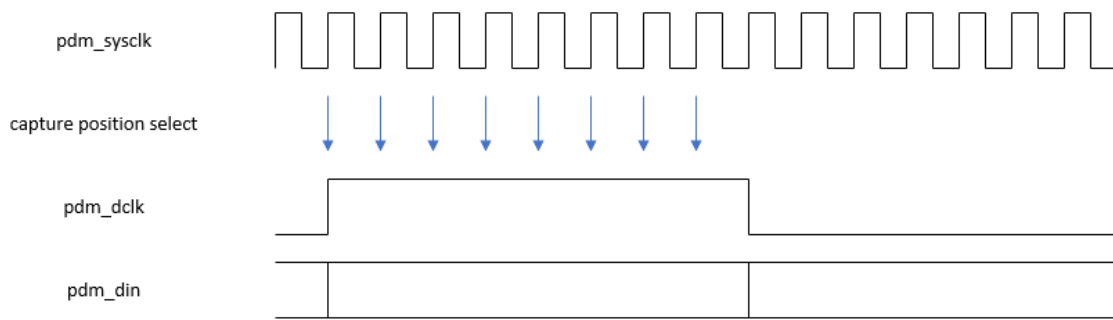
### 4.6.8 PDM Timing Specification

S905D2 using a pdm\_sysclk (configurable freq, typical 200Mhz, much higher than PDM freq.) to sampling PDM data in and PDM CLK, therefore S905D2 don't have a requirement of setup time and hold time.

1. PDM data should be keeping stable not less than 2 periods of pdm\_sysclk.
2. PDM data should be keep same delay to the edge of PDM clk (both rise and fall edge).

See the following picture.

Figure 20 PDM Timing Diagram



**Confidential for Radxa**

## 4.7 Power On Config

3 Boot pins are used as power on config (POC) pins, to set the booting sequence.

POC setting is latched at the rising edge of reset signal.

3 POC pins are all pull high internal, CPU will try to boot from NAND/eMMC first, if fails than try to boot from SD CARD, still fails then try to booting from USB (PC).

External 4.7K ohm pull down resistors can be used to change the POC setting. The resistors should be placed on right location, avoid stubs on high speed signals.

S905Y2's Power On Configuration is listed as following:

**Table 49. Power On Configuration Pin Table**

POC	Boot Pin	Name	Pull low	Pull high
POC0	Boot[4]	SPI NAND First	SPI NAND boot first	Default sequence
POC1	Boot[5]	USB First	USB boot first	Default sequence
POC2	Boot[6]	SPI NOR First	SPI NOR first	Default sequence

**Table 50. Booting Sequence Diagram**

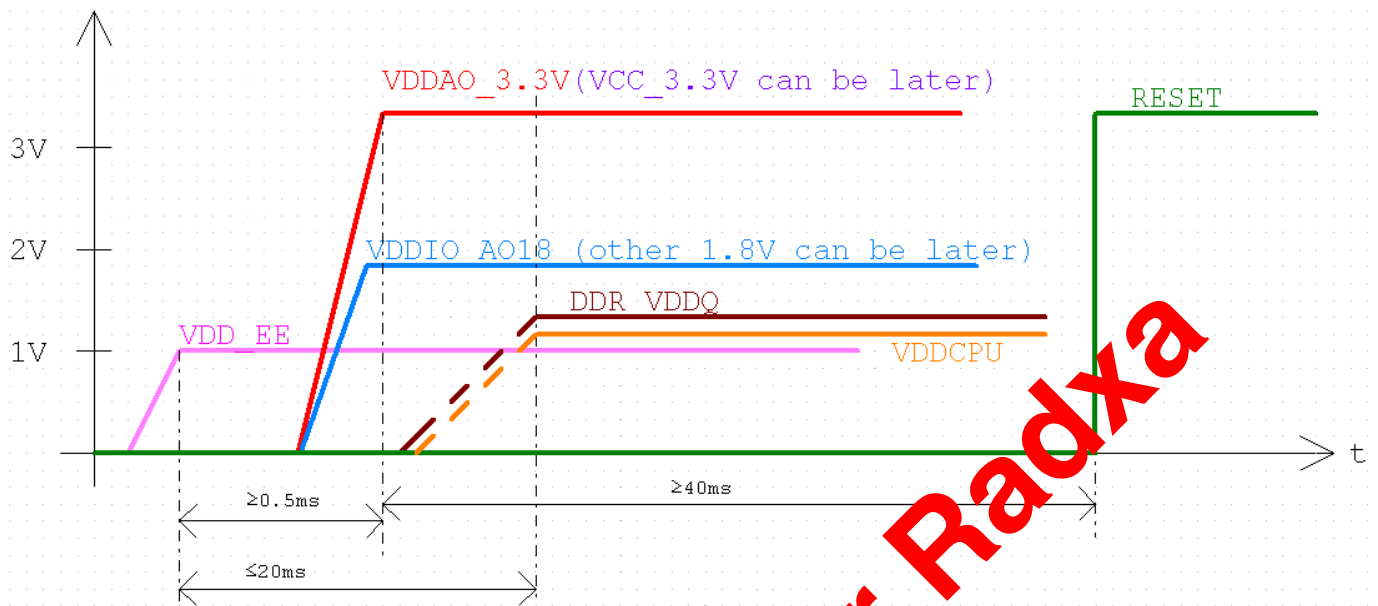
No.	POC_0 (SPI_NAND)	POC_1 (USB_BOOT)	POC_2 (SPI_NOR, eMMC/NAND )	1st Boot device	2nd Boot device	3rd Boot device	4th Boot device
1	0	0	0	USB(short delay)	SPI_NOR	NAND/eMMC	SD Card
2	0	0	1	USB(short delay)	NAND/eMMC	SD Card	-
3	0	1	0	SPI_NOR	NAND/eMMC	SD Card	USB
4	0	1	1	SPI_NAND	NAND/eMMC	USB	-
5	1	0	0	USB(short delay)	SPI_NOR	NAND/eMMC	SD Card
6	1	0	1	USB(short delay)	NAND/eMMC	SD Card	-
7	1	1	0	SPI_NOR	NAND/eMMC	SD Card	USB
8	1	1	1	NAND/eMMC	SD Card	USB	-

Note:

If GPIOC is not work as SDIO port, please do not pull CARD\_DET(GPIOC\_6) low when system booting up, to avoid romcode trying to boot from SD CARD.

## 4.8 Recommended Power on Sequence

Example power on sequence:



Note:

- 1) VDDAO\_3.3V & VCC3.3V & VDDIO\_AO18 should ramp up  $\geq 0.5\mu\text{s}$  later than VDD\_EE.
- 2) All power sources should get stable within 20ms (except for DDR\_VDDQ).
- 3) No sequence requirement between VDDCPU & DDR\_VDDQ and other power source.
- 4) VDDIO\_AO18 should ramp up at the same time with VDDAO\_3.3V & VCC3.3V, VDDAO\_3.3V & VCC3.3V should never be 2.5V higher than VDDIO\_AO18.
- 5) In some designs, VDDCPU & VDD\_EE are merged to VCC\_CORE, the power on sequence should be same as VDD\_EE.
- 6) RESET\_n should keep low for at least 40ms after power up (except DDR\_VDDQ).

Please refer to reference schematics.

Confidential for Radxa

## 4.9 Power Consumption

Note: Values listed here are estimated typical max value tested. Enough margin in circuit needs to be reserved.

Symbol	Maximum Current	Note
VDDCPU	2 A	
VDD_EE	2 A	
VDD_DDR	300mA	Estimate
VDDQ	500mA	

Symbol	Typical current	Maximum current	Note
VDD18_AO_XTAL	1mA	-	EFUSE: Max 100 mA when programming EFUSE
VDDAO_0V8	22mA		
AVDD0V8_PCIE	50mA	-	At 5Gbps mode
AVDD0V8_USB	8mA	8mA	
AVDD0V8_HDMI	23mA		At 6Gbps mode
AVDD_DDRPLL	6mA		
AVDD18_HCSL	8mA	10mA	
AVDD18_PCIE	24mA		At 5Gbps mode
AVDD18_DPLL	19mA	25mA	
AVDD18_HDMI	3.3mA		
AVDD33_HDMI	0mA		Default no current
AVDD18_USB	13.8mA	17mA	
AVDD33_USB	2mA	-	
AVDD18_SARADC	1.2mA		
VDDIO	-		Estimated GPIO power consumption: a pad output continue 100MHz clk (200Mbps) with 10pF loading is about 1.8mA @ 1.8V, 3.3mA @ 3.3V. External capacitor loading, resistance loading, internal pull up/down will affect the power consumption.

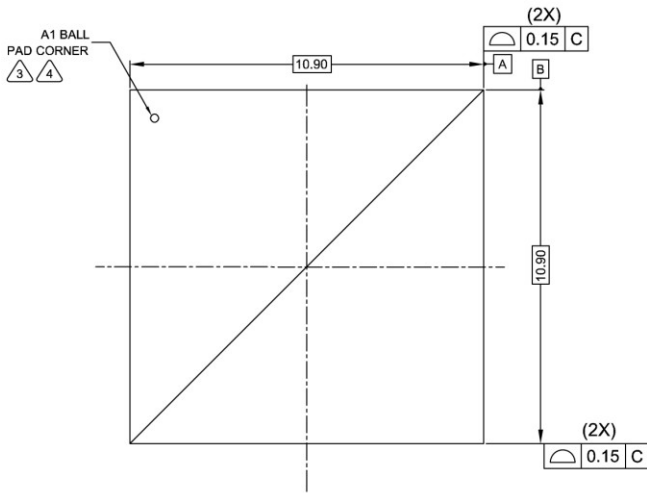
## 4.10 Storage and Baking Conditions

The processor is moisture sensitive device of MSL level 3, defined by IPC/JEDEC J-STD-020. Please follow the storage and backing guidelines.

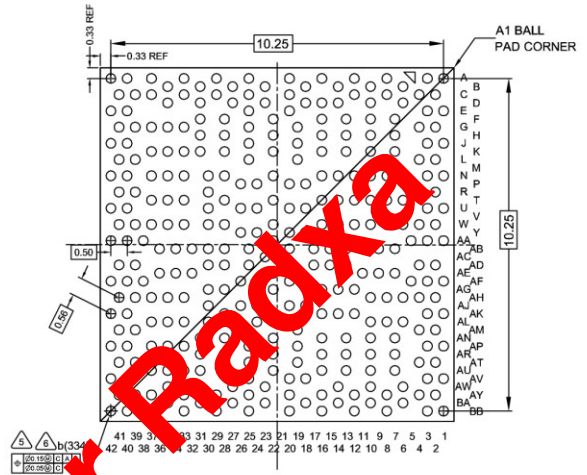
- 1) Calculated shelf life in sealed bag: 12 months at <math>40^{\circ}\text{C}</math> and <math>90\%</math> relative humidity (RH).
- 2) After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be
  - a) Mounted with 168 hours of factory conditions  $\leq 30^{\circ}\text{C}/60\% \text{RH}$ , or
  - b) Stored per J-STD-033
- 3) Devices require bake, before mounting, if Humidity Indicator Card reads >10%.
- 4) If baking is required, refer IPC/JEDEC J-STB-033 for baking process.

# 5. Mechanical Dimensions

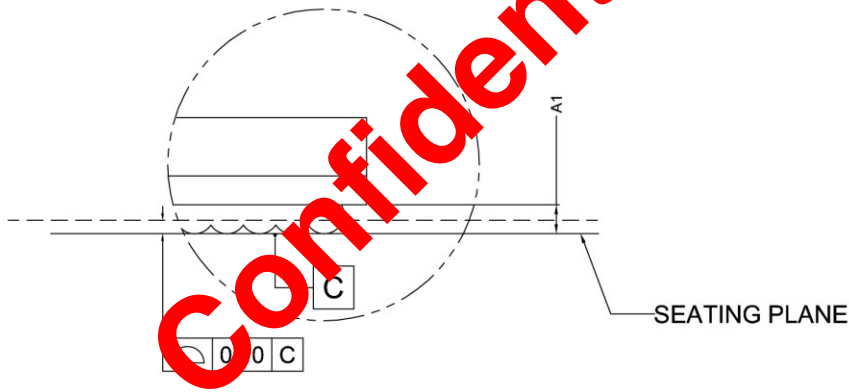
The S905Y2 processor comes in a 42x42 ball matrix FCBGA RoHS package. The mechanical dimensions are given in millimeters as below.



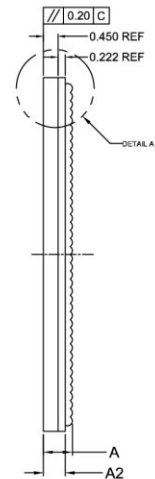
TOP VIEW



BOTTOM VIEW



DETAIL A  
ROTATED 90°



SIDE VIEW

Confidential for Packa

DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	0.825	0.895	0.965
A1	0.183	0.223	0.263
A2	0.622	0.672	0.722
b	0.250	0.300	0.350
NUMBER OF BALL 334			

**Confidential for Radxa**