



PRODUCT BRIEF

JMB585 PCIe Gen3x2 to 5 SATA 6Gb/s Bridge

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Revision History

Revision Number	Effective Date	Description of Revision		Author
		Reference	Description of the Change	
1.0	01/02/2019	-	Draft release	MD Lin

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1 Introduction

The JMB585 is a bridge controller between the PCIe host and the storage devices with SATA/AHCI interface. Its upstream port provides a PCIe which data transmission rate for PCIe Gen 3x2 specification. Meanwhile, its downstream port can connect to SATA/AHCI storage devices, such as a solid-state drive (SSD). The data speed of each port for the SATA port can arrive at 6Gb/s.

Also, the JMB585 SATA Host provides five ports and supports Port Multiplier. JMB585 supports command-based switching (CBS) and FIS (Frame Information Structure)-based switching (FBS). The default communication method between the SATA Host and the port Multiplier is CBS. FBS allows the Host controller to issue multiple commands that send and receive data simultaneously from any drive.

The JMB585 supports TRIM to the SSD and can transmit and receive data by both of AHCI mode and legacy IDE mode to and from the host respectively.

JMB585 is highly integrated with JMicron PCI Express and SATA self-designed PHYs.

Finally, the JMB585 is a new product that almost reaches PCIe Gen3x2 line bandwidth. JMB585 can be applied on PC, Mobile, servers, IPC, consumer electrical devices, storage device, and NVR/DVR system.

2 Features

General Features

- 15 GPIOs for customization.
- SPI interface for external SPI Flash (Option ROM).
- Supports Windows 7, Windows 10 and Linux-base OS
- Supports 3.3V I/O and 1.25V core power.
- 25MHz external crystal.
- 76-pin (2 lane PCIe to 5 SATA port) package.

PCI Express Features

- Supports up to two lane of PCI Express.
- Complies with PCI Express Base Specification Revision 3.1a.
- Supports PCIe link layer power saving mode.
- 100MHz differential PCI Express reference clock in.

SATA Features

- Supports 5 SATA port.
- Supports command-based and FIS-based for Port Multiplier.
- Complies with SATA Specification Revision 3.2.
- Supports AHCI mode and IDE programming interface.
- Supports Native Command Queue (NCQ).
- Supports SATA link power saving mode (partial and slumber)
- Supports SATA plug-in detection capable.
- Supports drive power control and staggered spin-up.
- Supports SATA Partial / Slumber power management state.

3 Block diagram

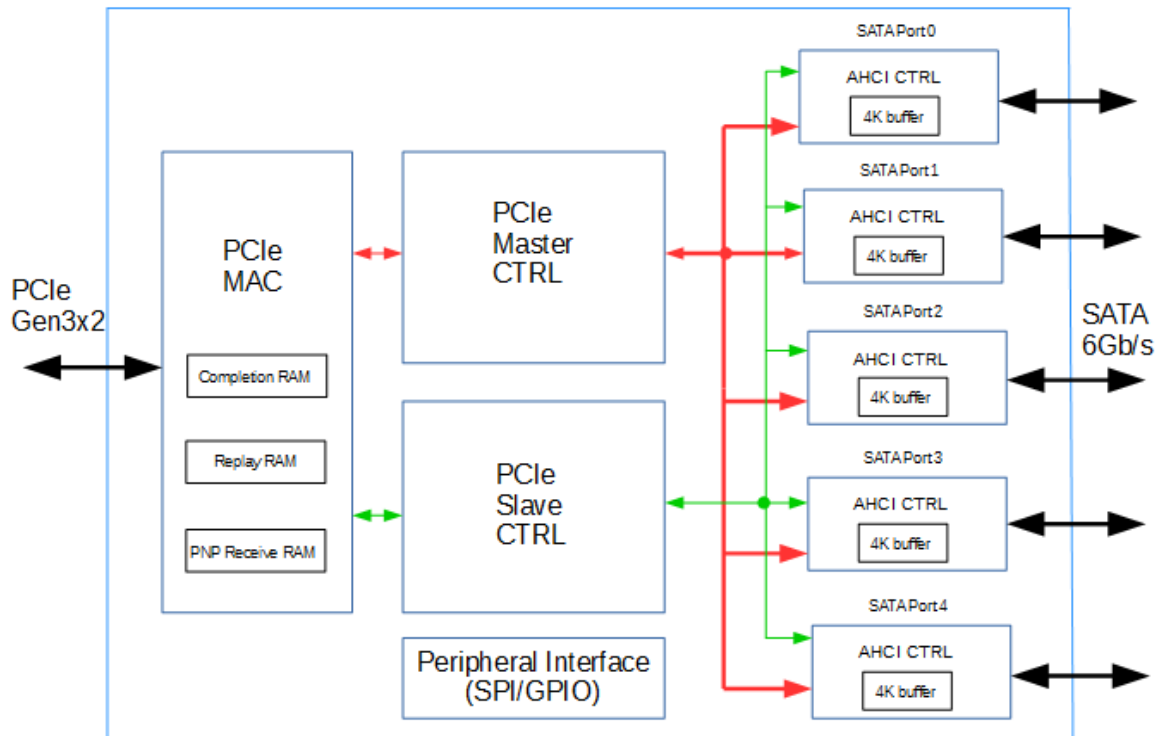


Figure 1 Block diagram

4 Package dimension

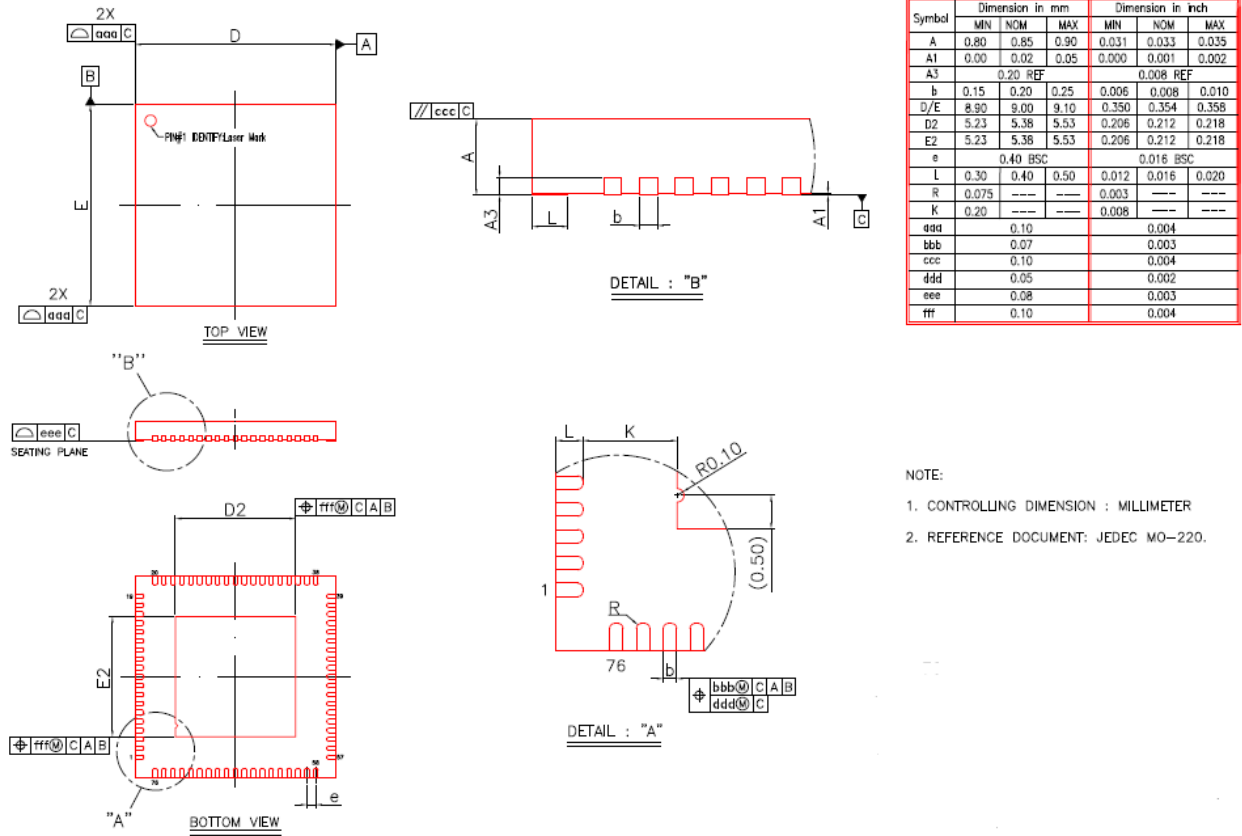


Figure 2 Package outline drawing of QFN76 9x9

A series of thin, light gray lines that resemble a circuit board or data paths, starting from the left and extending towards the right, ending near the bottom right corner.

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