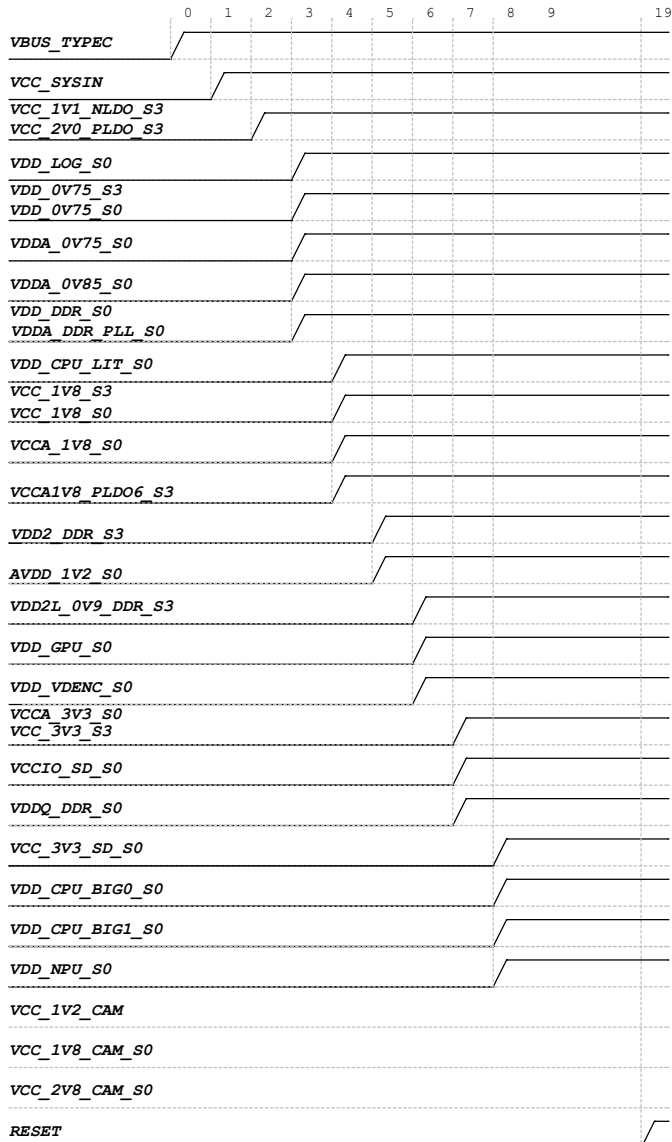


NanoPi R6S



NanoPi R6S		Rev 2208
Size A3	Page Name 01.Title	
Date: Tuesday, December 13, 2022		Sheet: 1 / 27

Power Sequence

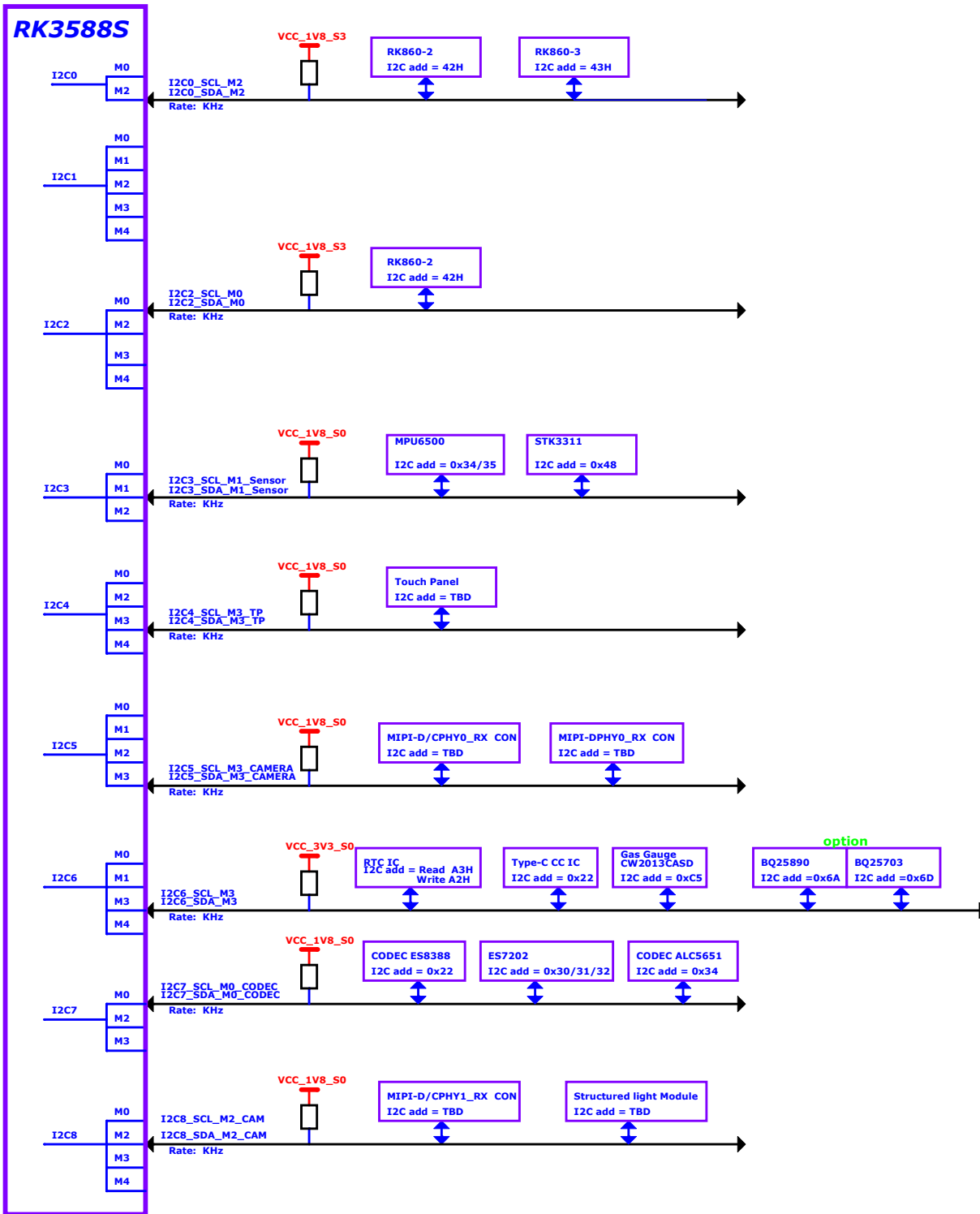


Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC_SYSIN	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO_S3	RK806-1_PLDO1	0.5A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT_BUCK or LDO	2A	VCC_1V2_CAM_S0	OFF	1.2V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_1V8_CAM_S0	OFF	1.8V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_2V8_CAM_S0	OFF	2.8V	OFF	OFF	TBD	TBD

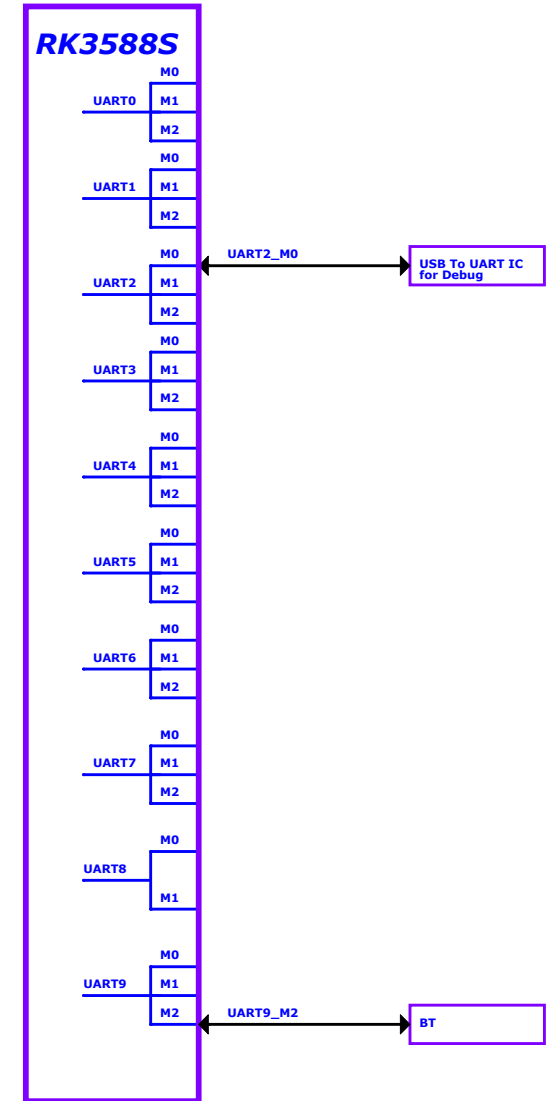
IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO1	Pin N36 N37	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin V37 Y37	1.8V or 3.3V	PMUIO2_1V8	VCC_1V8_S3	1.8V
	Pin V35 V36		PMUIO2	VCC_1V8_S3	1.8V
EMMCIO	Pin AC35	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
	Pin AC36		EMMCIO_1V8	VCC_1V8_S0	1.8V
VCCIO1	Pin H31	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AK11	1.8V or 3.3V	VCCIO2_1V8	VCC_1V8_S0	1.8V
	Pin AK10		VCCIO2	VCC_1Q_SD	1.8V/3.3V
VCCIO4	Pin G27 G28	1.8V or 3.3V	VCCIO4_1V8	VCC_1V8_S0	1.8V
	Pin G31		VCCIO4	VCC_3V3_S0	1.8V
VCCIO5	Pin AF35 AF36	1.8V or 3.3V	VCCIO5_1V8	VCC_1V8_S0	1.8V
	Pin AC33 AC34		VCCIO5	VCC_1V8_S0	1.8V
VCCIO6	Pin A334	1.8V or 3.3V	VCCIO6_1V8	VCC_1V8_S0	1.8V
	Pin AL33 AM33		VCCIO6	VCC_3V3_S0	3.3V

I2C MAP



UART MAP

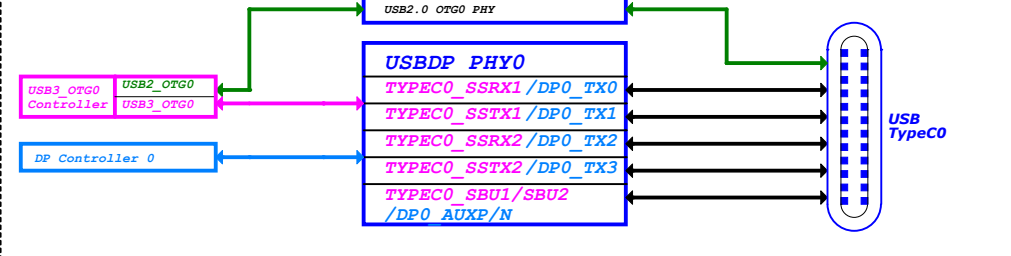


USB Controller Configure Table

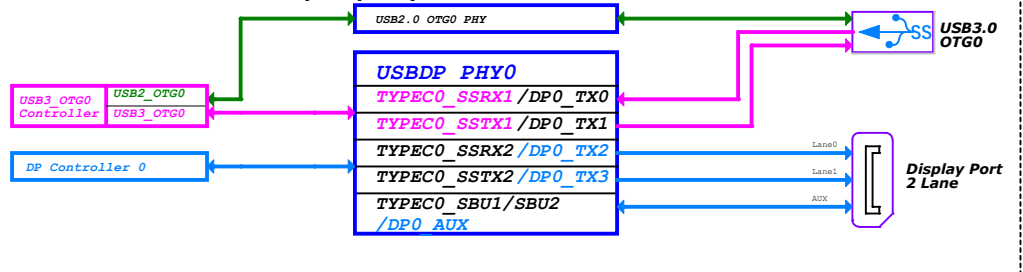
Controller Name	Pin Name	Type-C Function	DPx4Lane+USB20 OTG		USB30 OTG+DPx2Lane Function		USB20 OTG+DPx2Lane Function		USB20 OTG+DPx4Lane Function	
			OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2
USB30 OTG0 Device or Host	TYPEPC0_SBU1/DP0_AUX0	TYPEPC0_SBU1	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0	DP0_AUX0
	TYPEPC0_SBU2/DP0_AUX0N	TYPEPC0_SBU2	DP0_AUX0N	DP0_AUX0N	DP0_AUX0N	DP0_AUX0N	DP0_AUX0N	DP0_AUX0N	DP0_AUX0N	DP0_AUX0N
	TYPEPC0_SSRX1/DP0_TX0	TYPEPC0_SSRX1P	DP0_TX0P	DP0_TX0P	TYPEPC0_SSRX1P	DP0_TX0P	DP0_TX0P	DP0_TX0P	DP0_TX0P	DP0_TX0P
	TYPEPC0_SSRX1N/DP0_TX0N	TYPEPC0_SSRX1N	DP0_TX0N	DP0_TX0N	TYPEPC0_SSRX1N	DP0_TX0N	DP0_TX0N	DP0_TX0N	DP0_TX0N	DP0_TX0N
USB20 OTG0 Device or Host	TYPEPC0_SSTX1/DP0_TX1P	TYPEPC0_SSTX1P	DP0_TX1P	DP0_TX1P	TYPEPC0_SSTX1P	DP0_TX1P	DP0_TX1P	DP0_TX1P	DP0_TX1P	DP0_TX1P
	TYPEPC0_SSTX1N/DP0_TX1N	TYPEPC0_SSTX1N	DP0_TX1N	DP0_TX1N	TYPEPC0_SSTX1N	DP0_TX1N	DP0_TX1N	DP0_TX1N	DP0_TX1N	DP0_TX1N
	TYPEPC0_SSRX2/DP0_TX2P	TYPEPC0_SSRX2P	DP0_TX2P	DP0_TX2P	TYPEPC0_SSRX2P	DP0_TX2P	DP0_TX2P	DP0_TX2P	DP0_TX2P	DP0_TX2P
	TYPEPC0_SSRX2N/DP0_TX2N	TYPEPC0_SSRX2N	DP0_TX2N	DP0_TX2N	TYPEPC0_SSRX2N	DP0_TX2N	DP0_TX2N	DP0_TX2N	DP0_TX2N	DP0_TX2N
USB30 OTG2 Device or Host	TYPEPC0_SSTX2/DP0_TX2P	TYPEPC0_SSTX2P	DP0_TX2P	DP0_TX2P	TYPEPC0_SSTX2P	DP0_TX2P	DP0_TX2P	DP0_TX2P	DP0_TX2P	DP0_TX2P
	TYPEPC0_SSTX2N/DP0_TX2N	TYPEPC0_SSTX2N	DP0_TX2N	DP0_TX2N	TYPEPC0_SSTX2N	DP0_TX2N	DP0_TX2N	DP0_TX2N	DP0_TX2N	DP0_TX2N
	TYPEPC0_SSTX3/DP0_TX3P	TYPEPC0_SSTX3P	DP0_TX3P	DP0_TX3P	TYPEPC0_SSTX3P	DP0_TX3P	DP0_TX3P	DP0_TX3P	DP0_TX3P	DP0_TX3P
	TYPEPC0_SSTX3N/DP0_TX3N	TYPEPC0_SSTX3N	DP0_TX3N	DP0_TX3N	TYPEPC0_SSTX3N	DP0_TX3N	DP0_TX3N	DP0_TX3N	DP0_TX3N	DP0_TX3N
USB20 HOST0	TYPEPC0_SSTX2/DP0_TX2P	TYPEPC0_SSTX2P	DP0_TX2P	DP0_TX2P	TYPEPC0_SSTX2P	DP0_TX2P	DP0_TX2P	DP0_TX2P	DP0_TX2P	DP0_TX2P
	TYPEPC0_SSTX2N/DP0_TX2N	TYPEPC0_SSTX2N	DP0_TX2N	DP0_TX2N	TYPEPC0_SSTX2N	DP0_TX2N	DP0_TX2N	DP0_TX2N	DP0_TX2N	DP0_TX2N
USB20 HOST1	TYPEPC0_SSTX3/DP0_TX3P	TYPEPC0_SSTX3P	DP0_TX3P	DP0_TX3P	TYPEPC0_SSTX3P	DP0_TX3P	DP0_TX3P	DP0_TX3P	DP0_TX3P	DP0_TX3P
	TYPEPC0_SSTX3N/DP0_TX3N	TYPEPC0_SSTX3N	DP0_TX3N	DP0_TX3N	TYPEPC0_SSTX3N	DP0_TX3N	DP0_TX3N	DP0_TX3N	DP0_TX3N	DP0_TX3N

Note:
 DP Lane swap enable
 0: Lane0/1/2/3 TxData mapping to Lane0/1/2/3 TXDP/N
 1: Lane0/1/2/3 TxData mapping to Lane2/3/0/1 TXDP/N

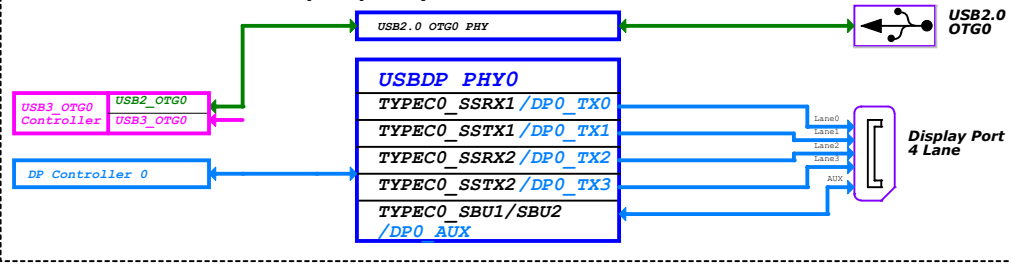
Config0: TypeC0 (With DP function)



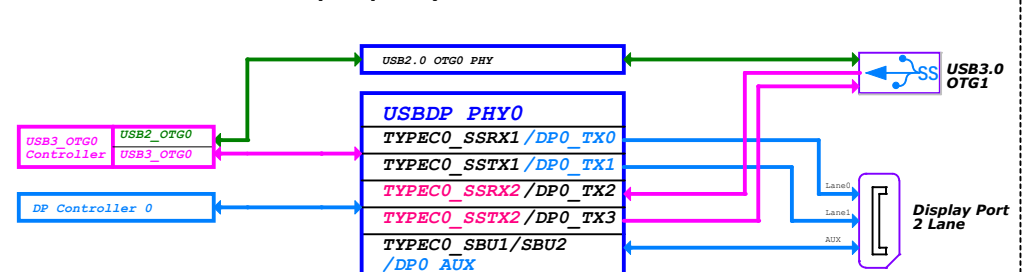
Config3:(Default) USB3.0 OTG0 + DP0 2Lane(Swap ON)



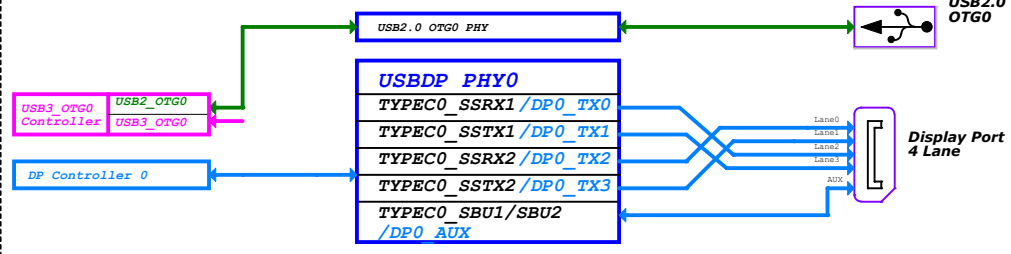
Config1: USB2.0 OTG0 + DP0 4Lane(Swap OFF)



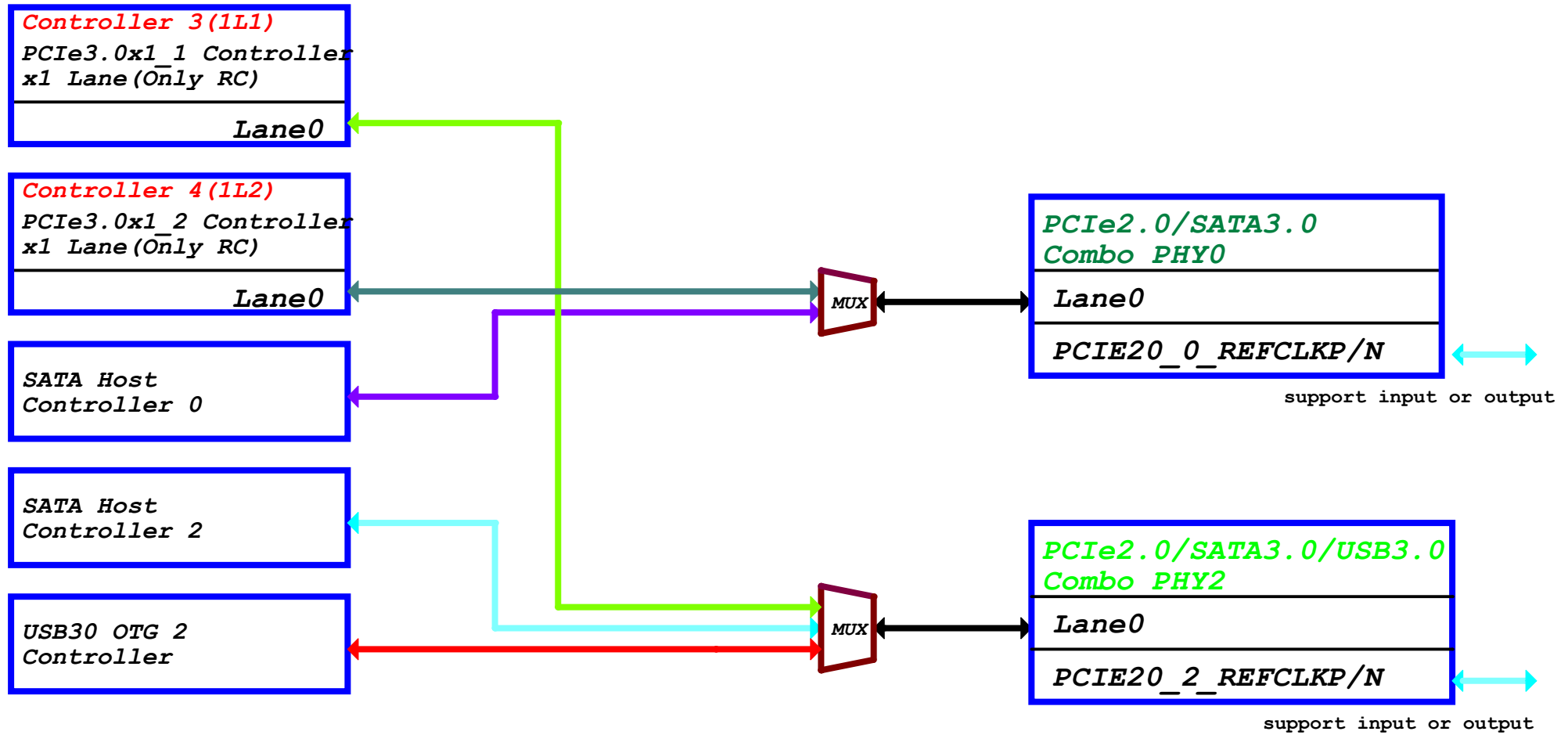
Config4: USB3.0 OTG0 + DP0 2Lane(Swap OFF)



Config2: USB2.0 OTG0 + DP0 4Lane(Swap ON)



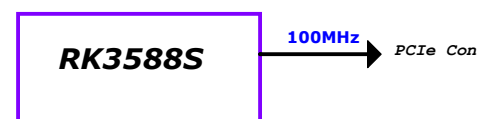
PCIe/SATA Connecter Diagram



PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

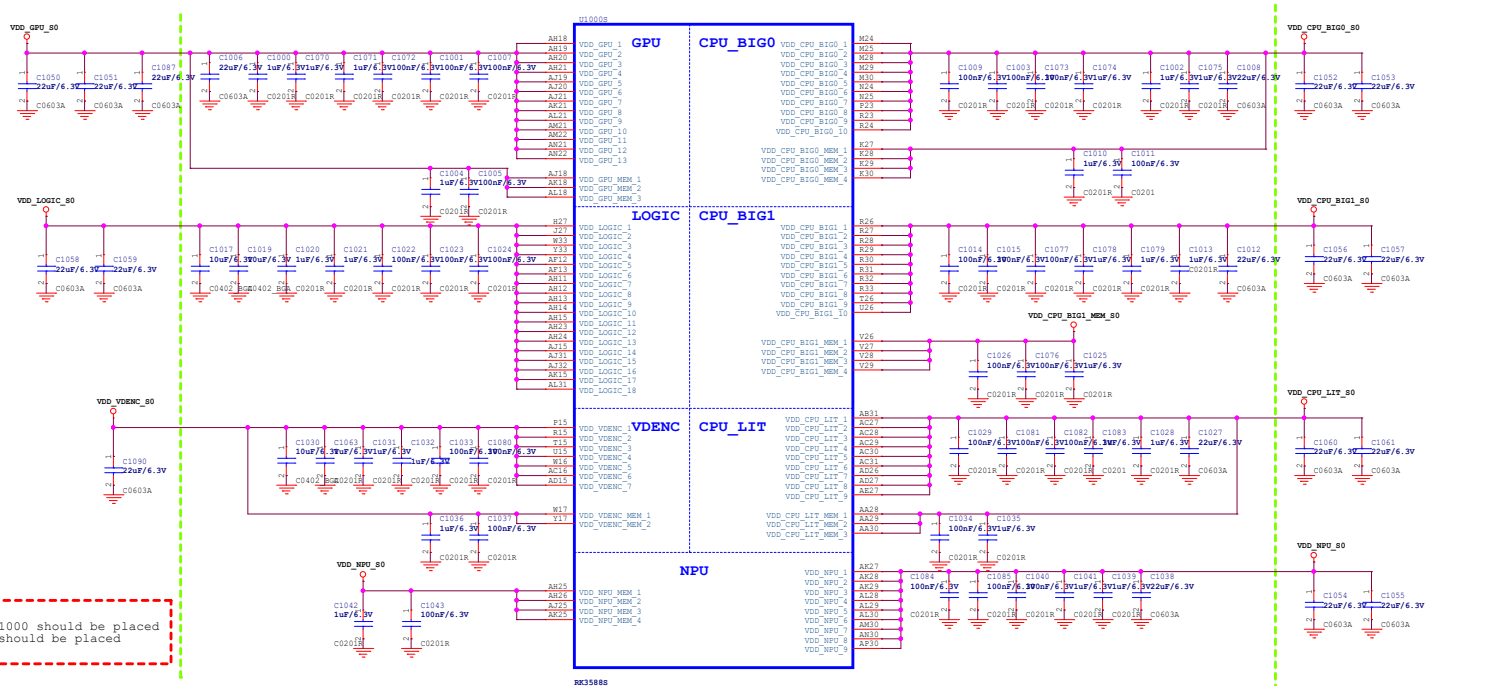
PCIe2.0 REFCLK



Note:

PCIE20*_REFCLKP/N is output or input gpio
M*=Mean to M0 or M1 or M2, It's the same source, Just multiplex to M0 or M1 or M2, Only use one at the same time.

RK3588S (Power&Gnd)



Note:
The Caps between green line and A1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package.

U1000		U1000		U1000		U1000		U1000		U1000		U1000		U1000	
Pin	Value	Pin	Value	Pin	Value	Pin	Value	Pin	Value	Pin	Value	Pin	Value	Pin	Value
A1	VSS_1	A22	VSS_101	A33	VSS_151	A44	VSS_201	A55	VSS_251	A66	VSS_301	A77	VSS_351	A88	VSS_401
A2	VSS_2	A23	VSS_102	A34	VSS_152	A45	VSS_202	A56	VSS_252	A67	VSS_302	A78	VSS_352	A89	VSS_402
A3	VSS_3	A24	VSS_103	A35	VSS_153	A46	VSS_203	A57	VSS_253	A68	VSS_303	A79	VSS_353	A90	VSS_403
A4	VSS_4	A25	VSS_104	A36	VSS_154	A47	VSS_204	A58	VSS_254	A69	VSS_304	A80	VSS_354	A91	VSS_404
A5	VSS_5	A26	VSS_105	A37	VSS_155	A48	VSS_205	A59	VSS_255	A70	VSS_305	A81	VSS_355	A92	VSS_405
A6	VSS_6	A27	VSS_106	A38	VSS_156	A49	VSS_206	A60	VSS_256	A71	VSS_306	A82	VSS_356	A93	VSS_406
A7	VSS_7	A28	VSS_107	A39	VSS_157	A50	VSS_207	A61	VSS_257	A72	VSS_307	A83	VSS_357	A94	VSS_407
A8	VSS_8	A29	VSS_108	A40	VSS_158	A51	VSS_208	A62	VSS_258	A73	VSS_308	A84	VSS_358	A95	VSS_408
A9	VSS_9	A30	VSS_109	A41	VSS_159	A52	VSS_209	A63	VSS_259	A74	VSS_309	A85	VSS_359	A96	VSS_409
A10	VSS_10	A31	VSS_110	A42	VSS_160	A53	VSS_210	A64	VSS_260	A75	VSS_310	A86	VSS_360	A97	VSS_410
A11	VSS_11	A32	VSS_111	A43	VSS_161	A54	VSS_211	A65	VSS_261	A76	VSS_311	A87	VSS_361	A98	VSS_411
A12	VSS_12	A33	VSS_112	A44	VSS_162	A55	VSS_212	A66	VSS_262	A77	VSS_312	A88	VSS_362	A99	VSS_412
A13	VSS_13	A34	VSS_113	A45	VSS_163	A56	VSS_213	A67	VSS_263	A78	VSS_313	A89	VSS_363	A00	VSS_413
A14	VSS_14	A35	VSS_114	A46	VSS_164	A57	VSS_214	A68	VSS_264	A79	VSS_314	A90	VSS_364	A01	VSS_414
A15	VSS_15	A36	VSS_115	A47	VSS_165	A58	VSS_215	A69	VSS_265	A80	VSS_315	A91	VSS_365	A02	VSS_415
A16	VSS_16	A37	VSS_116	A48	VSS_166	A59	VSS_216	A70	VSS_266	A81	VSS_316	A92	VSS_366	A03	VSS_416
A17	VSS_17	A38	VSS_117	A49	VSS_167	A60	VSS_217	A71	VSS_267	A82	VSS_317	A93	VSS_367	A04	VSS_417
A18	VSS_18	A39	VSS_118	A50	VSS_168	A61	VSS_218	A72	VSS_268	A83	VSS_318	A94	VSS_368	A05	VSS_418
A19	VSS_19	A40	VSS_119	A51	VSS_169	A62	VSS_219	A73	VSS_269	A84	VSS_319	A95	VSS_369	A06	VSS_419
A20	VSS_20	A41	VSS_120	A52	VSS_170	A63	VSS_220	A74	VSS_270	A85	VSS_320	A96	VSS_370	A07	VSS_420
A21	VSS_21	A42	VSS_121	A53	VSS_171	A64	VSS_221	A75	VSS_271	A86	VSS_321	A97	VSS_371	A08	VSS_421
A22	VSS_22	A43	VSS_122	A54	VSS_172	A65	VSS_222	A76	VSS_272	A87	VSS_322	A98	VSS_372	A09	VSS_422
A23	VSS_23	A44	VSS_123	A55	VSS_173	A66	VSS_223	A77	VSS_273	A88	VSS_323	A99	VSS_373	A10	VSS_423
A24	VSS_24	A45	VSS_124	A56	VSS_174	A67	VSS_224	A78	VSS_274	A89	VSS_324	A00	VSS_374	A11	VSS_424
A25	VSS_25	A46	VSS_125	A57	VSS_175	A68	VSS_225	A79	VSS_275	A90	VSS_325	A01	VSS_375	A12	VSS_425
A26	VSS_26	A47	VSS_126	A58	VSS_176	A69	VSS_226	A80	VSS_276	A91	VSS_326	A02	VSS_376	A13	VSS_426
A27	VSS_27	A48	VSS_127	A59	VSS_177	A70	VSS_227	A81	VSS_277	A92	VSS_327	A03	VSS_377	A14	VSS_427
A28	VSS_28	A49	VSS_128	A60	VSS_178	A71	VSS_228	A82	VSS_278	A93	VSS_328	A04	VSS_378	A15	VSS_428
A29	VSS_29	A50	VSS_129	A61	VSS_179	A72	VSS_229	A83	VSS_279	A94	VSS_329	A05	VSS_379	A16	VSS_429
A30	VSS_30	A51	VSS_130	A62	VSS_180	A73	VSS_230	A84	VSS_280	A95	VSS_330	A06	VSS_380	A17	VSS_430
A31	VSS_31	A52	VSS_131	A63	VSS_181	A74	VSS_231	A85	VSS_281	A96	VSS_331	A07	VSS_381	A18	VSS_431
A32	VSS_32	A53	VSS_132	A64	VSS_182	A75	VSS_232	A86	VSS_282	A97	VSS_332	A08	VSS_382	A19	VSS_432
A33	VSS_33	A54	VSS_133	A65	VSS_183	A76	VSS_233	A87	VSS_283	A98	VSS_333	A09	VSS_383	A20	VSS_433
A34	VSS_34	A55	VSS_134	A66	VSS_184	A77	VSS_234	A88	VSS_284	A99	VSS_334	A10	VSS_384	A21	VSS_434
A35	VSS_35	A56	VSS_135	A67	VSS_185	A78	VSS_235	A89	VSS_285	A00	VSS_335	A11	VSS_385	A22	VSS_435
A36	VSS_36	A57	VSS_136	A68	VSS_186	A79	VSS_236	A90	VSS_286	A01	VSS_336	A12	VSS_386	A23	VSS_436
A37	VSS_37	A58	VSS_137	A69	VSS_187	A80	VSS_237	A91	VSS_287	A02	VSS_337	A13	VSS_387	A24	VSS_437
A38	VSS_38	A59	VSS_138	A70	VSS_188	A81	VSS_238	A92	VSS_288	A03	VSS_338	A14	VSS_388	A25	VSS_438
A39	VSS_39	A60	VSS_139	A71	VSS_189	A82	VSS_239	A93	VSS_289	A04	VSS_339	A15	VSS_389	A26	VSS_439
A40	VSS_40	A61	VSS_140	A72	VSS_190	A83	VSS_240	A94	VSS_290	A05	VSS_340	A16	VSS_390	A27	VSS_440
A41	VSS_41	A62	VSS_141	A73	VSS_191	A84	VSS_241	A95	VSS_291	A06	VSS_341	A17	VSS_391	A28	VSS_441
A42	VSS_42	A63	VSS_142	A74	VSS_192	A85	VSS_242	A96	VSS_292	A07	VSS_342	A18	VSS_392	A29	VSS_442
A43	VSS_43	A64	VSS_143	A75	VSS_193	A86	VSS_243	A97	VSS_293	A08	VSS_343	A19	VSS_393	A30	VSS_443
A44	VSS_44	A65	VSS_144	A76	VSS_194	A87	VSS_244	A98	VSS_294	A09	VSS_344	A20	VSS_394	A31	VSS_444
A45	VSS_45	A66	VSS_145	A77	VSS_195	A88	VSS_245	A99	VSS_295	A10	VSS_345	A21	VSS_395	A32	VSS_445
A46	VSS_46	A67	VSS_146	A78	VSS_196	A89	VSS_246	A00	VSS_296	A11	VSS_346	A22	VSS_396	A33	VSS_446
A47	VSS_47	A68	VSS_147	A79	VSS_197	A90	VSS_247	A01	VSS_297	A12	VSS_347	A23	VSS_397	A34	VSS_447
A48	VSS_48	A69	VSS_148	A80	VSS_198	A91	VSS_248	A02	VSS_298	A13	VSS_348	A24	VSS_398	A35	VSS_448
A49	VSS_49	A70	VSS_149	A81	VSS_199	A92	VSS_249	A03	VSS_299	A14	VSS_349	A25	VSS_399	A36	VSS_449
A50	VSS_50	A71	VSS_150	A82	VSS_200	A93	VSS_250	A04	VSS_300	A15	VSS_350	A26	VSS_400	A37	VSS_450

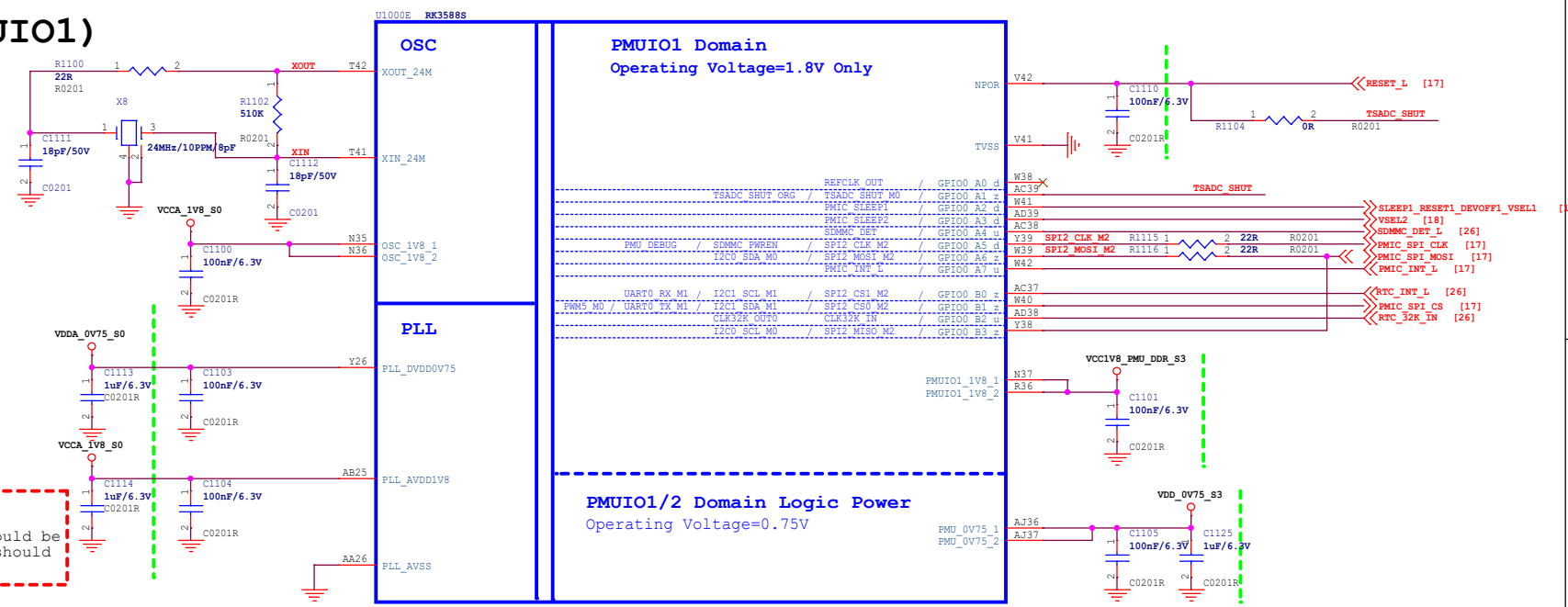
RK3588S (OSC/PLL/PMUIO1)

Note:
Adjusted the load capacitance according to the crystal specification

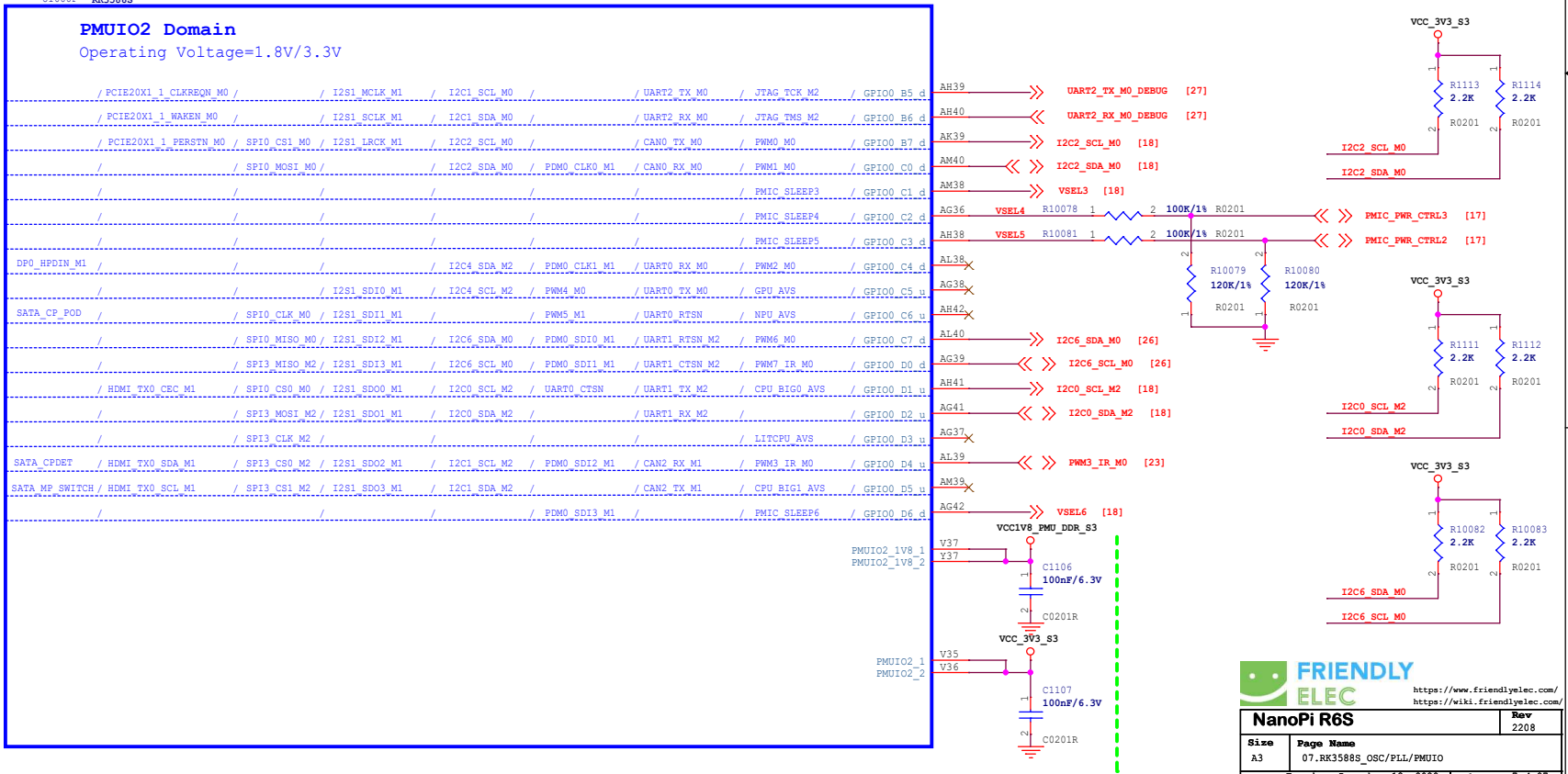
The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

$CL = \{CL1 * CL2 / (CL1 + CL2)\} + PCB \text{ strays}$
Total $CL <= 12pF$

Note:
The Caps between green line and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

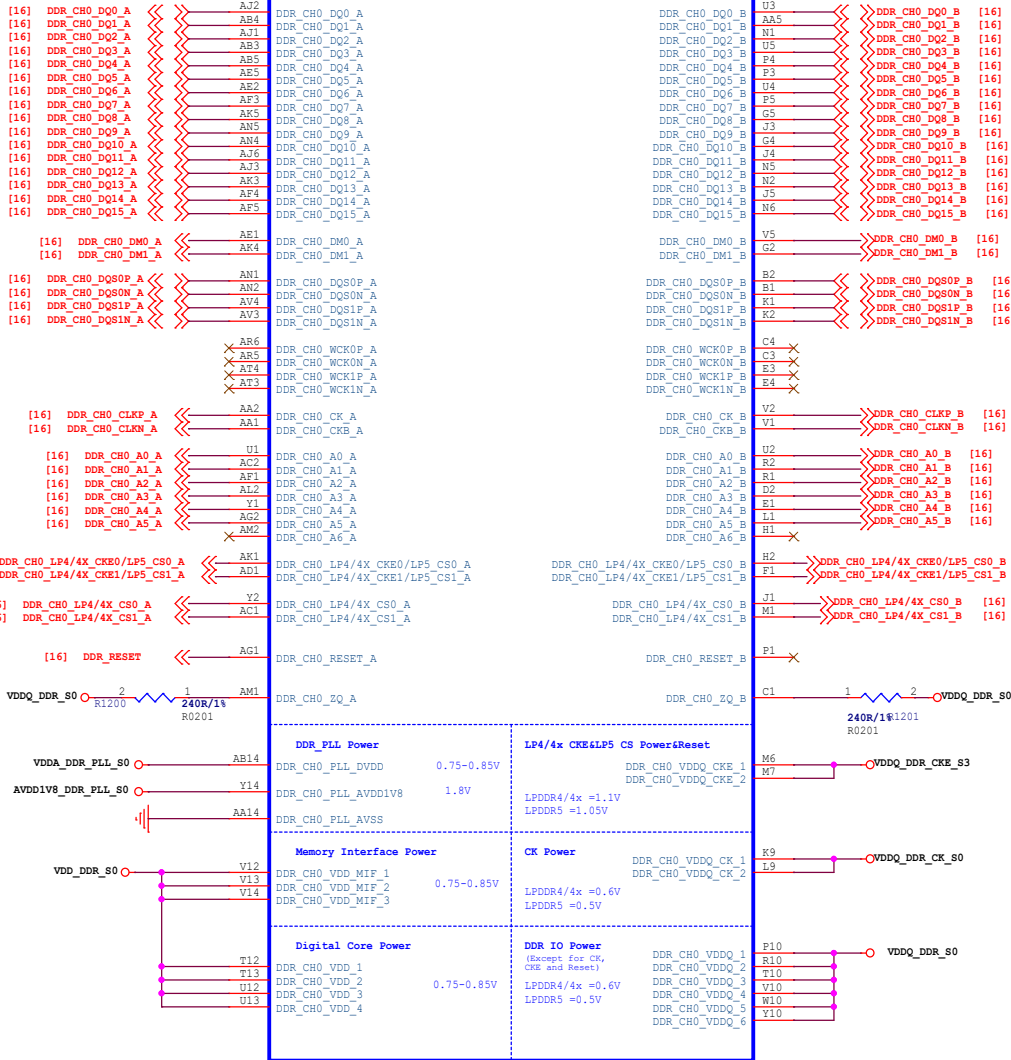


RK3588S (PMUIO2)

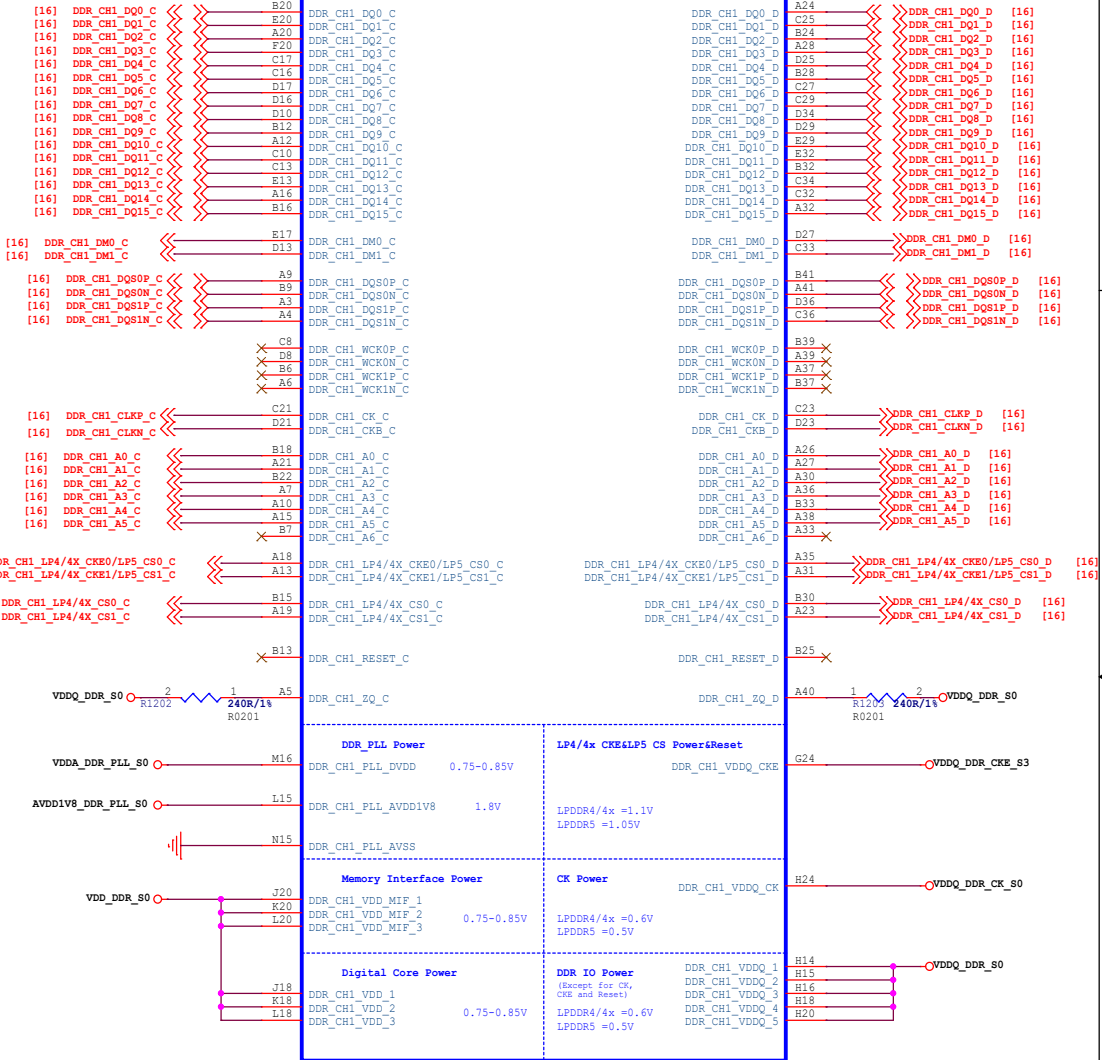


RK3588S (DDR PHY)

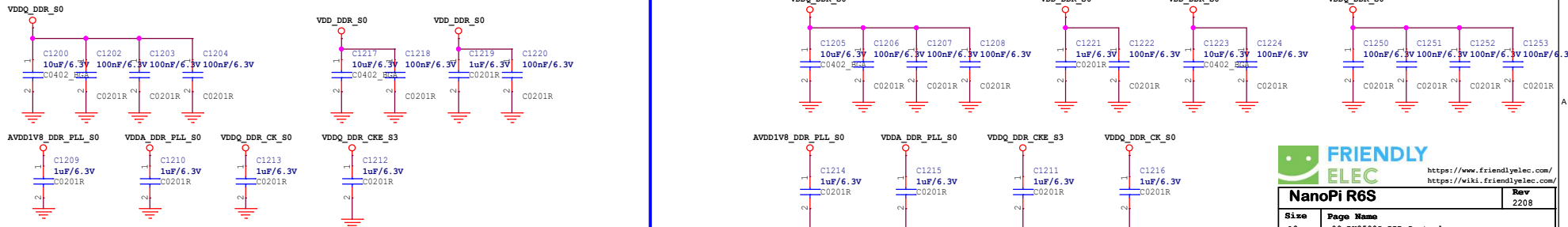
U1000A RK3588S



U1000B RK3588S



DDR FILTER



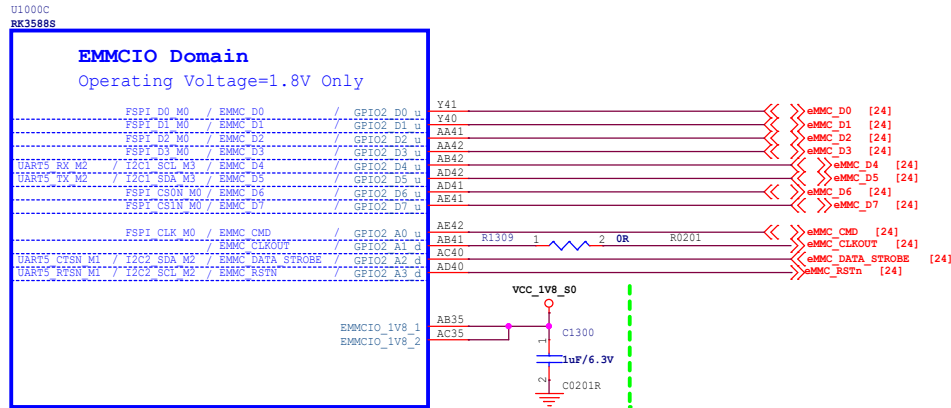
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NanoPi R6S

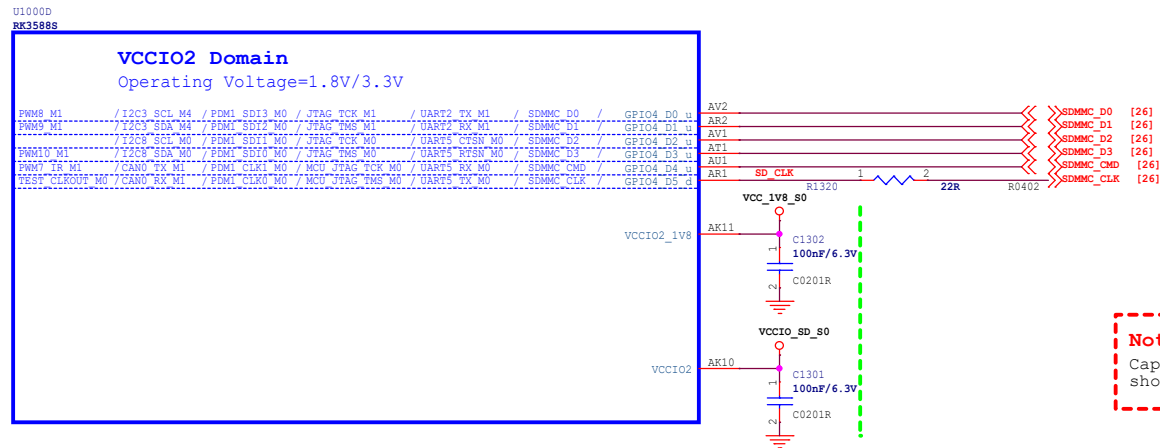
Size	Page Name	Rev
A3	08_RK3588S DDR Controller	2208

Date: Tuesday, December 13, 2022 Sheet: 8 / 27

RK3588S (EMMCIO Domain)



RK3588S (VCCIO2 Domain)



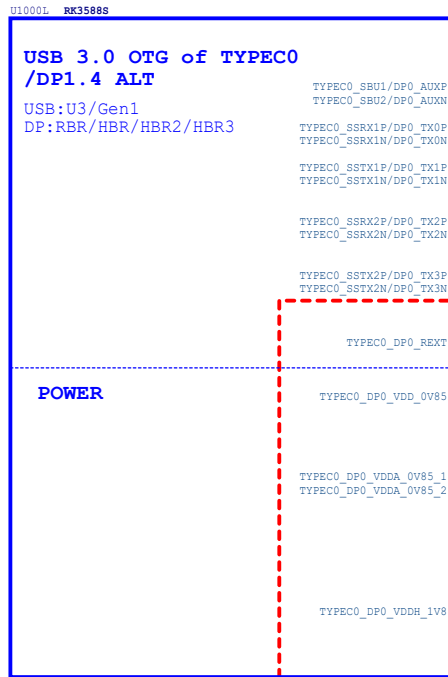
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3588S (USB3.0/DP1.4)

USB30/DP1.4 Alt Mode Configuration

Option1	DP x4Lane	DP_TX_Lane0-3
Option2	TYPEC x4Lane	SSTX 1P/1N SSTX 2P/2N SSRX 1P/1N SSRX 2P/2N
Option3	USB30X2Lane+DPX2Lane	USB30:SSTX 1P/1N SSRX 1P/1N DP:Lane2 Lane3
Option4	USB30X2Lane+DPX2Lane	USB30:SSTX 2P/2N SSRX 2P/2N DP:Lane0 Lane1

DP Lane
Swap Off:
Lane0/1/2/3_TXdata mapping to Lane0/1/2/3_TXDP/N
Swap On:
Lane0/1/2/3_TXdata mapping to Lane2/3/0/1_TXDP/N

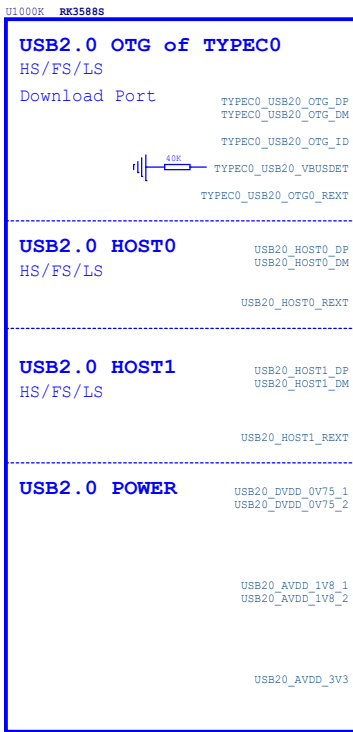


TYPEC&DP MUX Differential Pair:
DATE:95 Ohm +10%
For Typec

USB30 Differential Pair: DP Differential Pair:
DATE:90 Ohm +10% DATE:100 Ohm +10%
For USB30 For DP

Do not delete!!!
If TYPECO is not used:
Signal:leave floating
REXT:8.2K ohm 1% resistor must
be connected externally
Power: Must supply power

RK3588S (USB2.0)



Note:
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 24K ohm resistor.The VBUSDETpin voltage range <=3.3V.

Note:
TYPECO_USB20_OTG:
DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

USB20_HOST0/USB20_HOST1:
If not used:
DP/DM:Leave floating
REXT:Leave floating

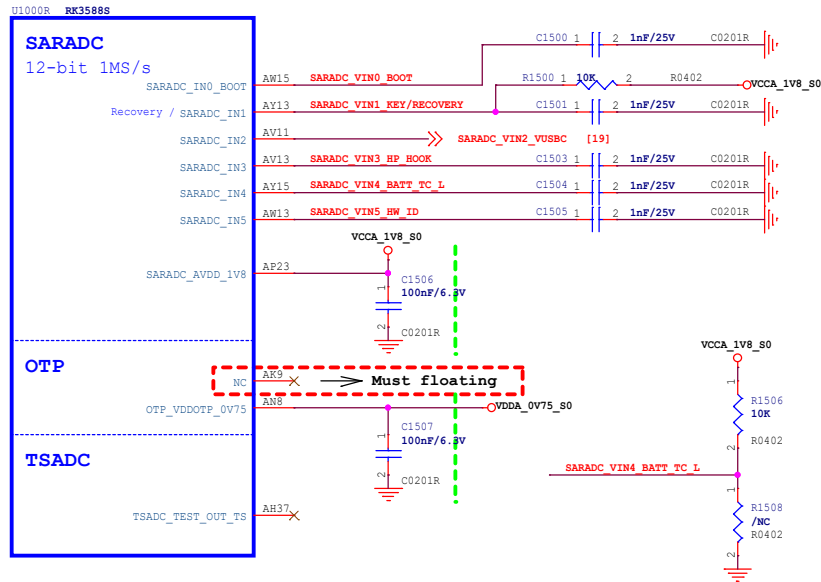
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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<https://wiki.friendlyelec.com/>

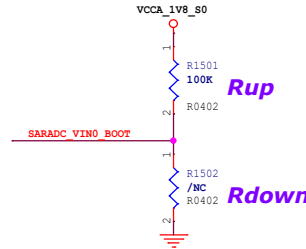
NanoPi R6S		Rev 2208
Size A3	Page Name 10_RK3588S_USB20/USB30/DP_PHY	
Date: Tuesday, December 13, 2022	Sheet: 10/ 27	

RK3588S (SARADC/OTP/TSADC)

← SARADC_VIN0_BOOT [27]

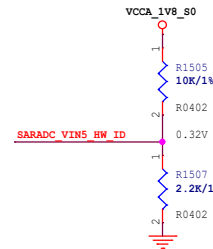


BOOT MODE CONFIG



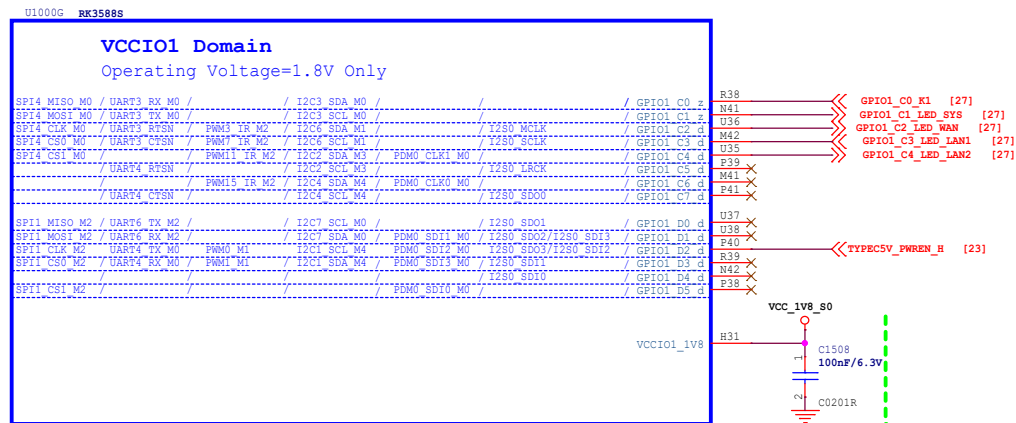
Item	Rup	Rdown	ADC	BOOT MODE(saradc_in5)
LEVEL1	DNP	100K	0	USB (Maskrom mode)
LEVEL2	100K	20K	682	SD Card-USB
LEVEL3	100K	51K	1365	EMMC-USB
LEVEL4	100K	100K	2047	FSPI M0-USB
LEVEL5	100K	200K	2730	FSPI M1-USB
LEVEL6	100K	499K	3412	FSPI M2-USB
LEVEL7	100K	DNP	4095	FSPI_M2-FSPI_M0-EMMC -SD Card-USB

BOARD ID CONFIG



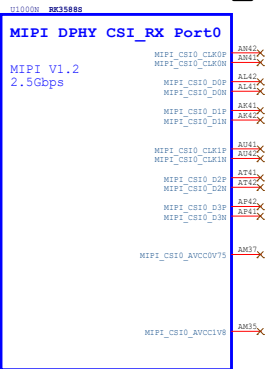
	0.32V (8GB)	0.429V (4GB)
R1505	10K/1%	15K/1%
R1507	2.2K/1%	4.7K/1%

RK3588S (VCCIO1 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3588S (MIPI_DPHY CSIO RX)



MIPI CSI Differential Pair:
100 Ohm +/-10%

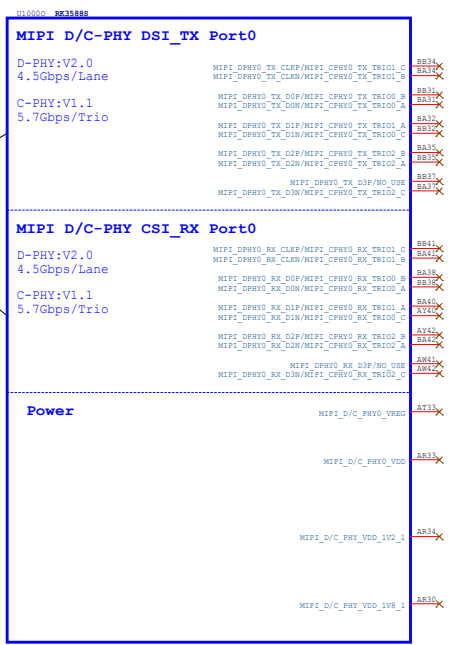
Note:
If not used:
Signal:leave floating
Power: Floating

Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3, but clock lane1 is invalid; In dual clock lanes mode, CLK0P/0N is the clock lane of Data lane0 and Data lane1, while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

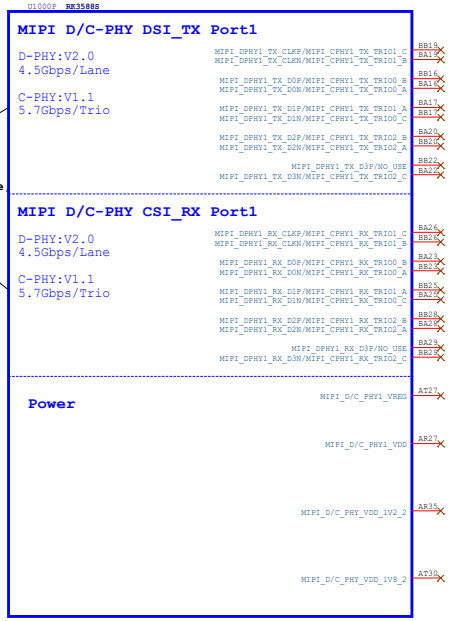
RK3588S (MIPI_D/C PHY0)



TX and RX port must work in the same mode, DPHY or CPHY

Note:
If not used:
Signal:leave floating
Power: Floating

RK3588S (MIPI_D/C PHY1)



TX and RX port must work in the same mode DPHY or CPHY

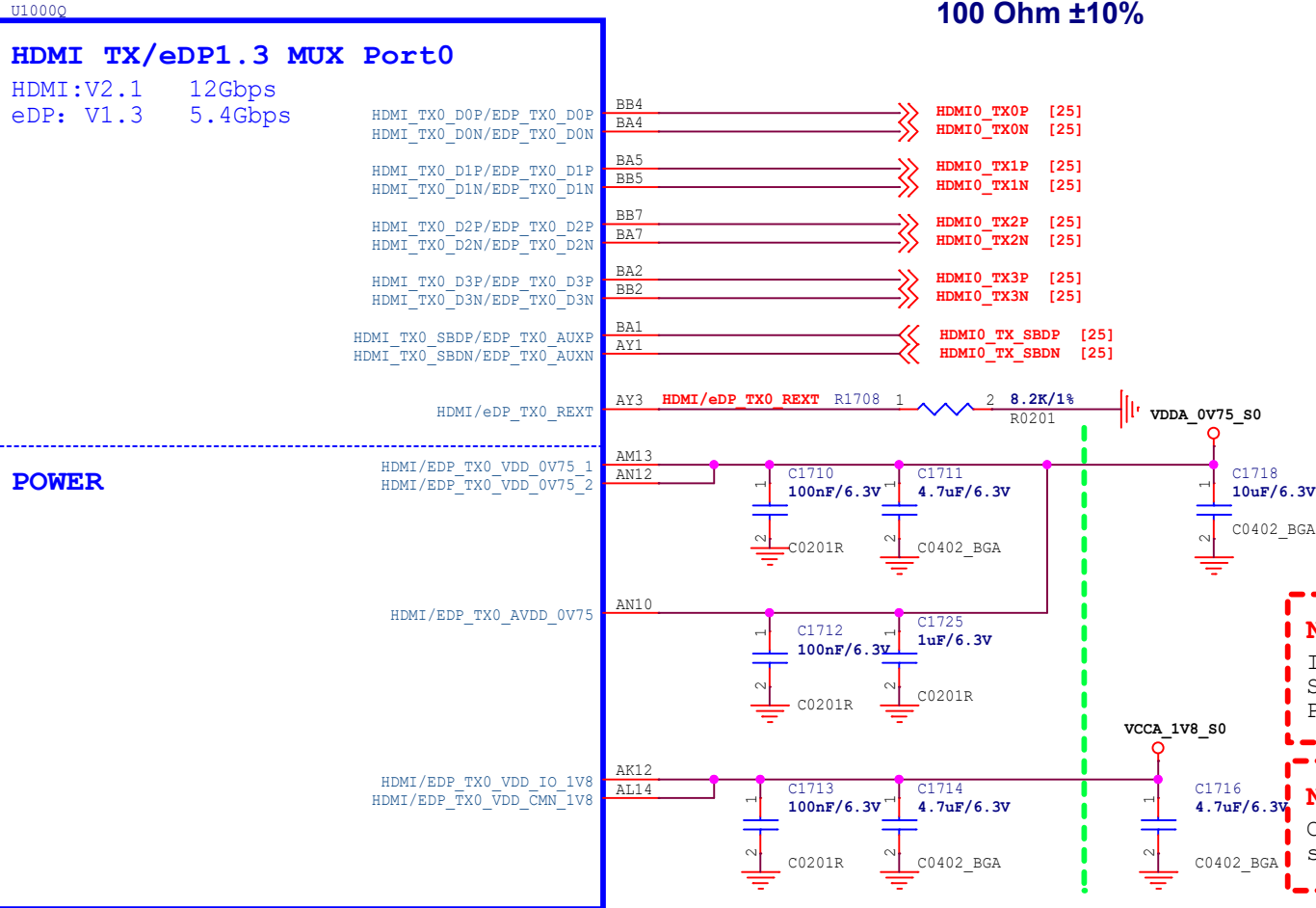
Note:
If not used:
Signal:leave floating
Power: Floating

RK3588S (HDMI2.1 TX/eDP1.3 TX)

Note:

The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

HDMI TX
100 Ohm ±10%



Note:
If not used:
Signal: leave floating
Power: Floating or tie to VSS

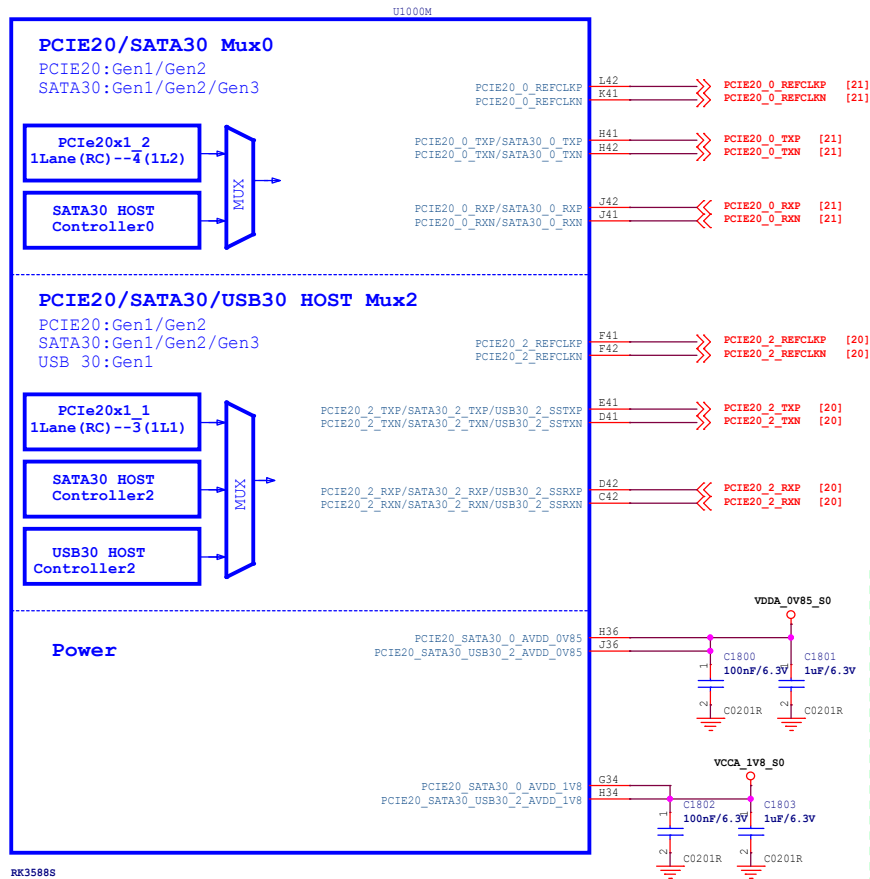
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package



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NanoPi R6S		Rev 2208
Size A4	Page Name 13.RK3588S_HDMI/eDP Interface	
Date: Tuesday, December 13, 2022	Sheet: 13/ 27	

RK3588S (PCIE20/SATA30/USB30)



CLK Differential Pair:
100 Ohm±10%
DATA Differential Pair:
PCIE20: 85 Ohm±10%
SATA30: 100 Ohm±10%
USB30: 90ohm±10%

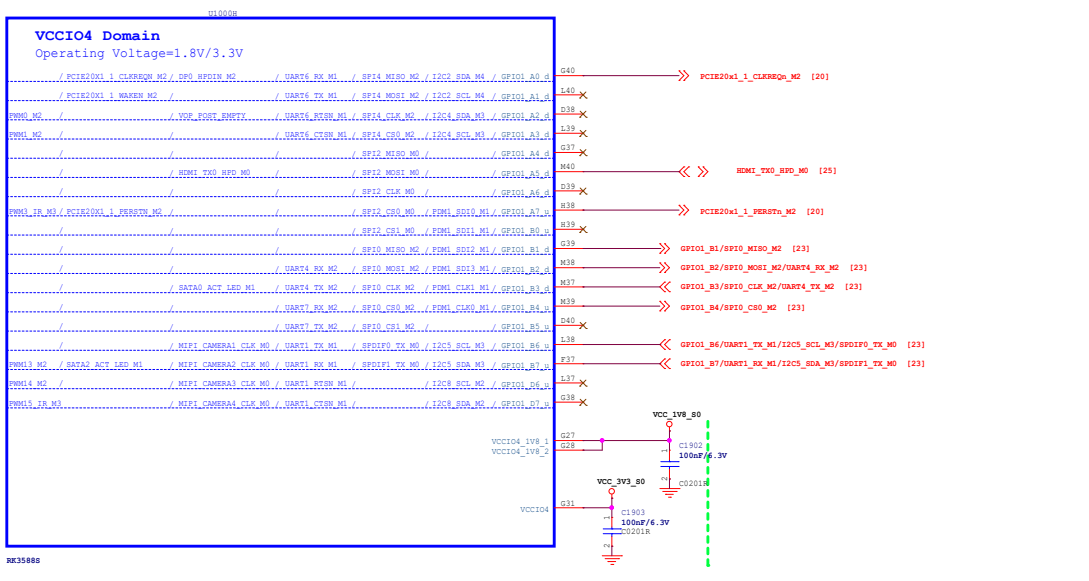
Note:
If not used:
Signal: leave floating
Power: Tie to VSS

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package

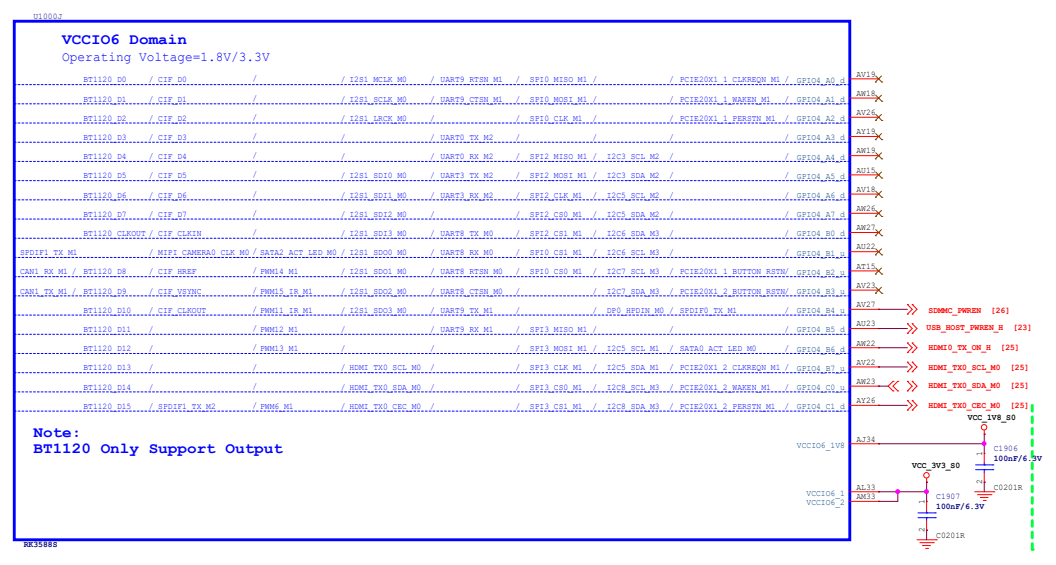
PCIE2.0 PHY

Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

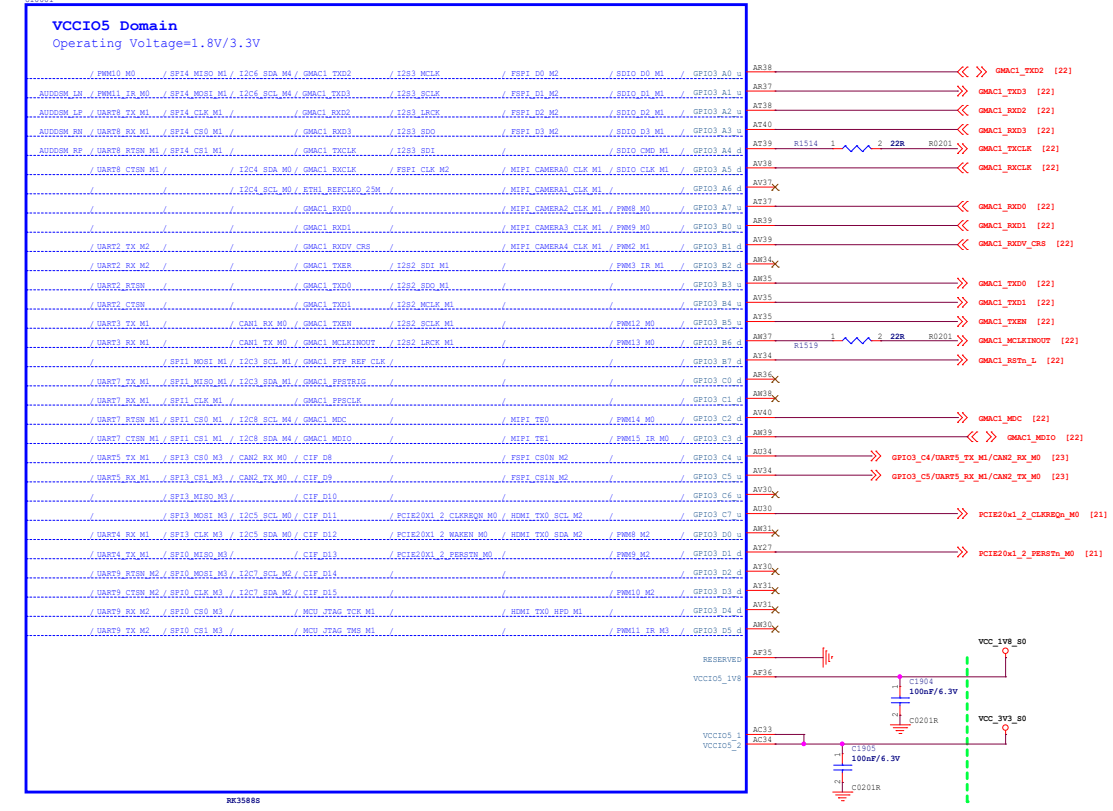
RK3588S (VCCIO4 Domain)



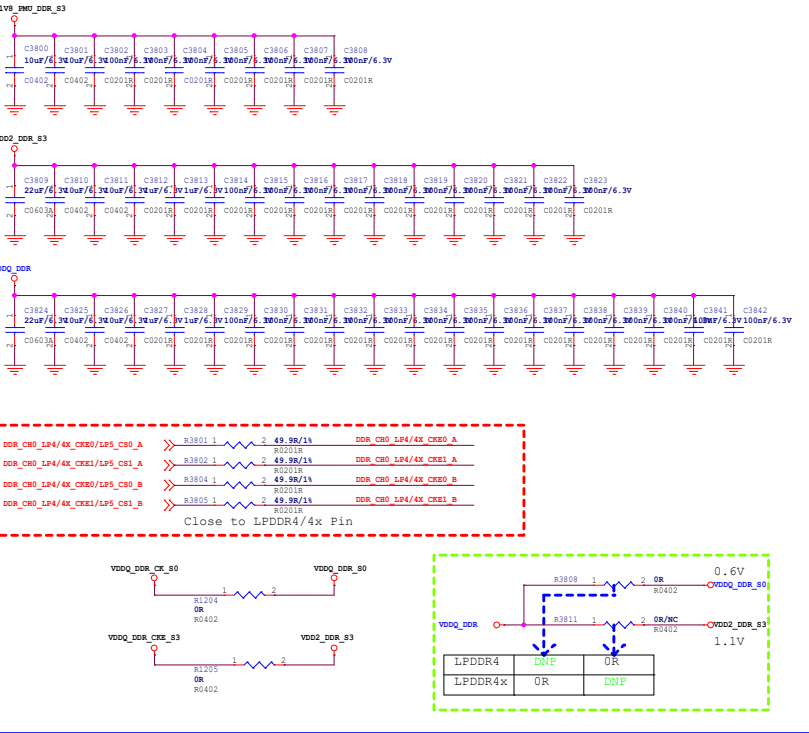
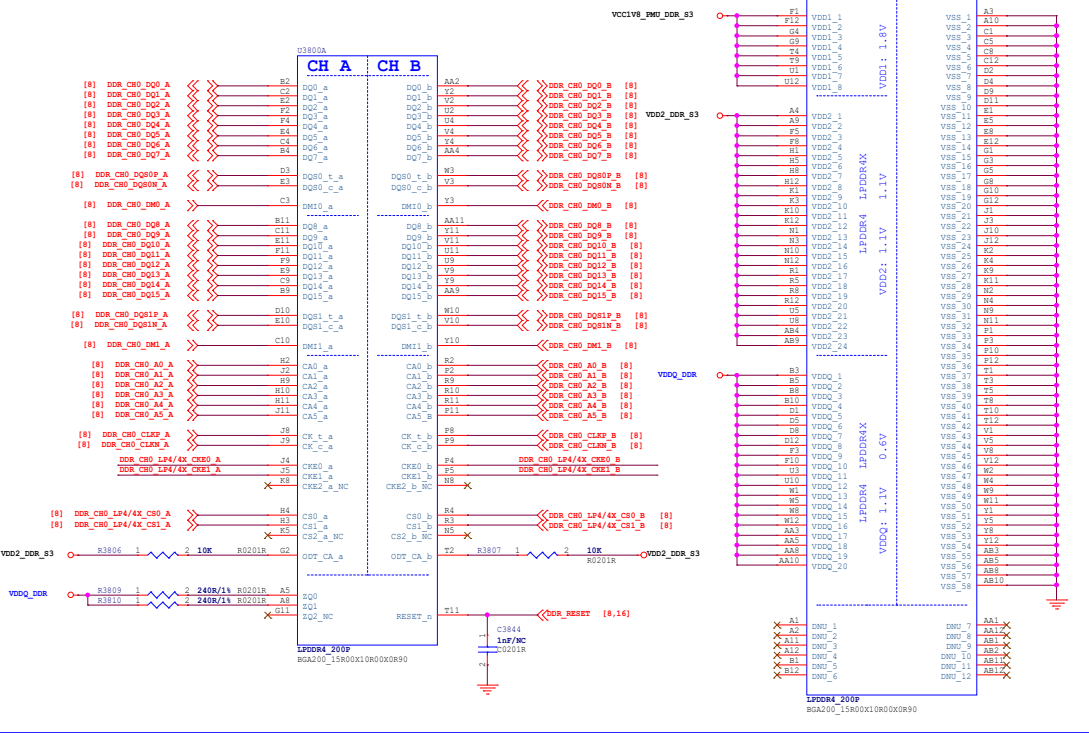
RK3588S (VCCIO6 Domain)



RK3588S (VCCIO5 Domain)



LPDDR4/4X



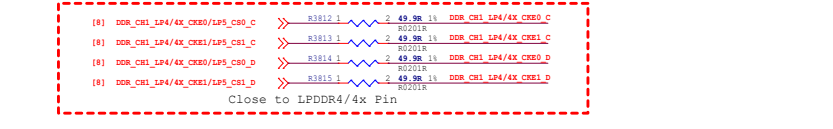
Sequence: VDD1-VDD2-VDDQ

LPDDR4 LPDDR4X

VDD1: 1.70-1.95 1.70-1.95

VDD2: 1.06-1.17 1.06-1.17

VDDQ: 1.06-1.17 0.57-0.65



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NanoPi R6S

Rev 2208

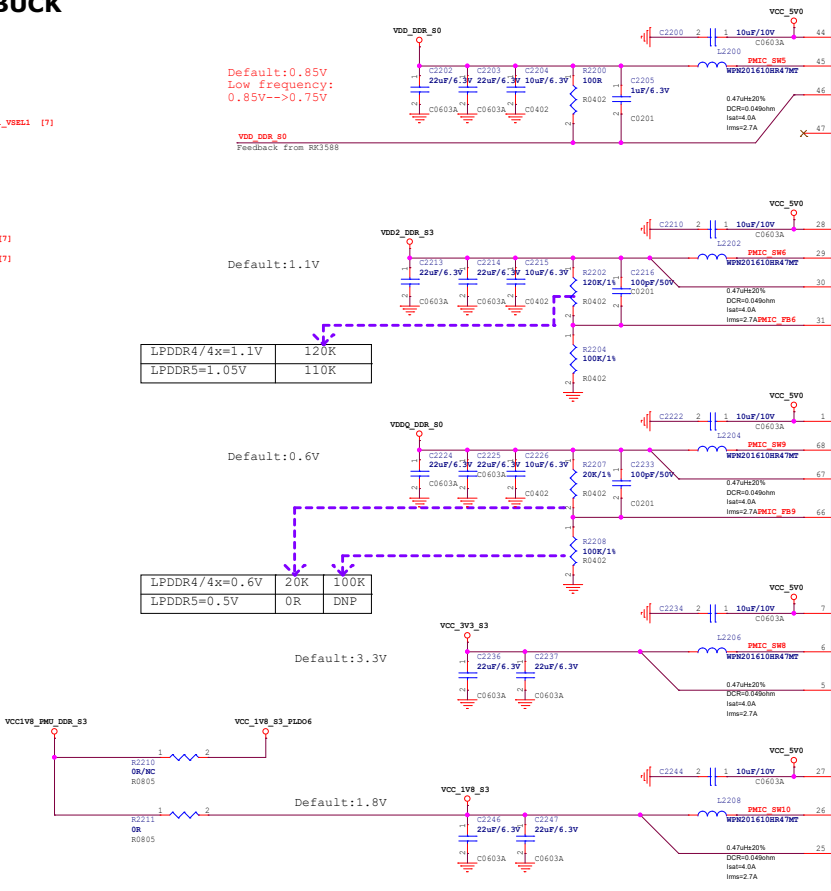
Blank Page Name

Custom 16-GRAM-LPDDR4X_200P_2x32bit

Date: Tuesday, December 13, 2022 Sheet: 16 / 21

PMIC RK806-1 BUCK

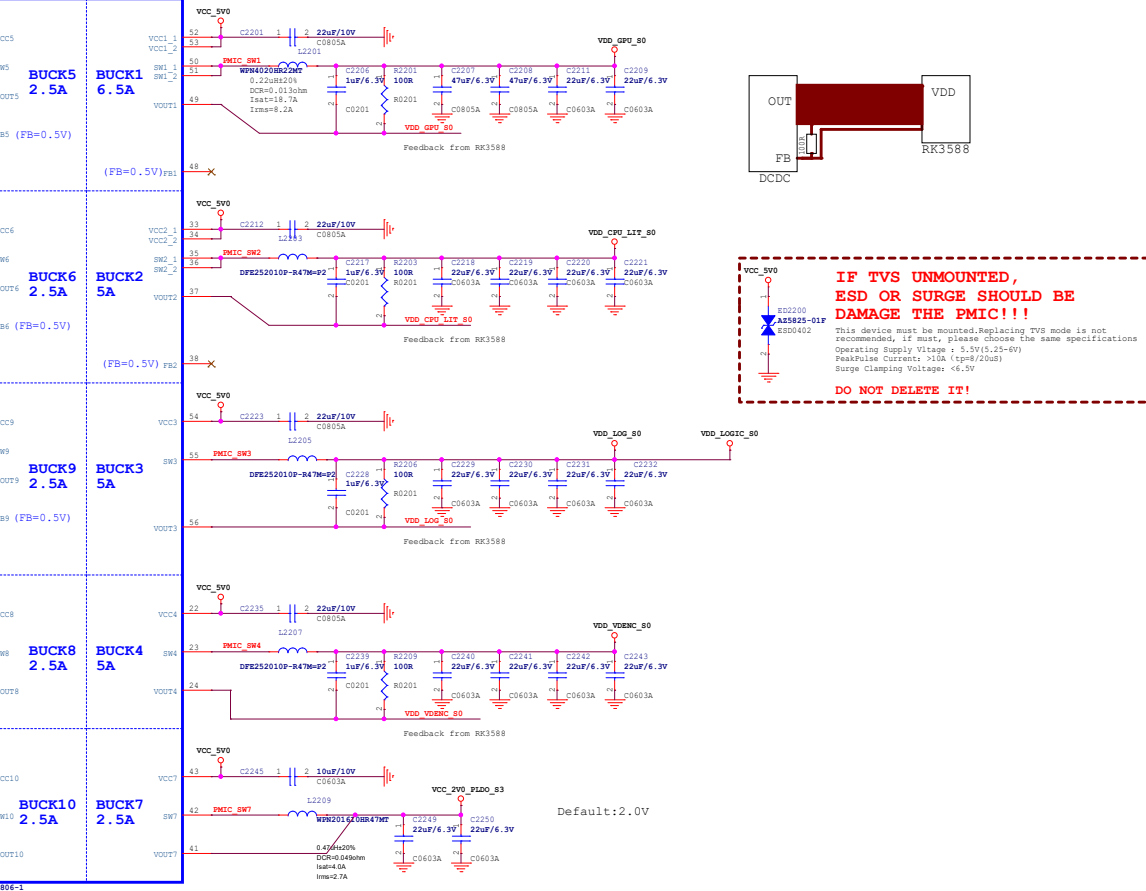
- PMIC_SPI_CS [7]
- PMIC_SPI_MOSI [7]
- PMIC_SPI_CLK [7]
- SLEEP1_RESET1_DEVOPFI_VSEL1 [7]
- PMIC_INT_L [7]
- RESET_L [7]
- PMIC_EXT_EN_OUT [18]
- PMIC_PWR_CTRL3 [7]
- PMIC_PWR_CTRL3 [7]



LPDDR4/4x=1.1V	120K
LPDDR5=1.05V	110K

LPDDR4/4x=0.6V	20K	100K
LPDDR5=0.5V	0R	DNP

Default: 1.8V	
---------------	--

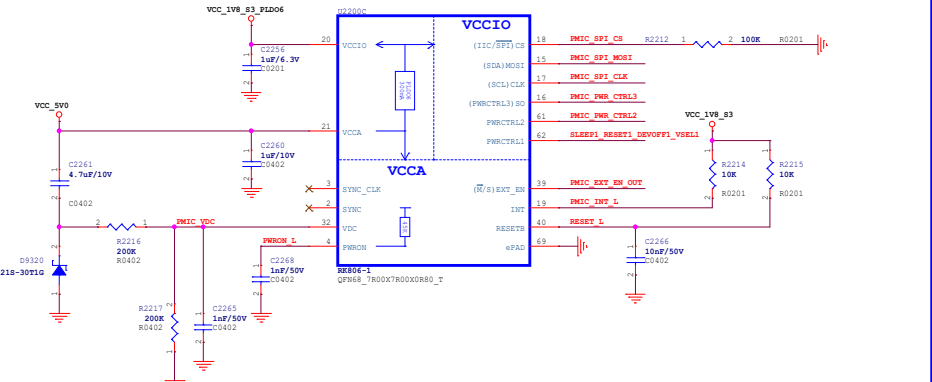


IF TVS UNMOUNTED, ESD OR SURGE SHOULD BE DAMAGE THE PMIC!!!

This device must be mounted. Replacing TVS mode is not recommended, if must, please choose the same specifications
 Operating Supply Voltage: +5.5V/5.25-6V
 Peak Pulse Current: >1A (tps/20us)
 Surge Clamping Voltage: <6.5V

DO NOT DELETE IT!

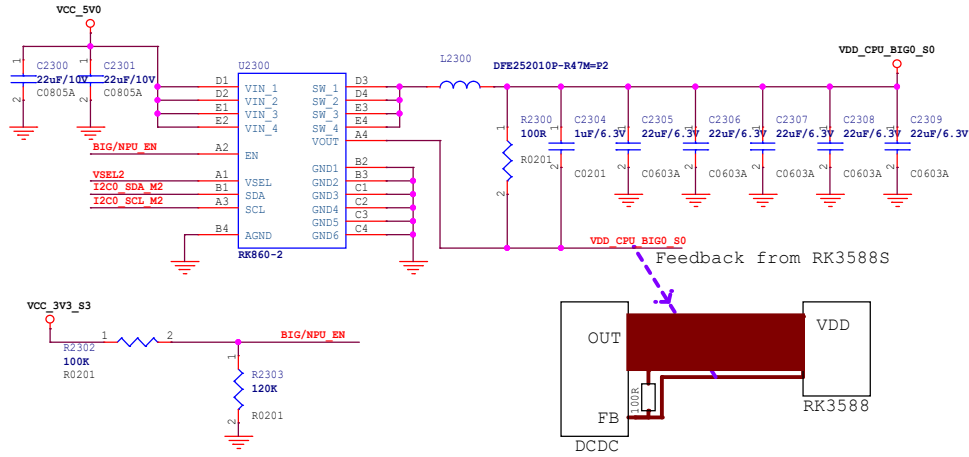
PMIC RK806-1 Management



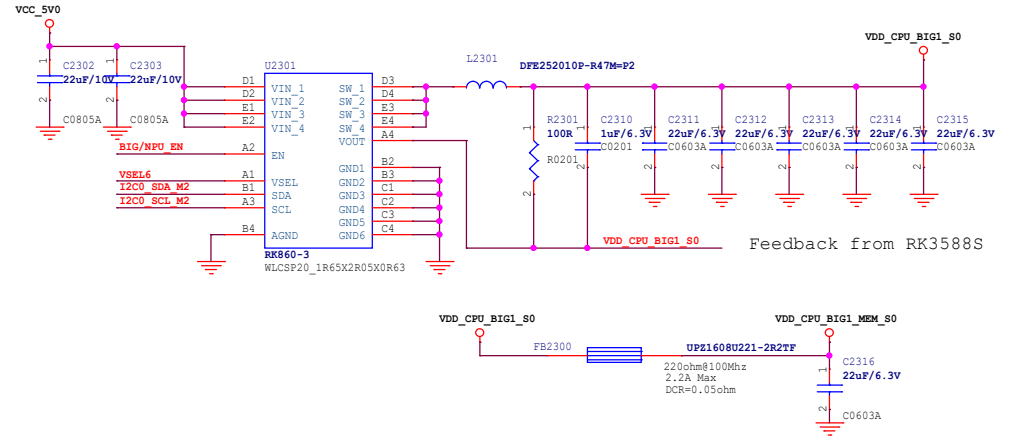
PMIC RK806-1 LDO



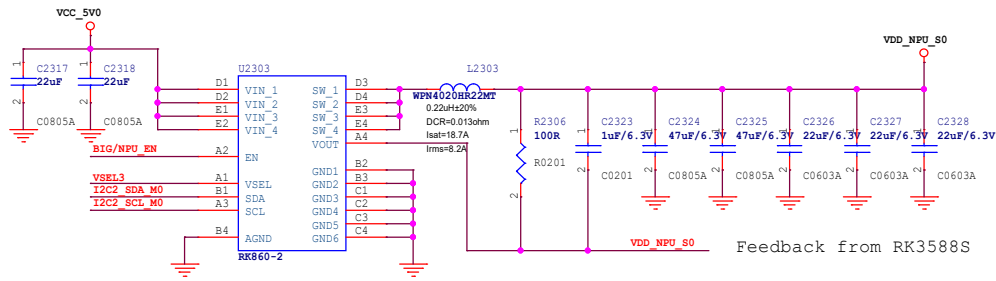
VDD_CPU_BIG0



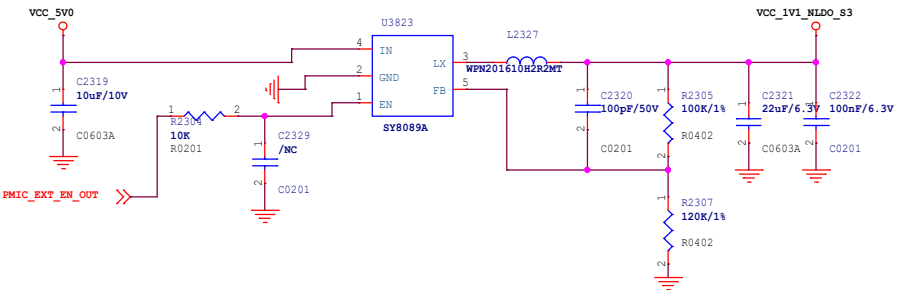
VDD_CPU_BIG1



VDD_NPU

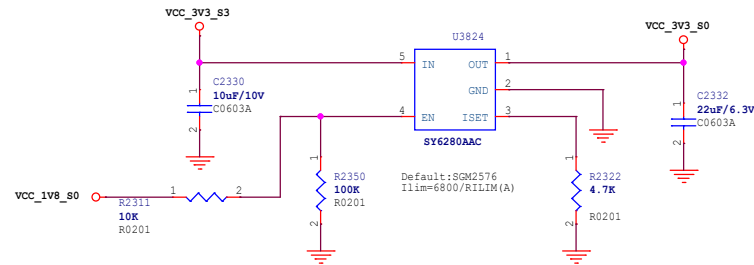


VCC_1V1_NLDO_S3

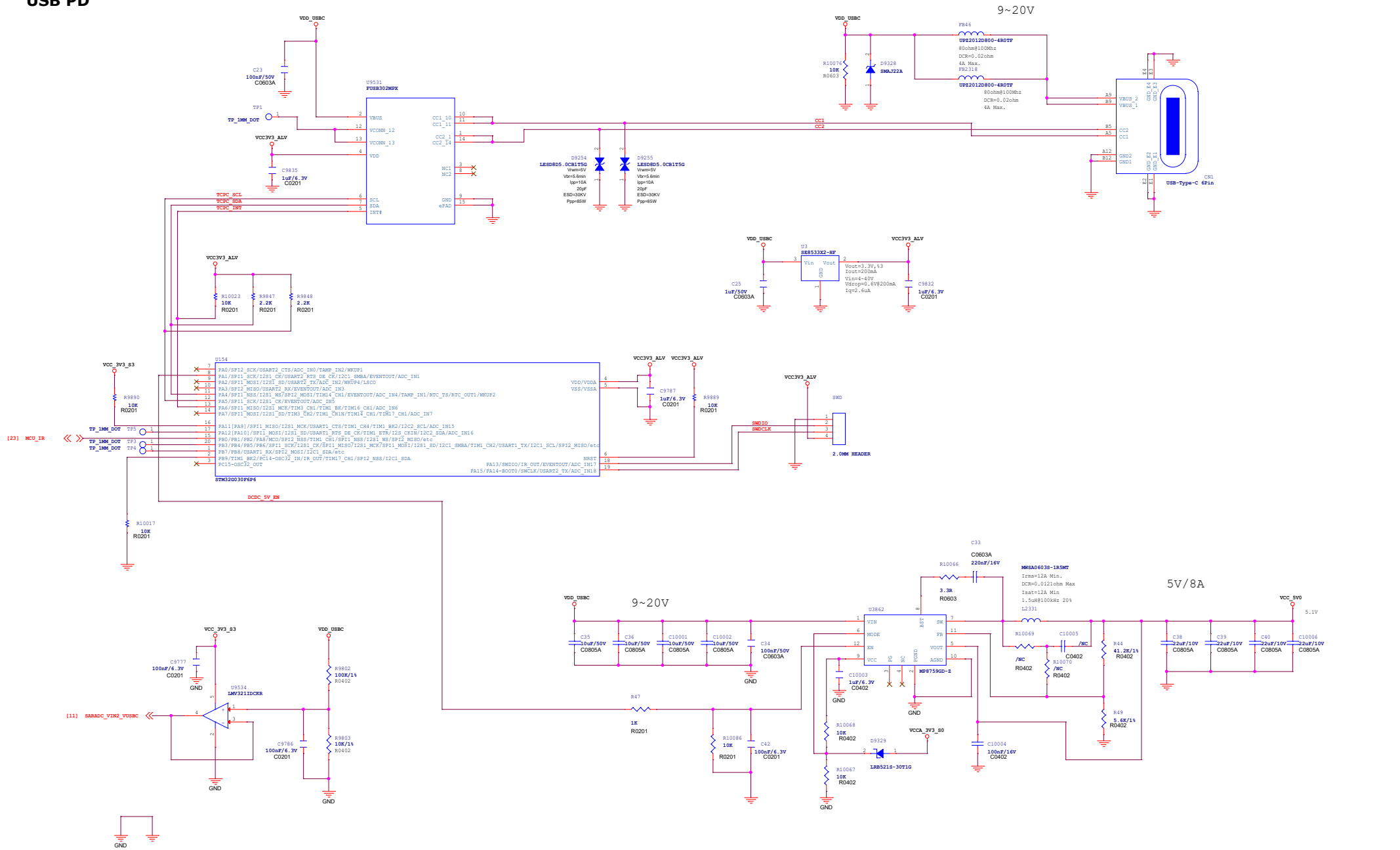


I2C0_SCL_M2 (7)
 I2C0_SDA_M2 (7)
 I2C2_SCL_M0 (7)
 I2C2_SDA_M0 (7)

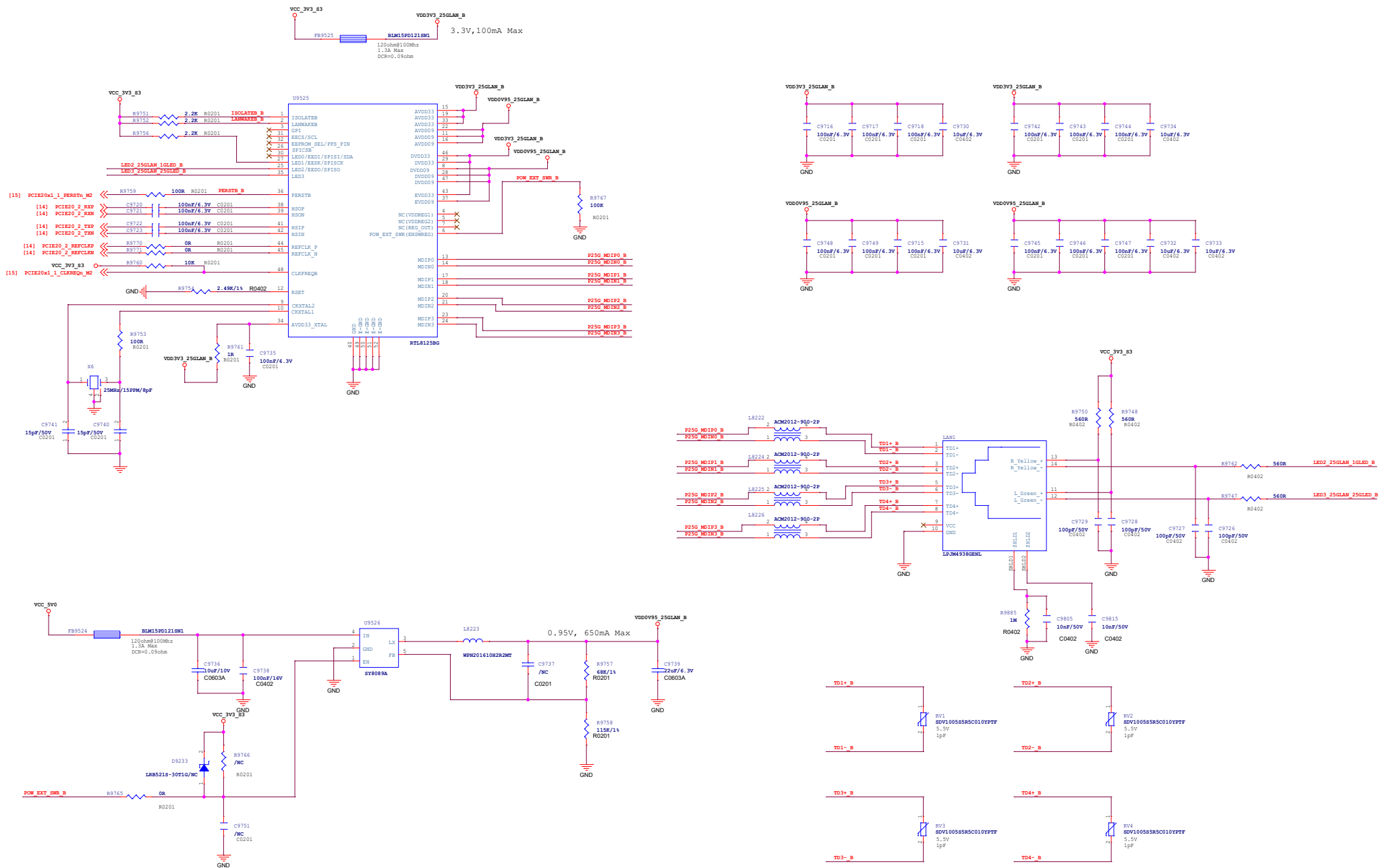
VSEL2 (7)
 VSEL3 (7)
 VSEL6 (7)



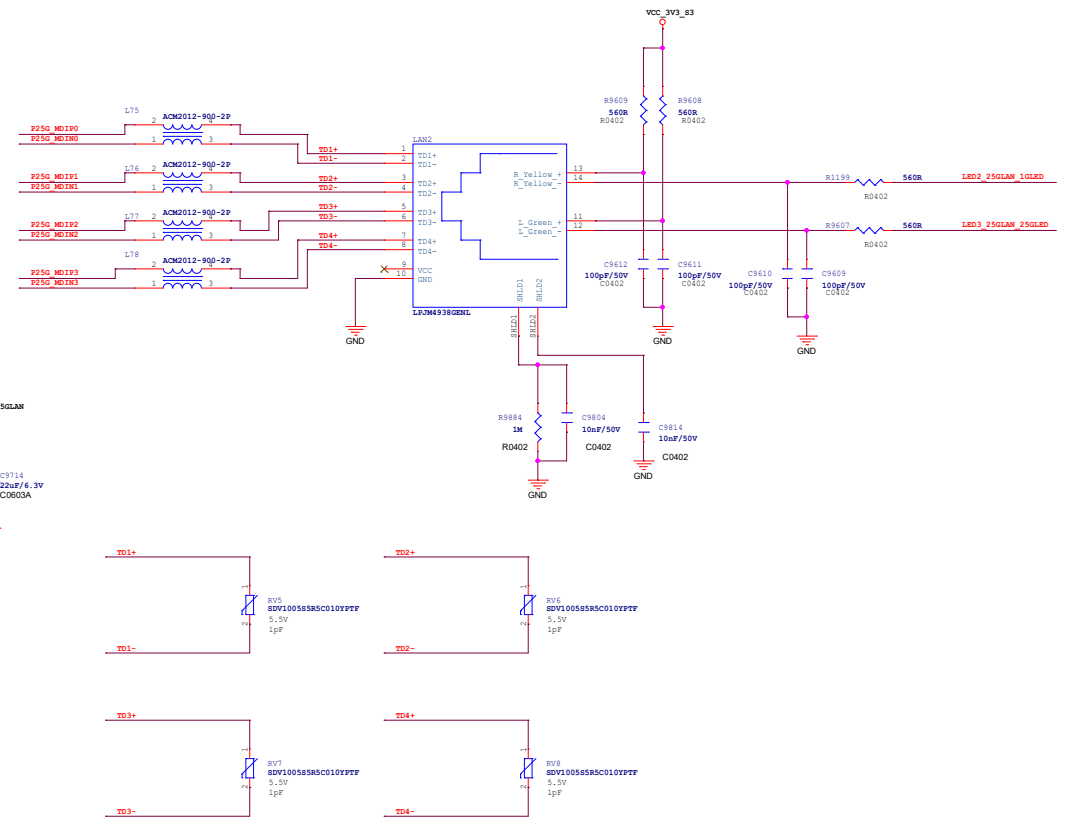
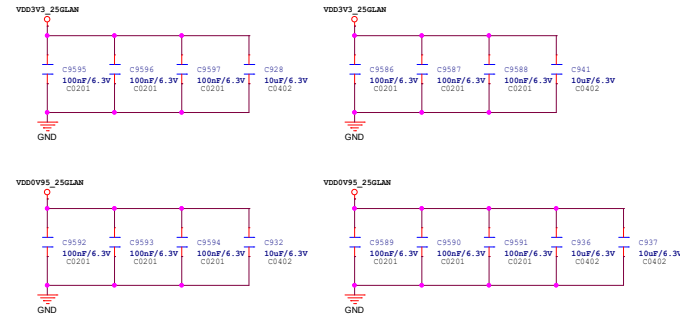
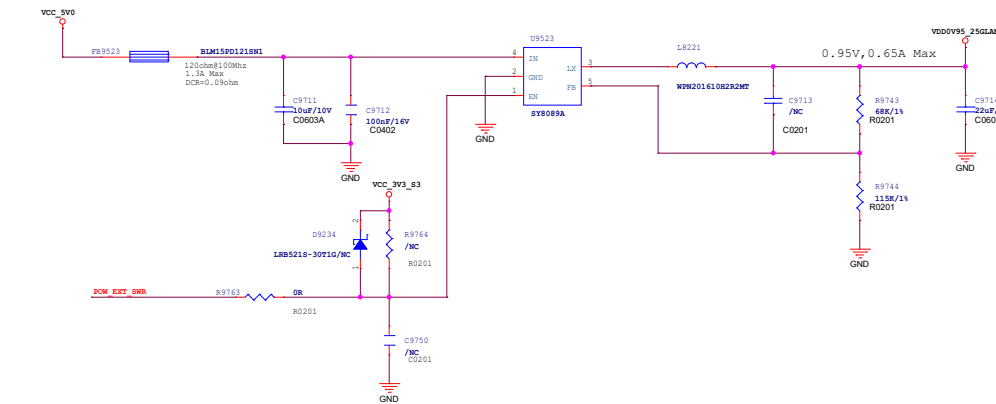
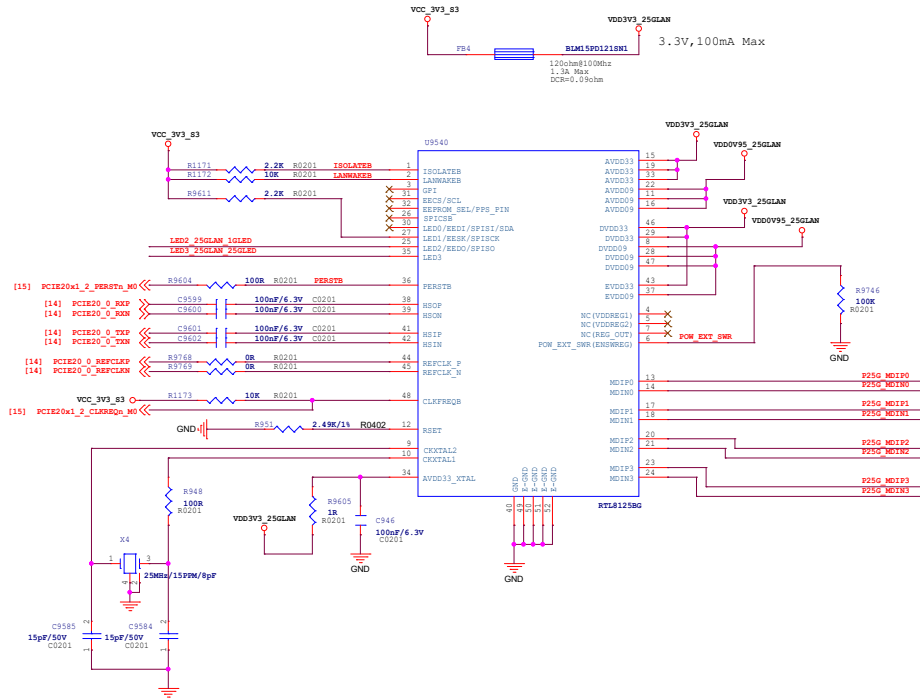
USB PD



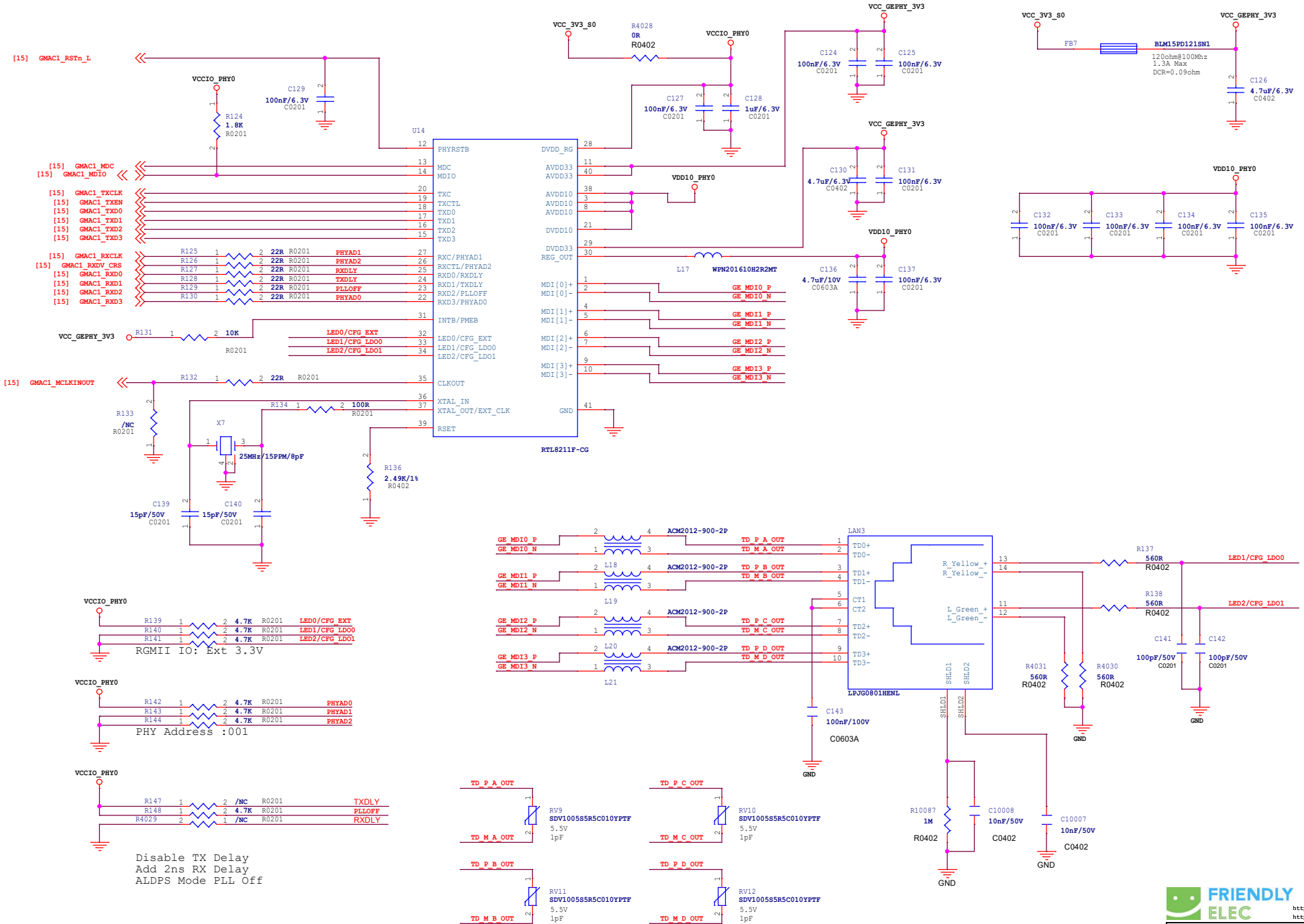
2.5Gbps Ethernet



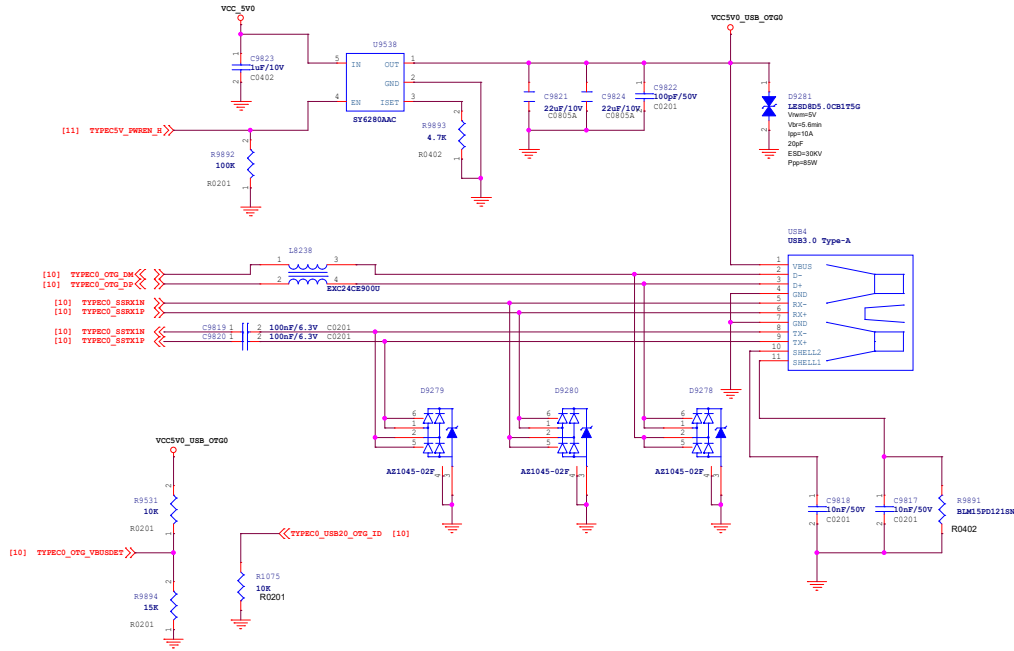
2.5Gbps Ethernet



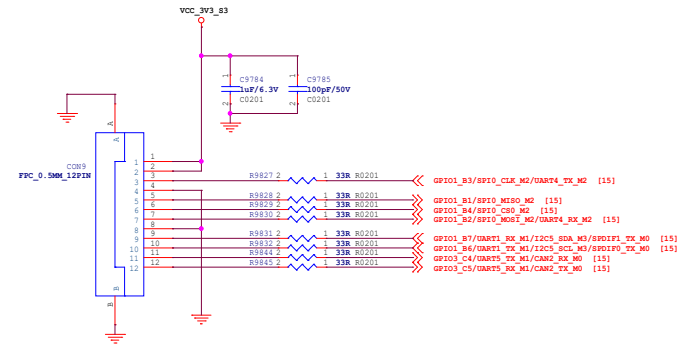
1G Ethernet



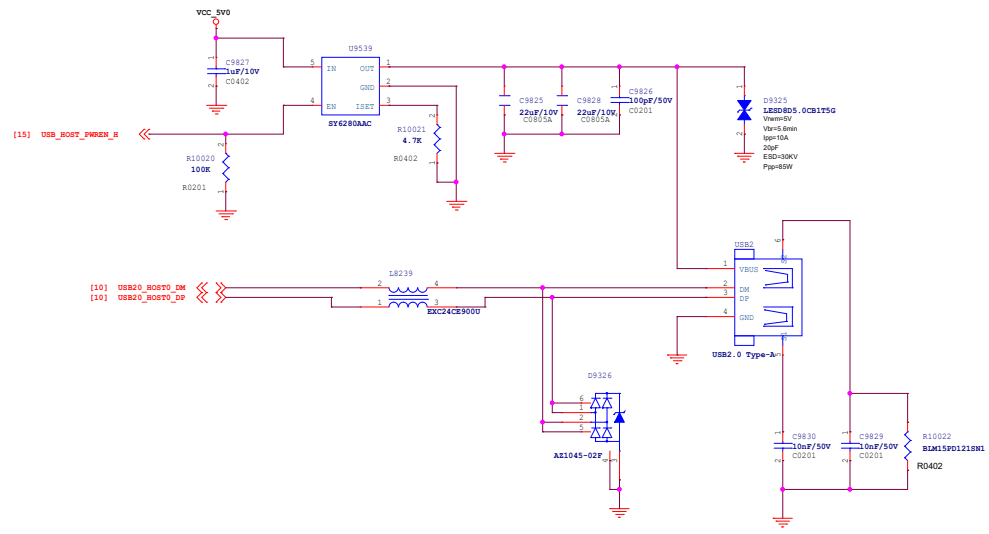
USB 3.0/ADB/MASK



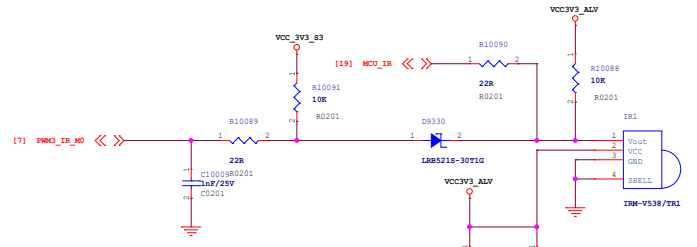
GPIO



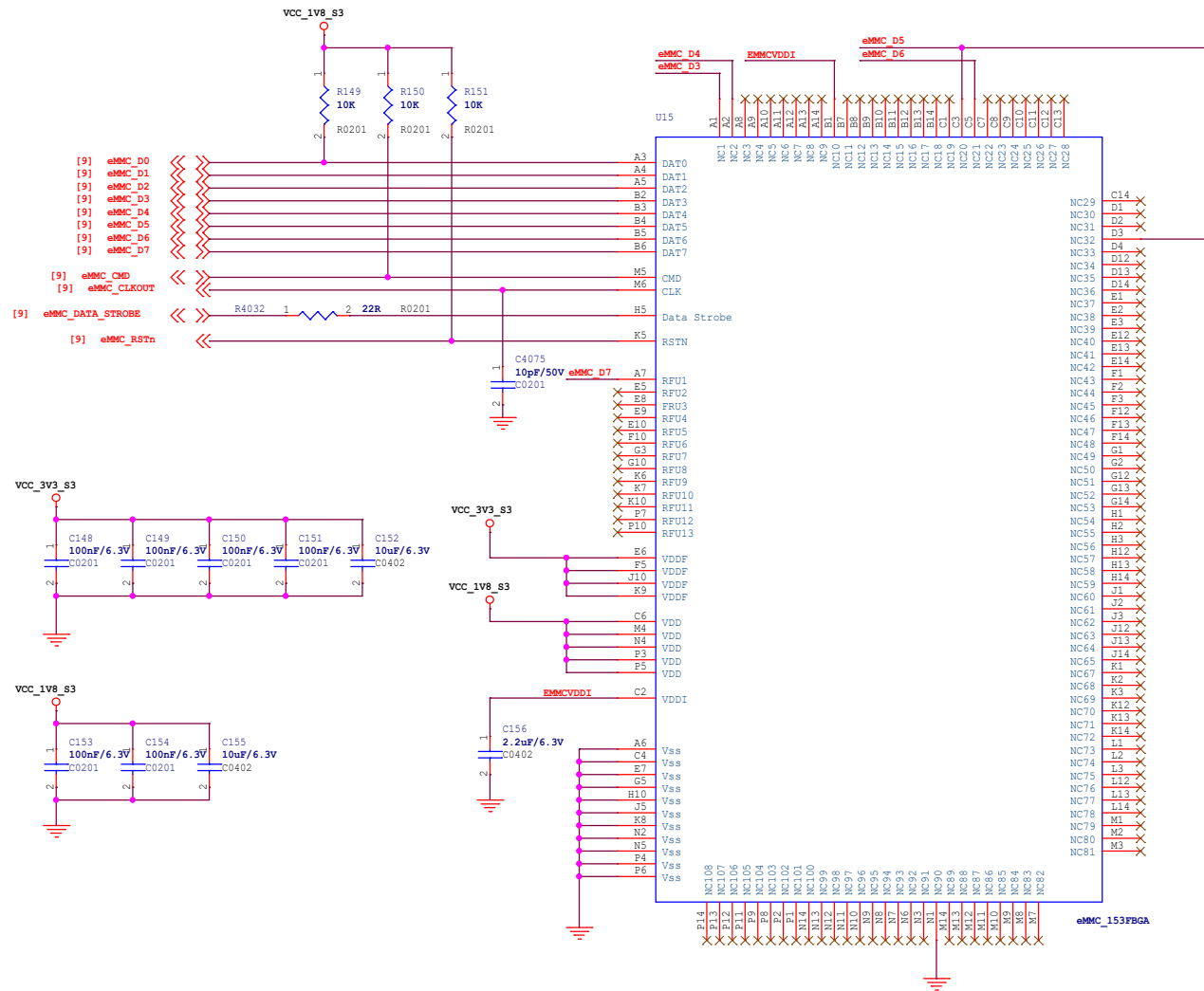
USB 2.0



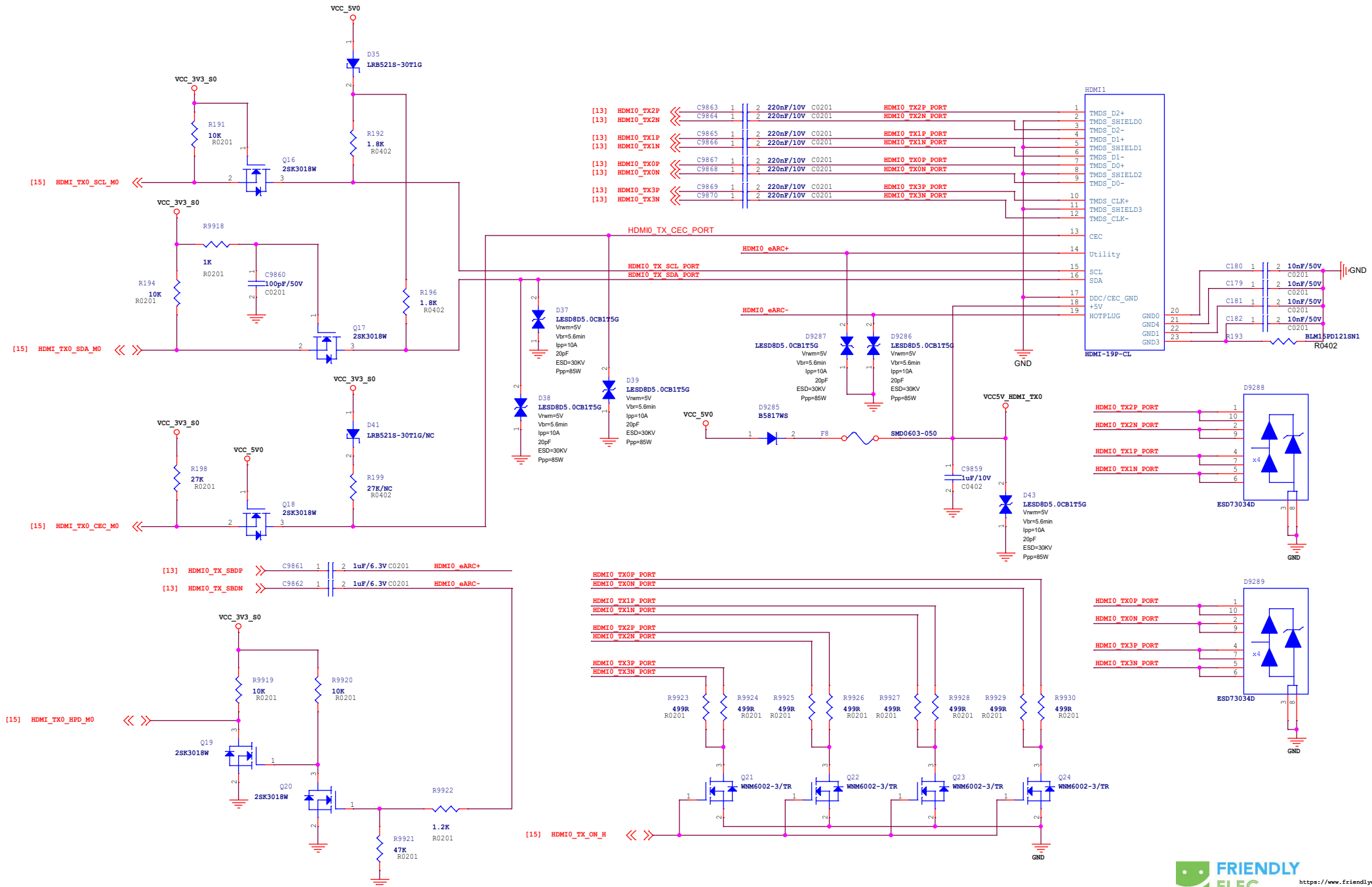
IR



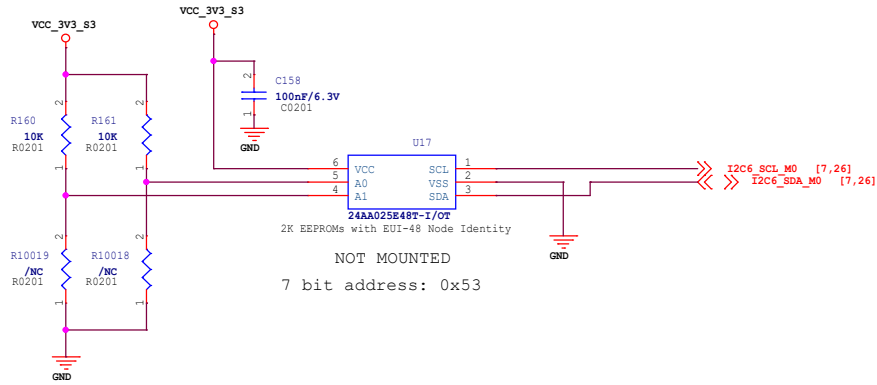
eMMC



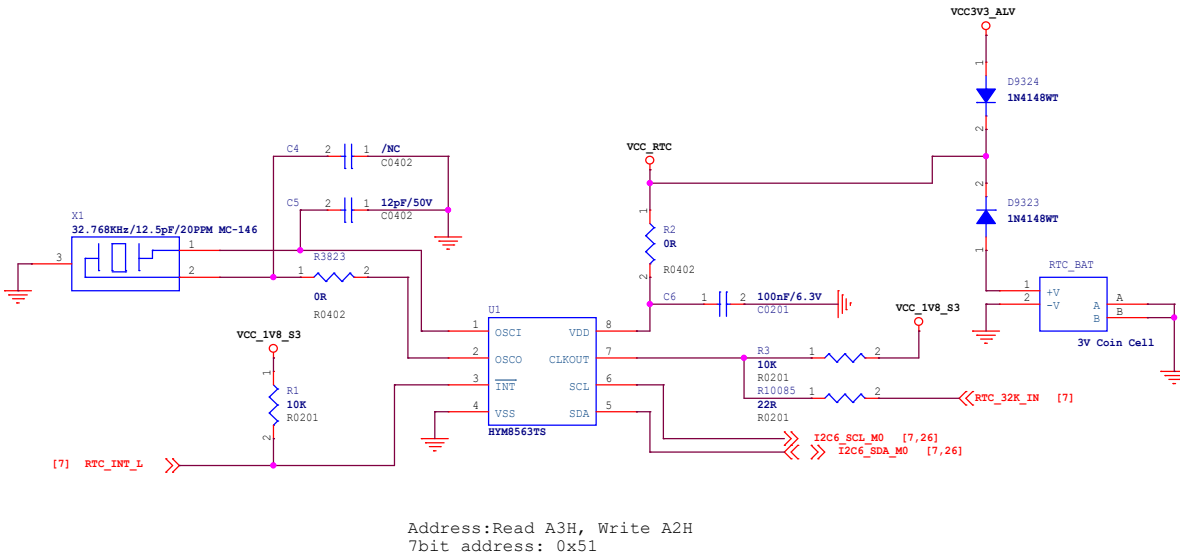
HDMI TX0



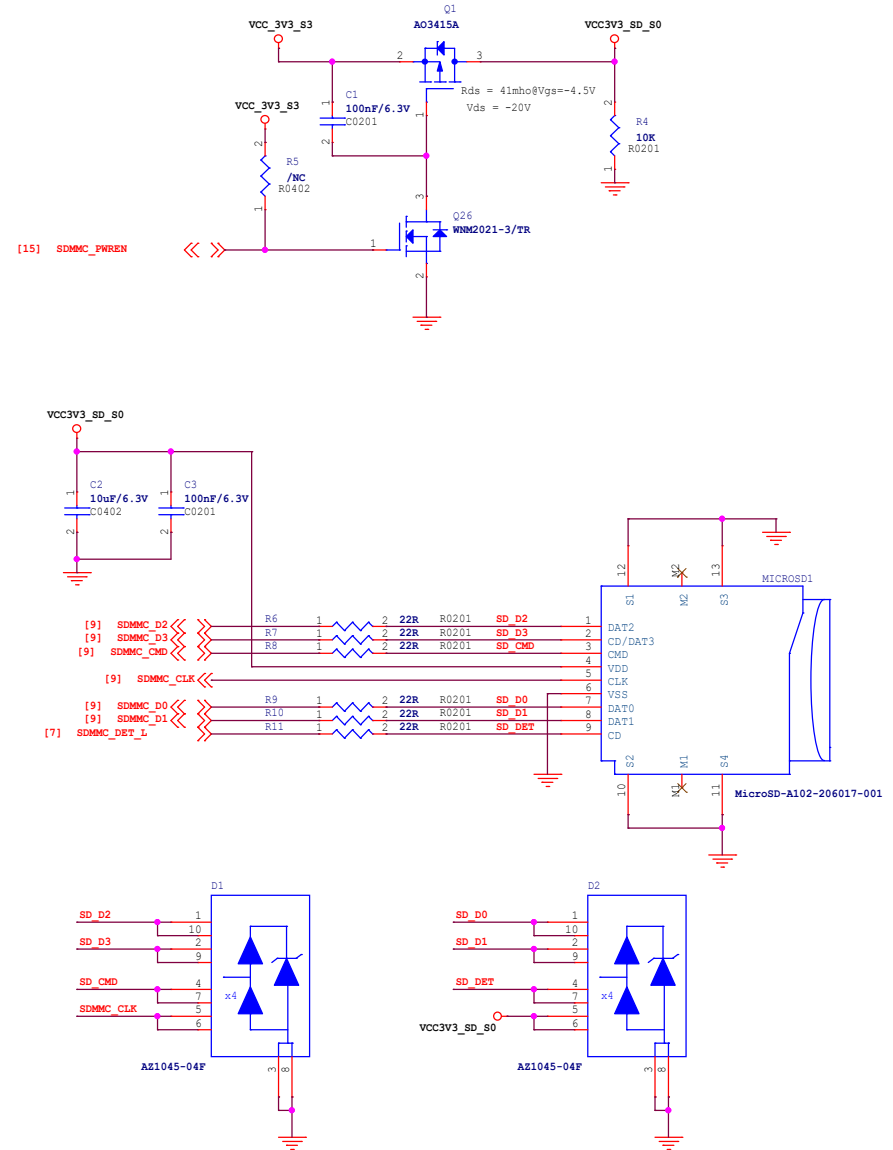
EUI-48 Node Identity



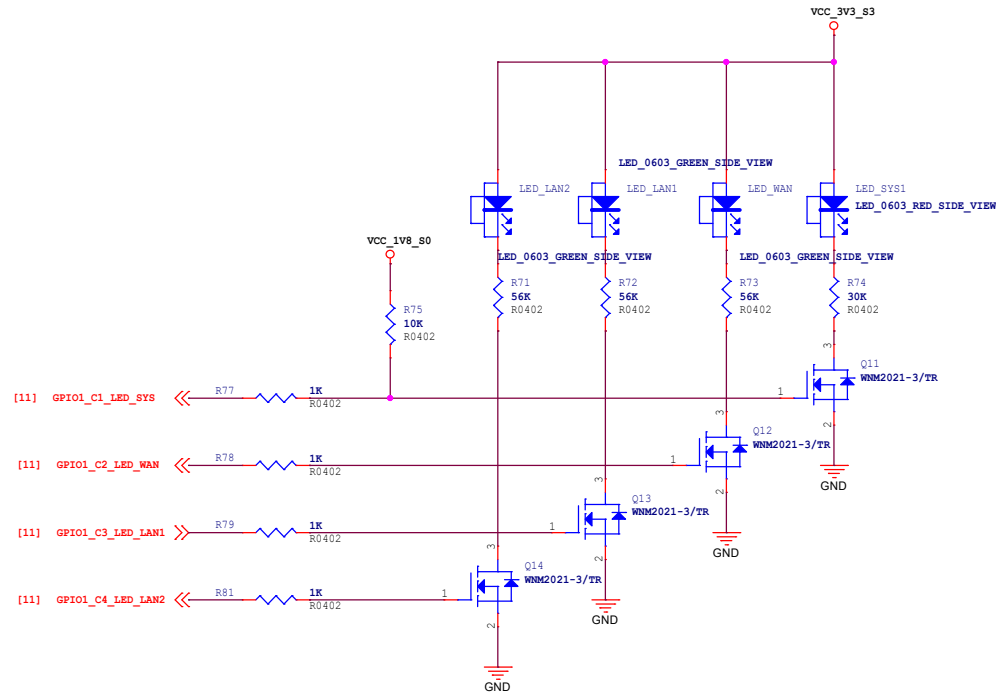
RTC



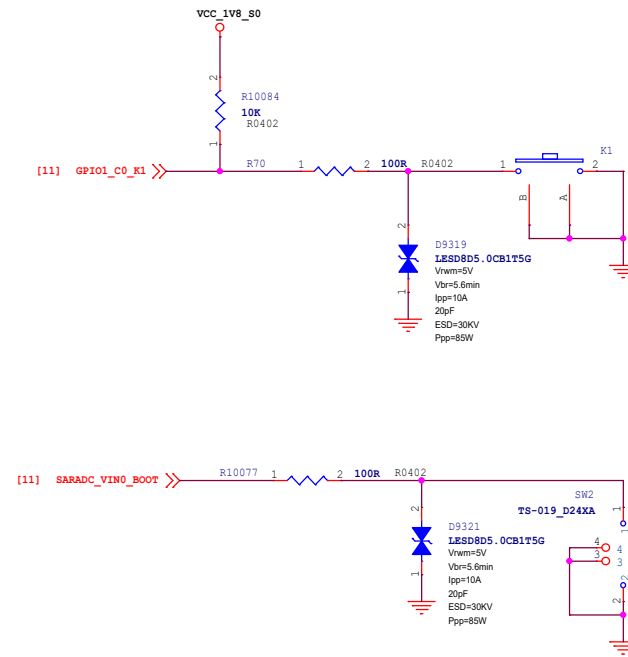
microSD



LED



Button



Debug UART

