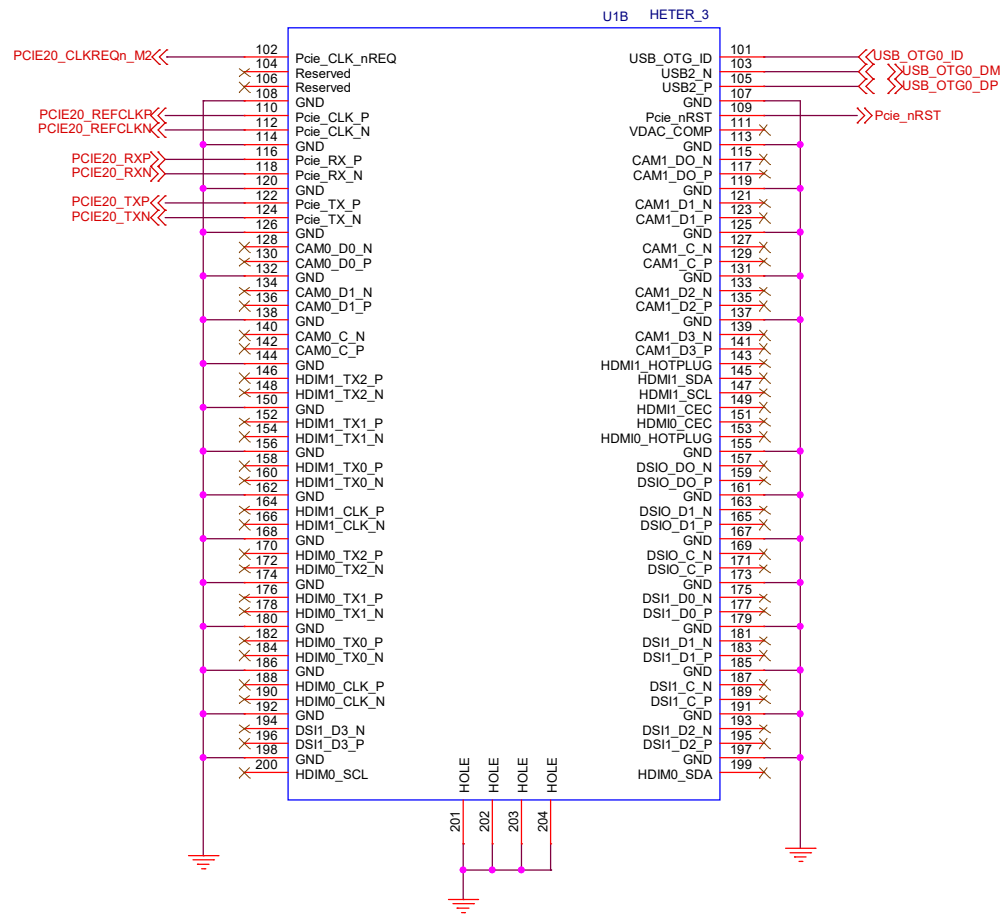
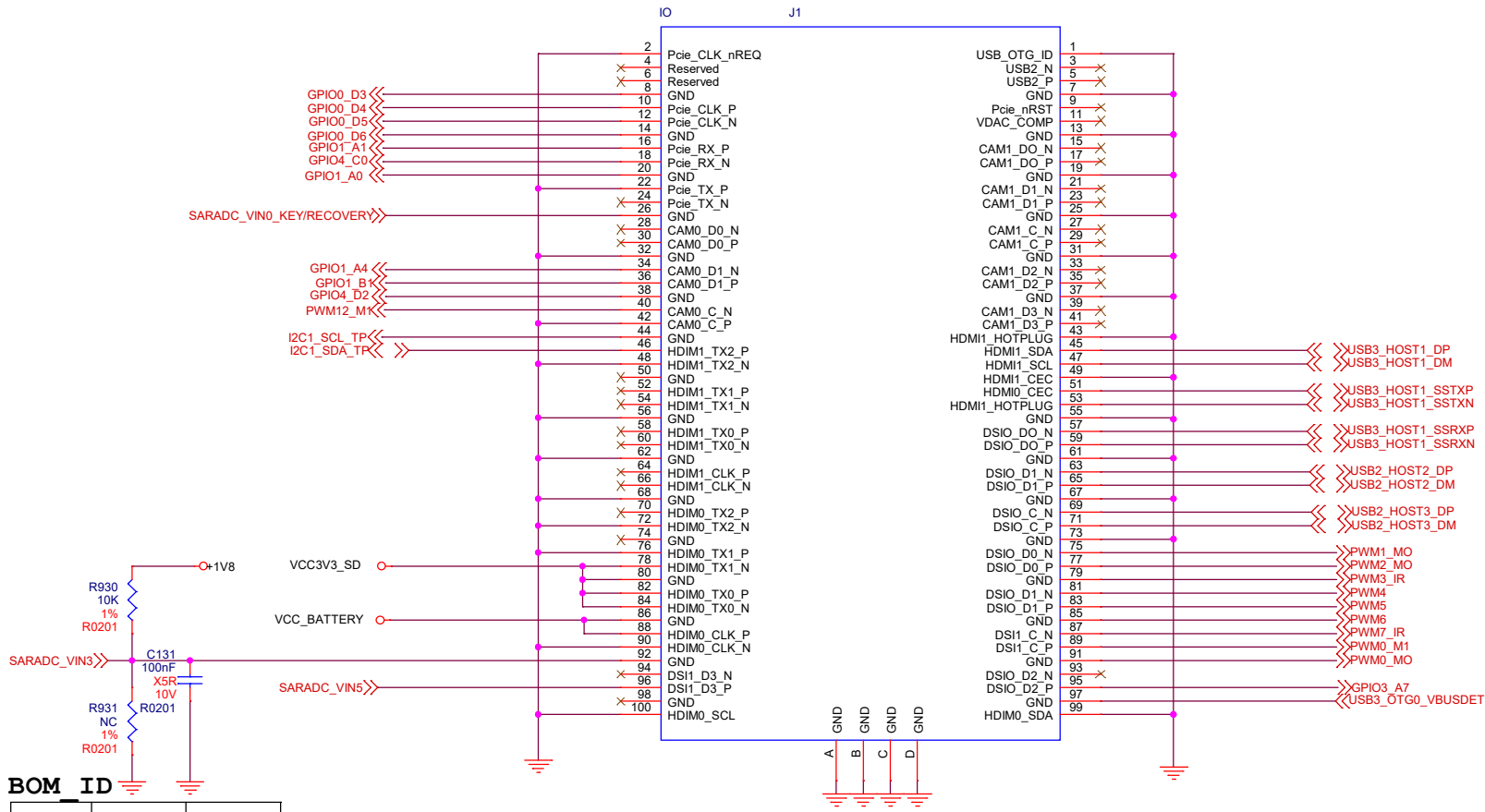
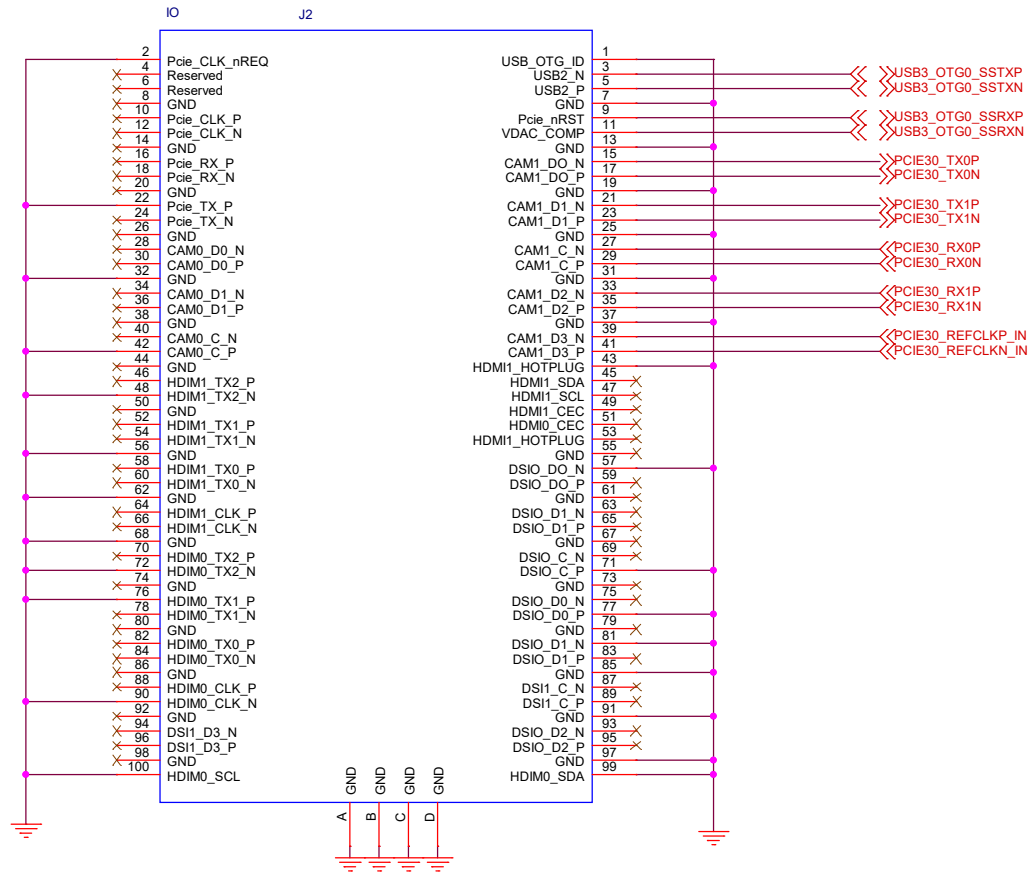


Size	Title: <b>Radxa_E25</b>	REV
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Date: <b>Friday, October 28, 2022</b>	Sheet <b>1</b> of <b>11</b>	

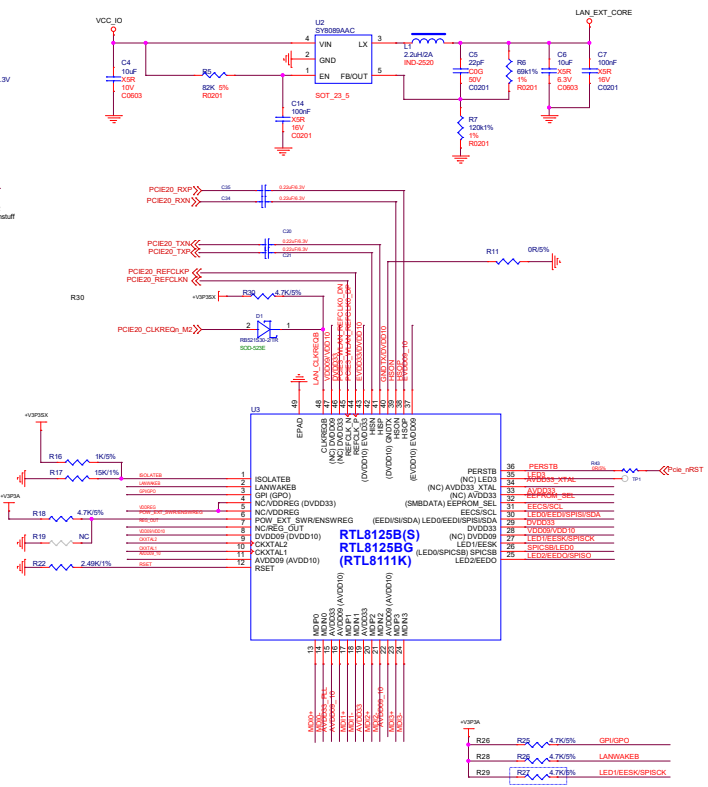
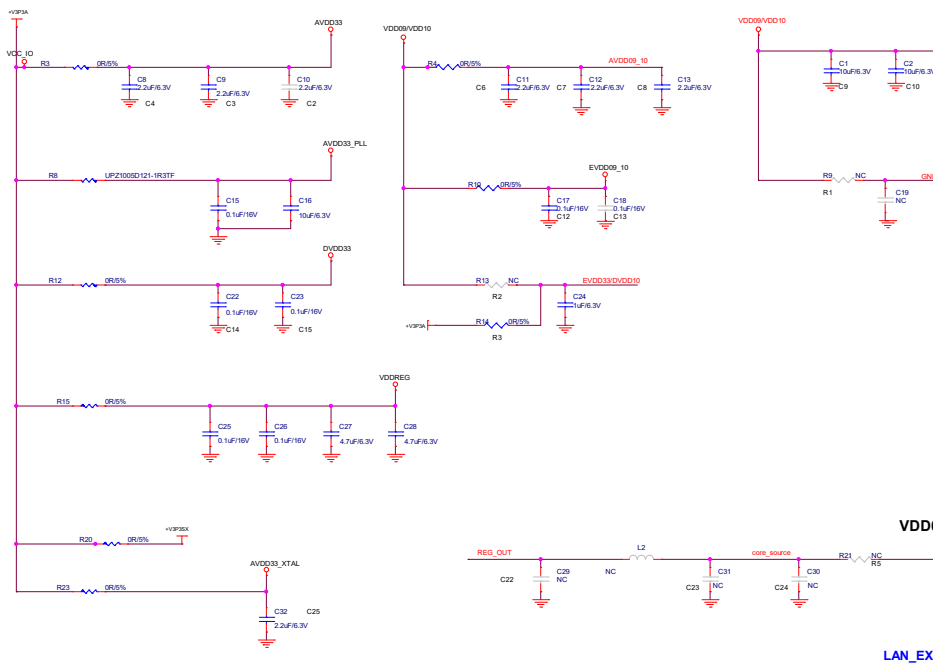


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Date: <b>Friday, October 28, 2022</b>	Sheet <b>2</b> of <b>11</b>	

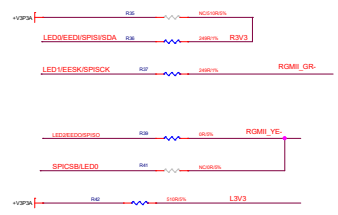
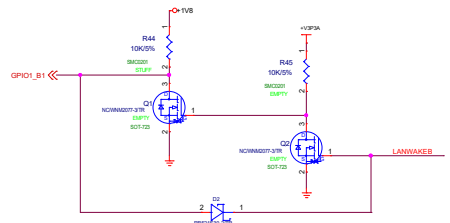
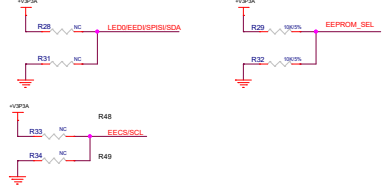




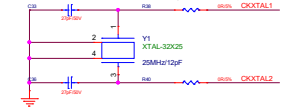
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Date: Friday, October 28, 2022	Sheet 4 of 11	



For RTL8125B(S)\_BG & RTL8111K

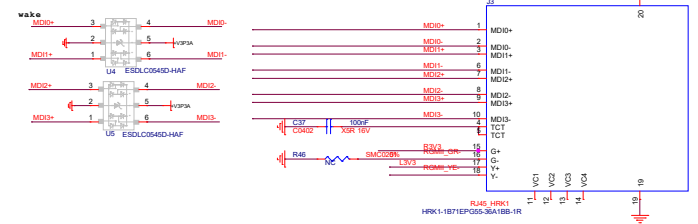


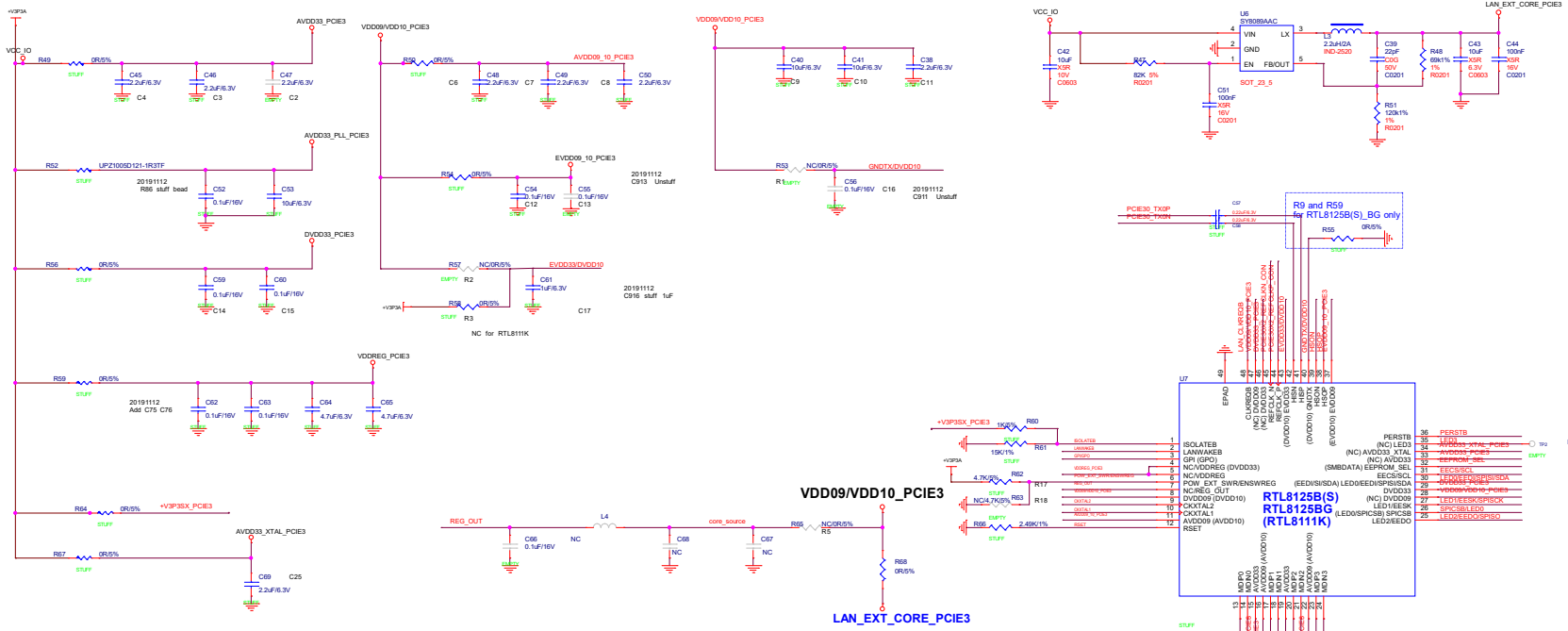
Clock Source



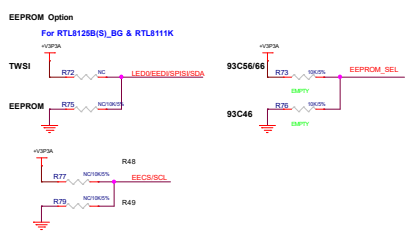
2.5G

TVS for Surge Improvement

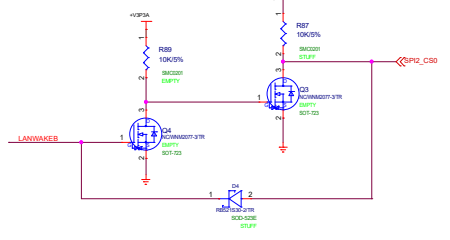
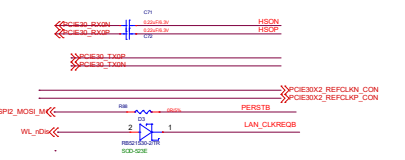
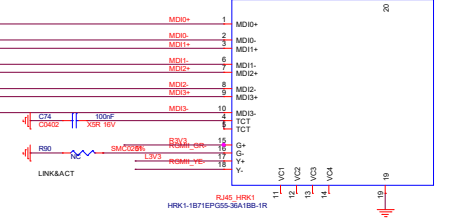


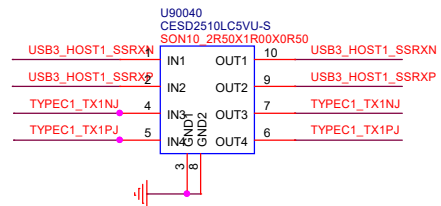
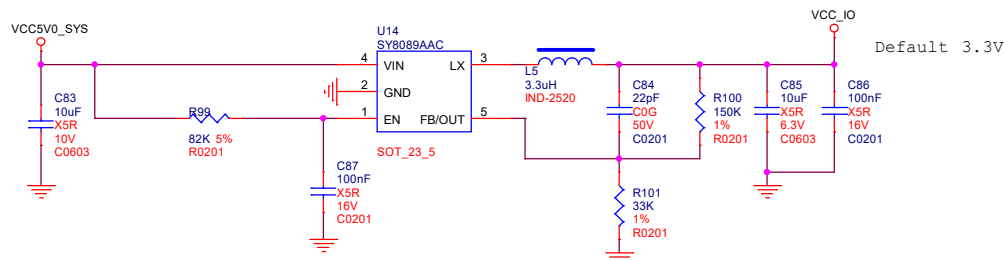
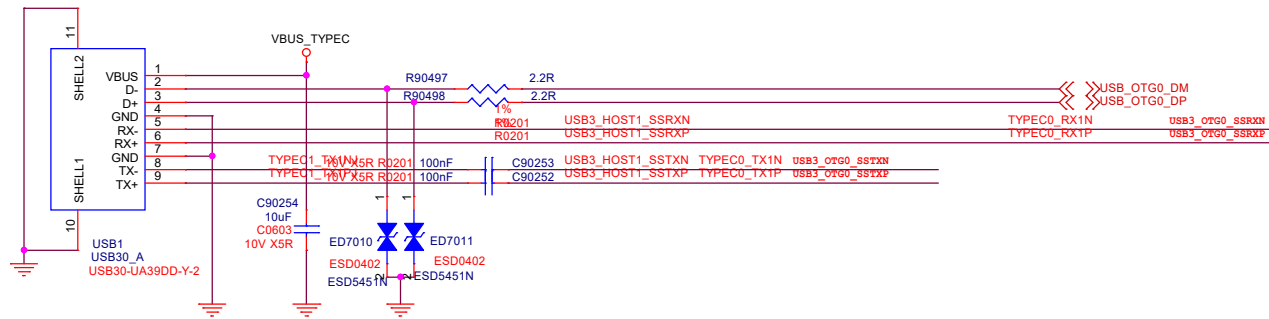
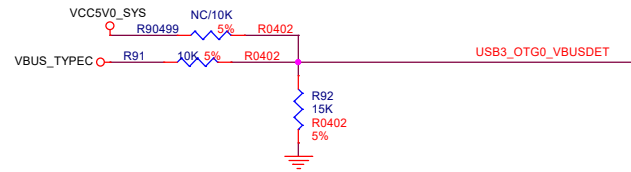
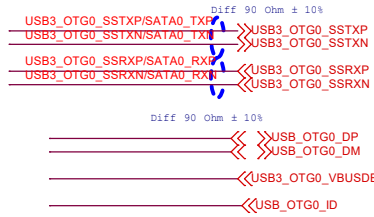


**TVS for Surge Improvement**

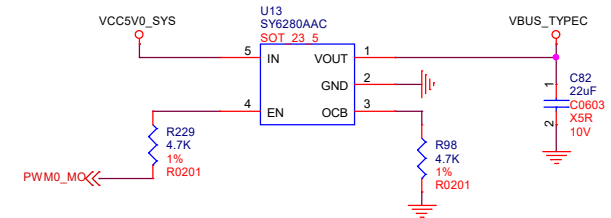
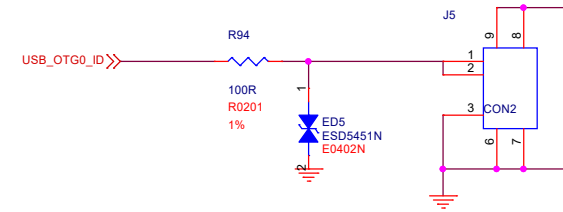


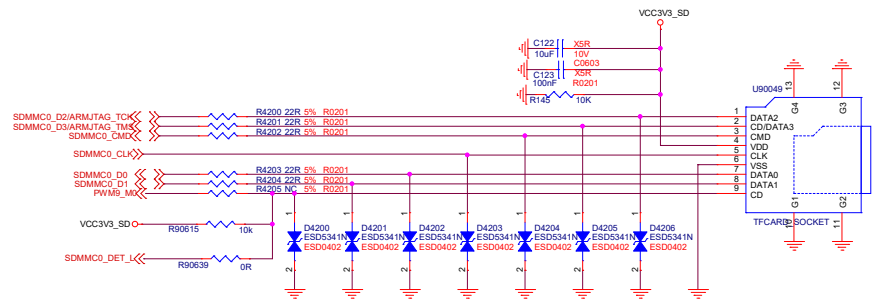
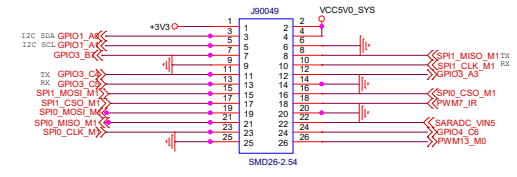
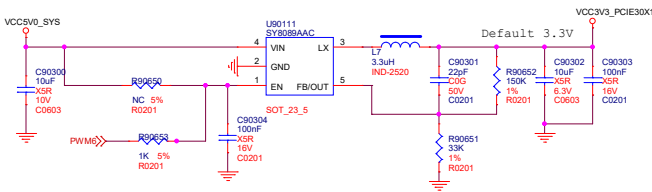
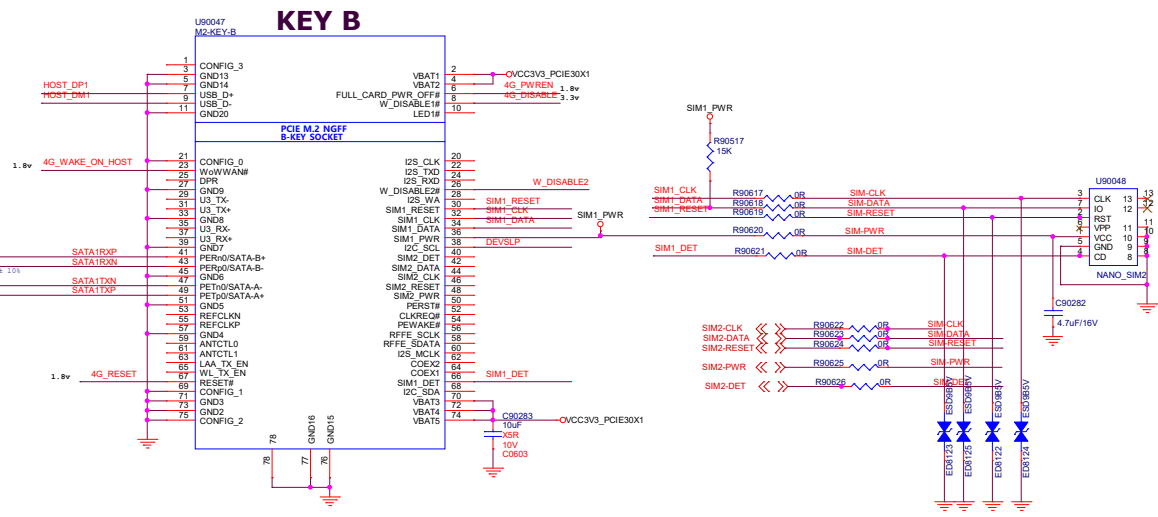
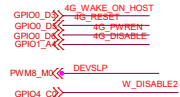
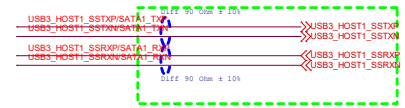
**2.5G**





## DEVICE/HOST

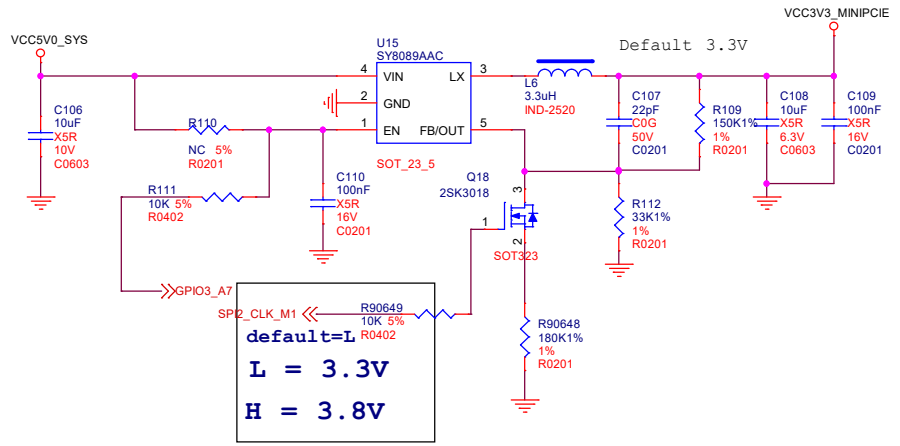
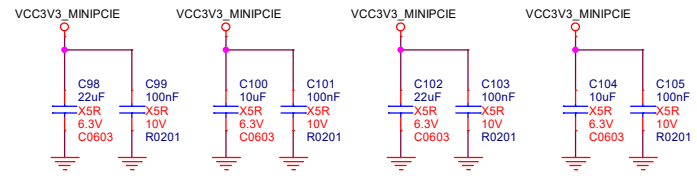
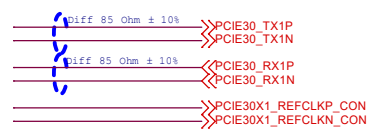
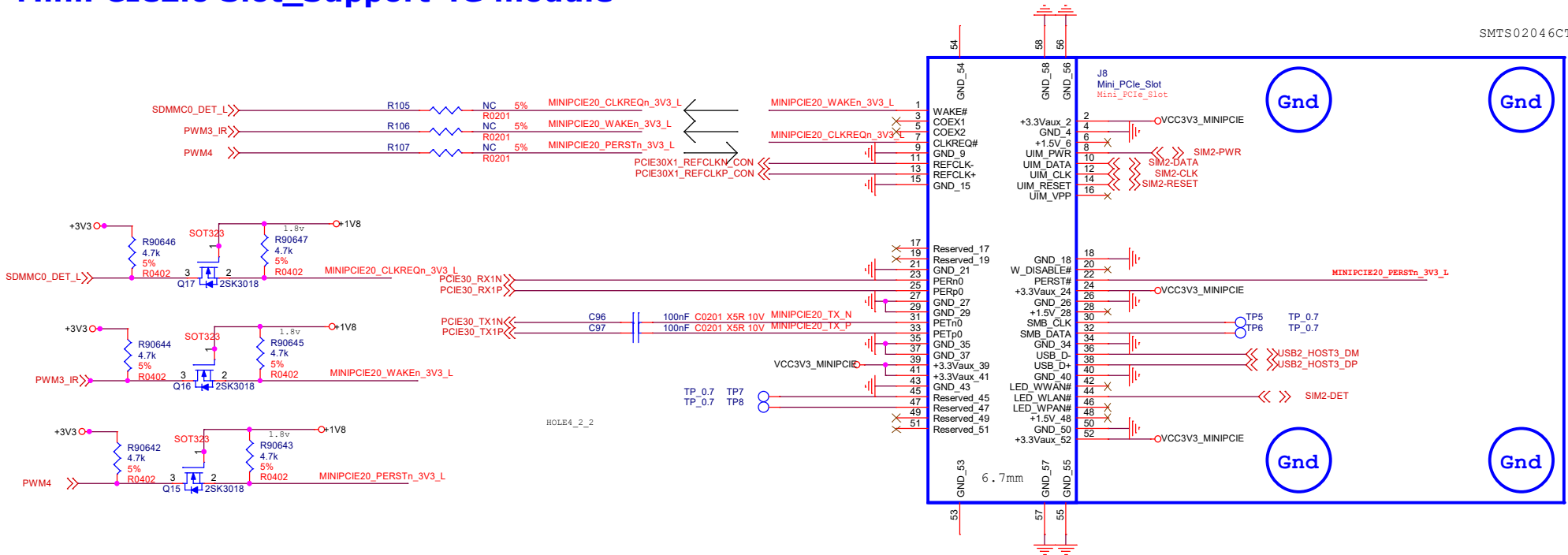




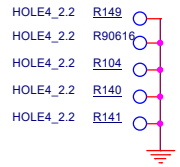


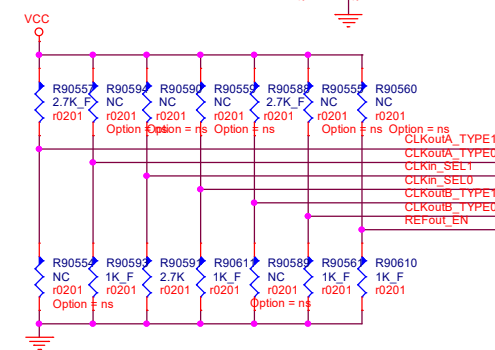
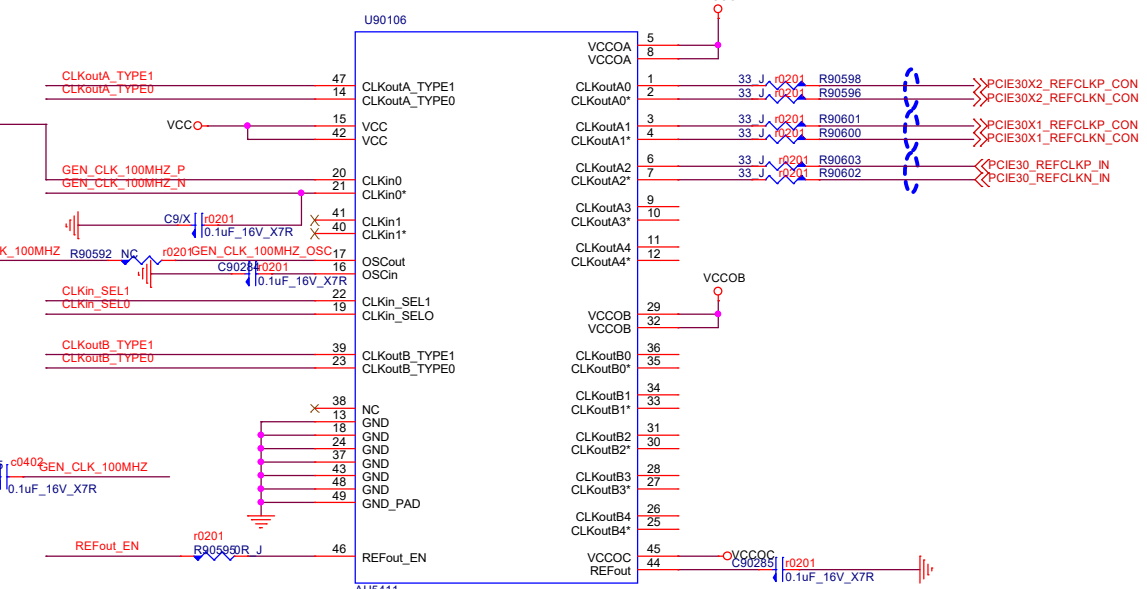
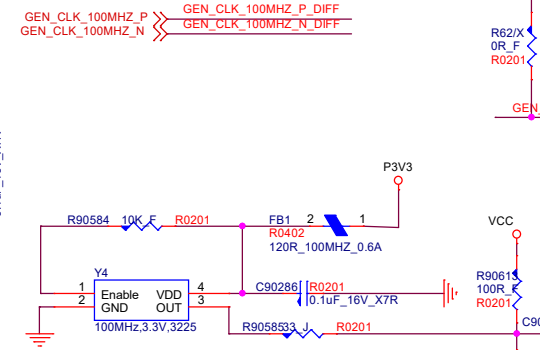
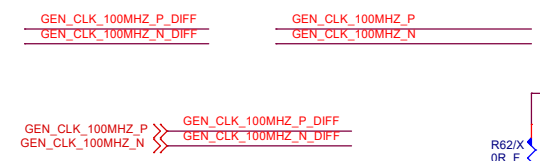
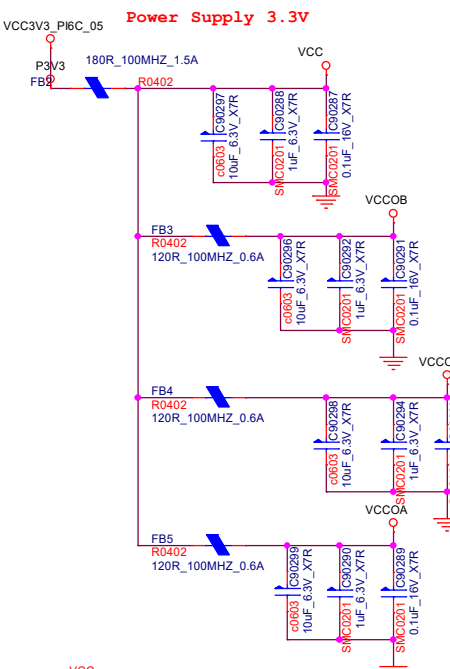
# MiniPCIe2.0 Slot\_Support 4G module

SMTS02046CTJ



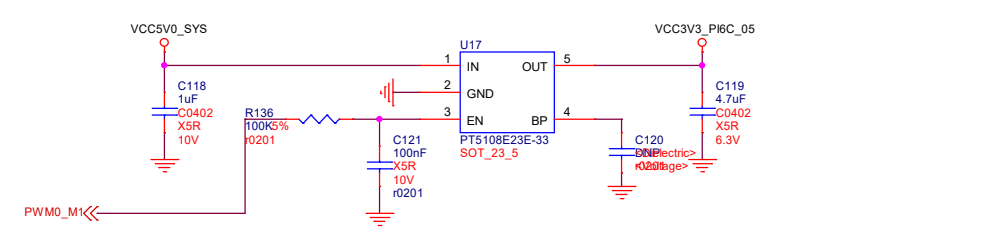
default=L  
L = 3.3V  
H = 3.8V



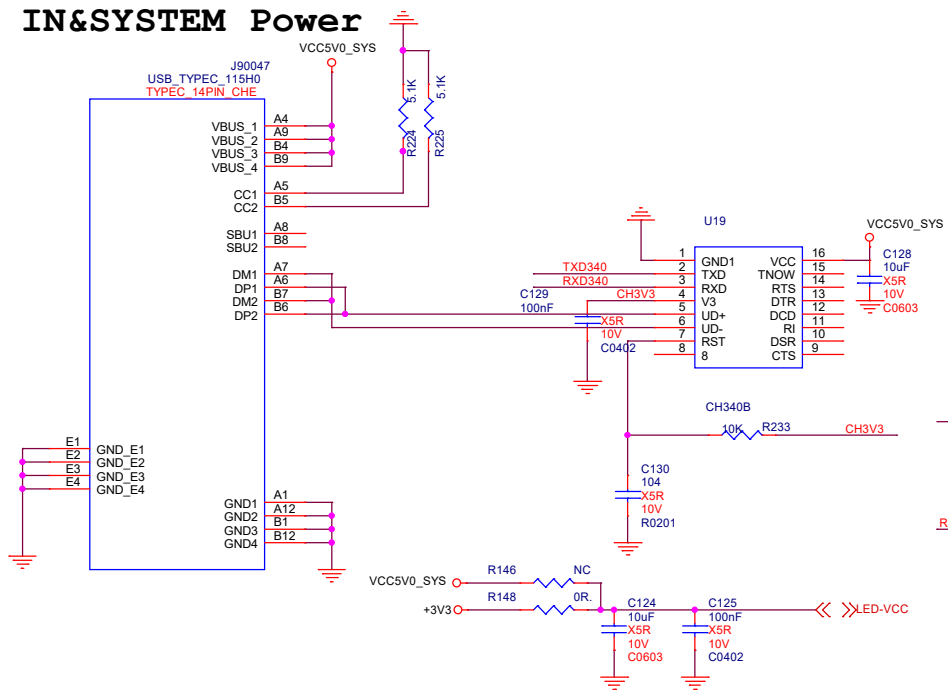


Input clock selection		
CLKin_SEL1	CLKin_SEL0	Selected Clock
0	0	CLKin_SEL0
0	1	CLKin_SEL1
1	0	crystal ac
1	1	crystal dc

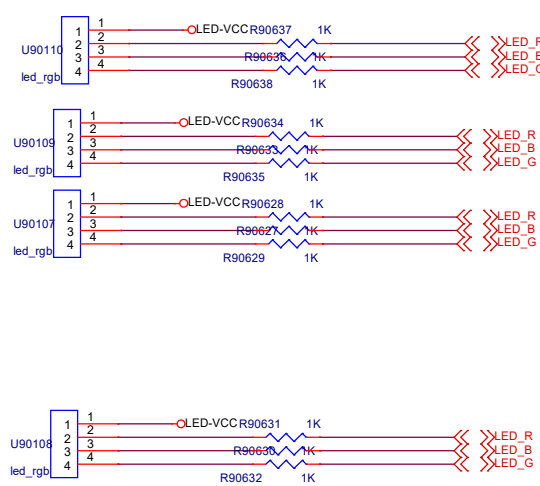
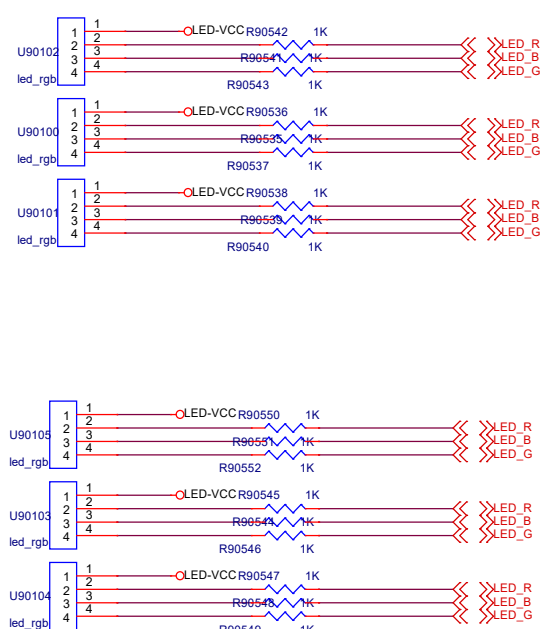
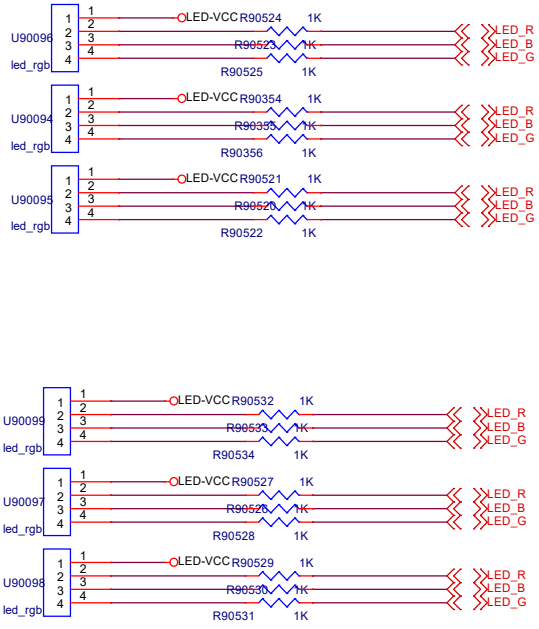
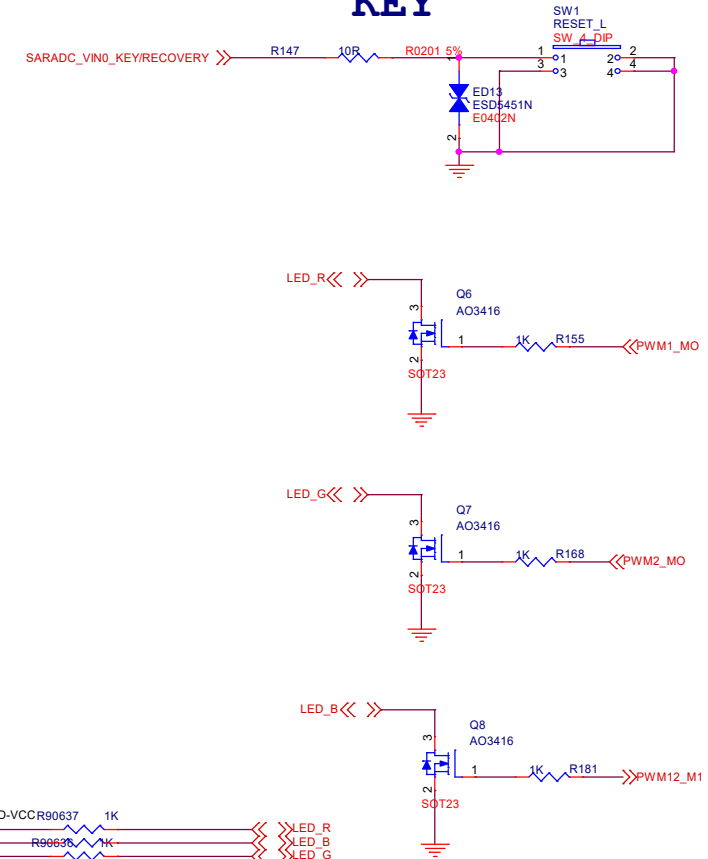
Programming of Output Driver Type		
Clkoutx-Type0	Clkoutx-Type1	CLK BUFFER TYPE
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	HIZ




# DC IN&SYSTEM Power



# KEY





Size	Title: <b>Radxa_E25</b>	REV
	Page Name: <b>11.DC IN/FCARD/KEY/RGB</b>	<b>1.4</b>
Date: <b>Friday, October 28, 2022</b>	Sheet <b>11</b> of <b>11</b>	