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Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

Description

Note

Option

radxa

Size: A3	Title: ROCK3 Compute Module	REV: V1.1
	Page Name: Index_and_Notes	
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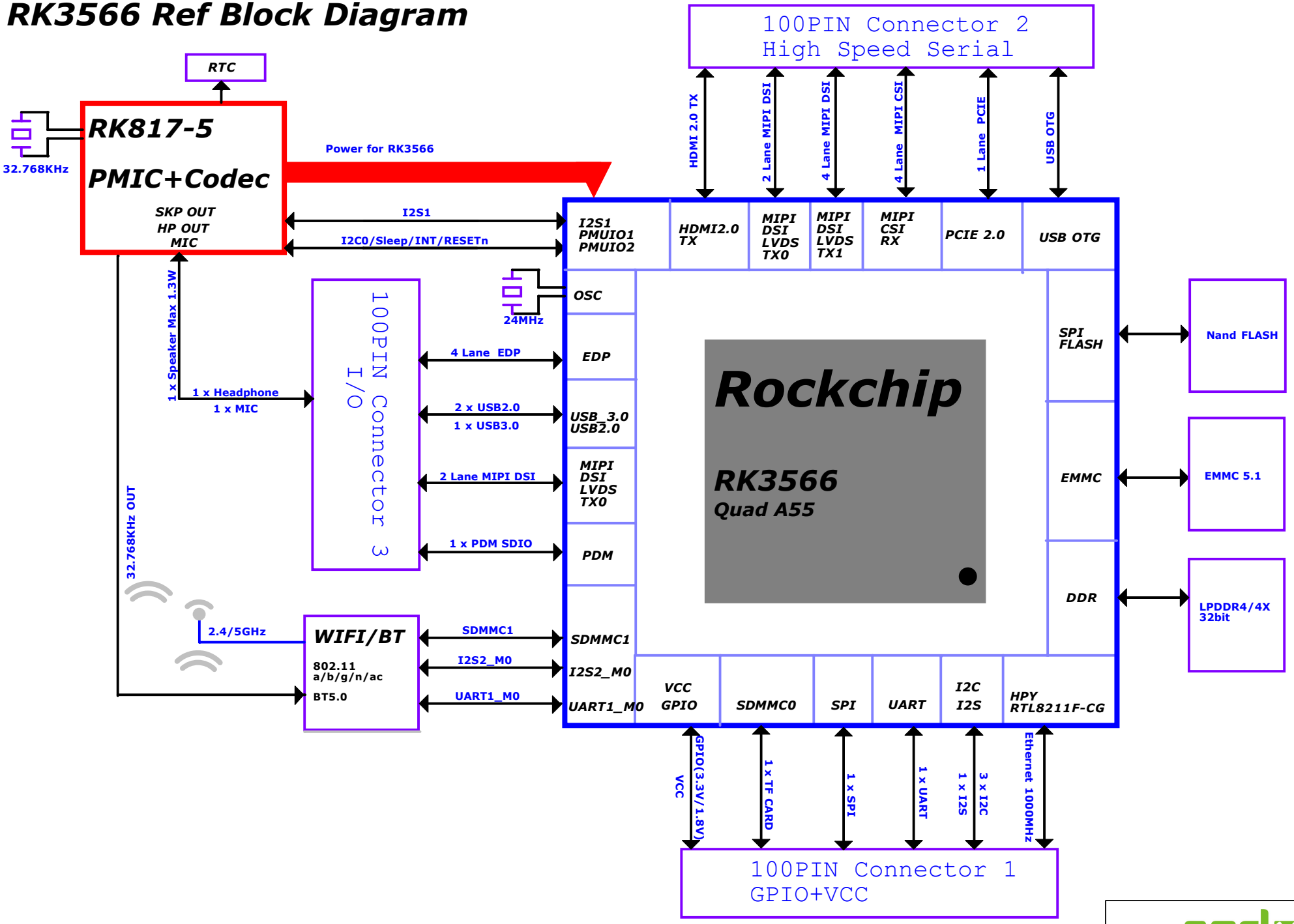
Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2021-02		Revision preliminary version	
V1.1	2021-07			

RK3566 Ref Block Diagram



Size A3	Title: ROCK3 Compute Module	REV V1.1
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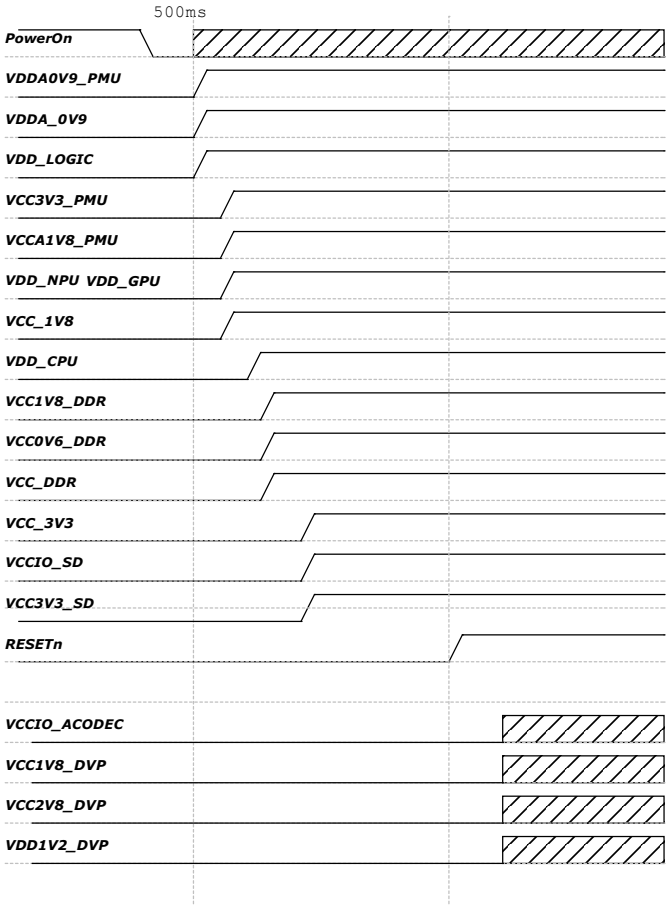
Power Sequence
&Power Path assignment



IO Power Domain Map

Refer to the actual design!

IO Domain	Pin Num	Support IO Voltage		Assignment IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	1P16	YES	NO	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	1N15	YES	YES	VCCA1V8_PMU	VCCA1V8_PMU	1.8V	
VCCIO1	1D13	YES	YES	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	1C13	YES	YES	VCCIO_FLASH	VCC_1V8	1.8V	FLASH_VOL_SEL = 1 --> VCCIO_FLASH = 1.8V
VCCIO3	1F17	YES	YES	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	1E16	YES	YES	VCCIO_WL	VCC_1V8	1.8V	
VCCIO5	1N5 1N6	YES	YES	VCCIO5	VCC_1V8	1.8V	
VCCIO6	1L4 1L5	YES	YES	VCCIO6	VCC_1V8	1.8V	
VCCIO7	1N8	YES	YES	VCCIO7	VCC_3V3	3.3V	

Check the software configuration(dts)
of voltage level, which must be
keep the same as hardware design **!!! Attention**

radxa

Size	Title:	REV
A3	ROCK3 Compute Module	V1.1
	Page Name: Power_Sequence/IO_Domain_Map	
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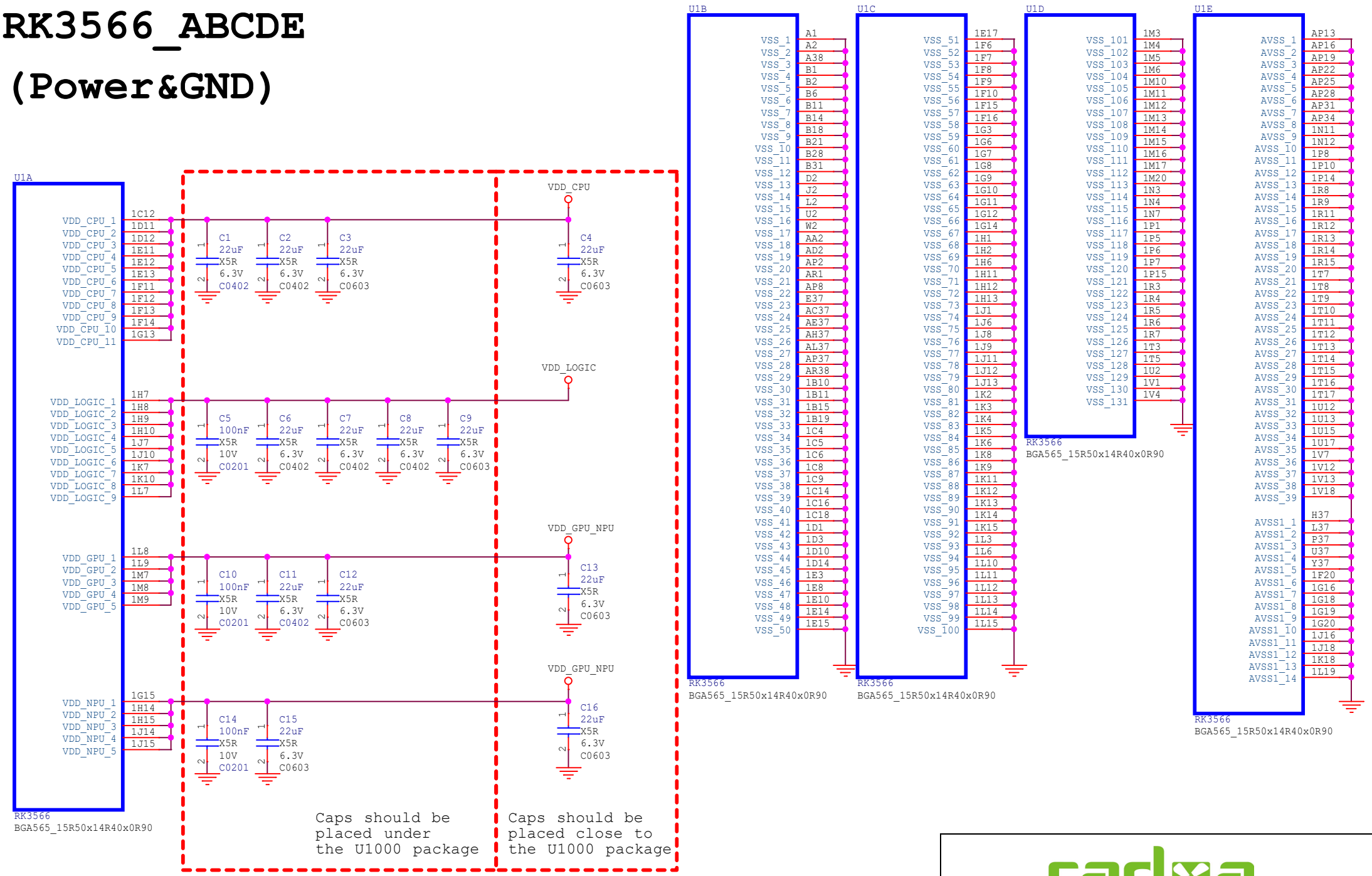
RK3566_ABCDE

(Power&GND)



radxa

Size	Title:	ROCK3 Compute Module	REV
A4	Page Name:	RK3566_Power/GND	V1.1
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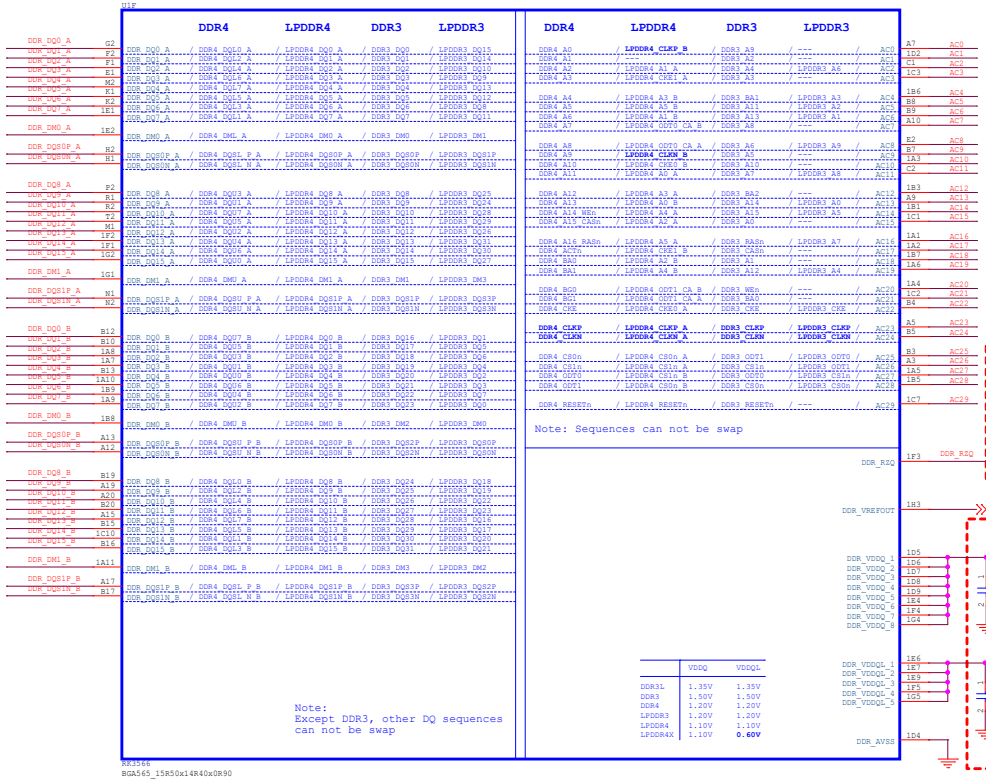
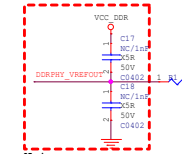
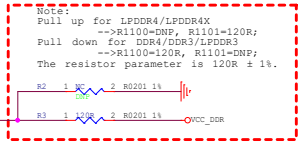
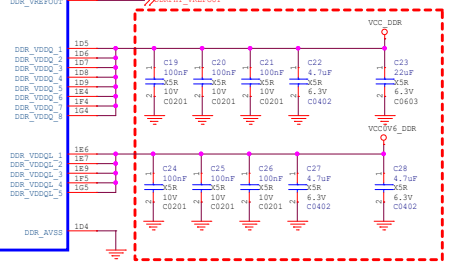
RK3566_F(DDR PHY)



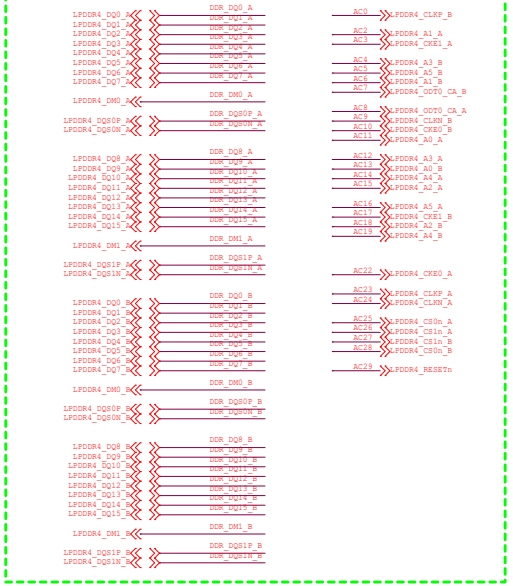






Caps should be placed under
the U1000 package

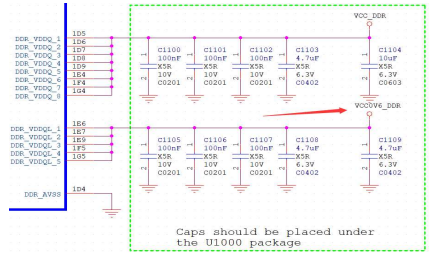
Default: DQ&CA Connection for LPDDR4/LPDDR4X



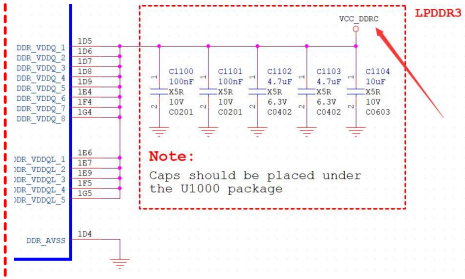
Attention!

For LPDDR4X DDR_VDDQL = 0.6V,
refer to the connection example
For LPDDR3 ultra low power mode,
DDR_VDDQ&DDR_VDDQL connect to VCC_DDRC

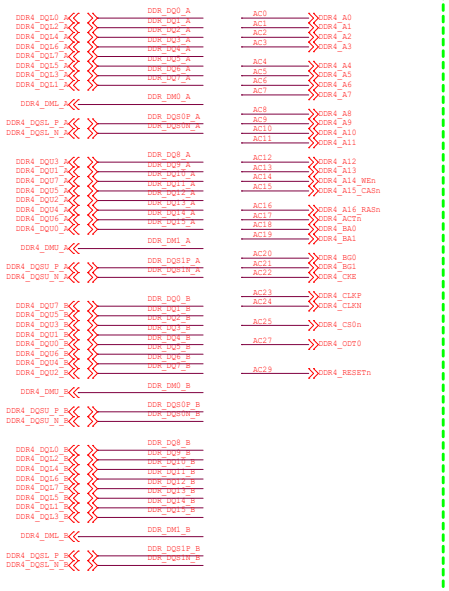
Note:
LPDDR4x mode:
Pin 1E6,1E7,1E9,1F5,1G5 connected to VCC0V6_DDR power supply
For example



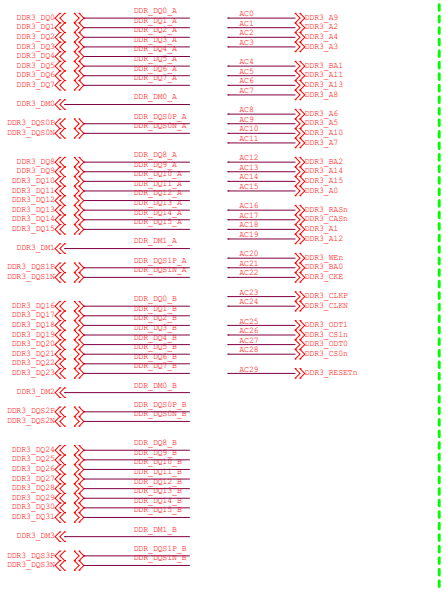
Note:
LPDDR3 ultra low power mode:



Option: DQ&CA Connection for DDR4



Option: DQ&CA Connection for DDR3



Option: DQ&CA Connection for LPDDR3

radxa					
Size	Title:	ROCK3 Compute Module			REV
A2	Page Name:	RK3566_DDR_PHY			V1.1
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RK3566_G(OSC/PLL/PMUIO1/2)

Adjust the load capacitor according to the crystal spec.

U1G

OSC

XOUT24M

XIN24M

PMUIO1 Domain

Operating Voltage=3.3V Only

nPOR_u

PMUIO1

Operating Voltage =1.8V Only

(PMUPLL_AVDD_1V8)

TVSS

GPIO0_D3_d

GPIO0_D4_d

GPIO0_D5_d

GPIO0_D6_d

PMU PLL

PMUPLL_AVDD_0V9

PMUPLL_AVDD_1V8

PMUPLL_AVSS

PMUIO2 Domain

Operating Voltage=1.8V/3.3V

PMUIO2

SYS PLL

SYSPLL_AVDD_0V9

SYSPLL_AVDD_1V8

SYSPLL_AVSS

PMUIO1/2/OSC Domain Logic Power

Operating Voltage=0.9V

PMU_VDD_LOGIC_0V9

RK3566

BGA565_15R50x14R40x0R90

Caps should be placed close to the U1000 package

Caps should be placed under the U1000 package

Caps should be placed under the U1000 package

Caps should be placed under the U1000 package

Caps should be placed close to the U1000 package

Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

U90008

BL24C16A-RRRC

Size	Title:	ROCK3 Compute Module	REV
A3	Page Name:	RK3566_OSC/PLL/PMUIO	V1.1
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RK3566_I(VCCIO2 Domain)

U1I

VCCIO2 Domain

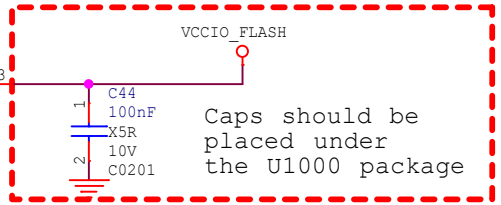
Operating Voltage=1.8V/3.3V

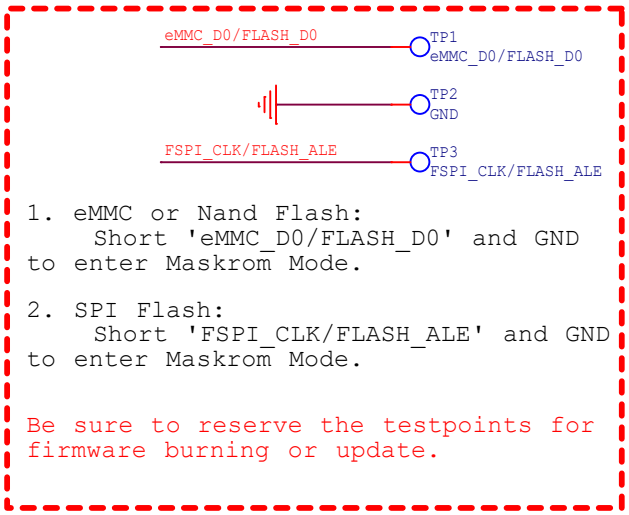
EMMC_D0	/ FLASH_D0	/ GPIO1_B4_u	A32	eMMC_D0/FLASH_D0
EMMC_D1	/ FLASH_D1	/ GPIO1_B5_u	B27	eMMC_D1/FLASH_D1
EMMC_D2	/ FLASH_D2	/ GPIO1_B6_u	B32	eMMC_D2/FLASH_D2
EMMC_D3	/ FLASH_D3	/ GPIO1_B7_u	B29	eMMC_D3/FLASH_D3
EMMC_D4	/ FLASH_D4	/ GPIO1_C0_u	B33	eMMC_D4/FLASH_D4
EMMC_D5	/ FLASH_D5	/ GPIO1_C1_u	A30	eMMC_D5/FLASH_D5
EMMC_D6	/ FLASH_D6	/ GPIO1_C2_u	B30	eMMC_D6/FLASH_D6
EMMC_D7	/ FLASH_D7	/ GPIO1_C3_u	A33	eMMC_D7/FLASH_D7
EMMC_CMD	/ FLASH_WRn	/ GPIO1_C4_u	A27	eMMC_CMD/FLASH_WRn
EMMC_CLKOUT	/ FLASH_DQS	/ GPIO1_C5_d	A29	R14 1 22R 2 R0201 5% eMMC_CLKOUT/FLASH_DQS
EMMC_DATA_STROBE	/ FSPI_CS1n / FLASH_CLE	/ GPIO1_C6_d	1A16	eMMC_DATA_STROBE/FLASH_CLE
EMMC_RSTn	/ FSPI_D2 / FLASH_WPn	/ GPIO1_C7_d	1B16	eMMC_RSTn/FSPI_D2/FLASH_WPn
	FSPI_CLK / FLASH_ALE	/ GPIO1_D0_d	1A15	FSPI_CLK/FLASH_ALE
	FSPI_D0 / FLASH_RDY	/ GPIO1_D1_u	1A17	FSPI_D0/FLASH_RDY
	FSPI_D1 / FLASH_RDn	/ GPIO1_D2_u	1A18	FSPI_D1/FLASH_RDn
	FSPI_CS0n / FLASH_CS0n	/ GPIO1_D3_u	1B17	FSPI_CS0n/FLASH_CS0n
	FSPI_D3 / FLASH_CS1n	/ GPIO1_D4_u	1C15	FSPI_D3/FLASH_CS1n

Default is determined by Pin
FLASH_VOL_SEL/GPIO0_A7_u:
L:VCCIO2 must supply 3.3V
H:VCCIO2 must supply 1.8V

VCCIO2 — 1C13

RK3566
BGA565_15R50x14R40x0R90





Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

RK3566_J(VCCIO3 Domain)

U1J

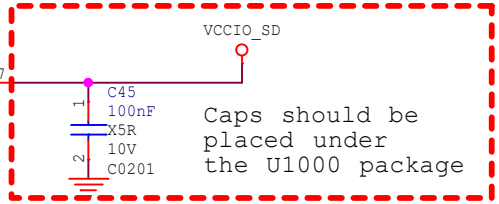
VCCIO3 Domain

Operating Voltage=1.8V/3.3V

PWM8_M1 / SDMMC0_D0	/ UART2_TX_M1 / UART6_TX_M1	/ GPIO1_D5_u	1E20	SDMMC0_D0
PWM9_M1 / SDMMC0_D1	/ UART2_RX_M1 / UART6_RX_M1	/ GPIO1_D6_u	1F19	SDMMC0_D1
SDMMC0_D2	/ ARM_JTAG_TCK / UART5_CTSn_M0	/ GPIO1_D7_u	1D20	SDMMC0_D2
SDMMC0_D3	/ ARM_JTAG_TMS / UART5_RTSn_M0	/ GPIO2_A0_u	1F18	SDMMC0_D3
PWM10_M1 / SDMMC0_CMD	/ UART5_RX_M0	/ GPIO2_A1_u	1E19	SDMMC0_CMD
SDMMC0_CLK	/ TEST_CLKOUT / UART5_TX_M0	/ GPIO2_A2_d	G38	R15 1 22R 2 R0201 5% SDMMC0_CLK

VCCIO3 — 1F17

RK3566
BGA565_15R50x14R40x0R90



Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

radxa

Size	Title:	ROCK3 Compute Module	REV
A4	Page Name:	RK3566_Flash/SD_Controller	V1.1
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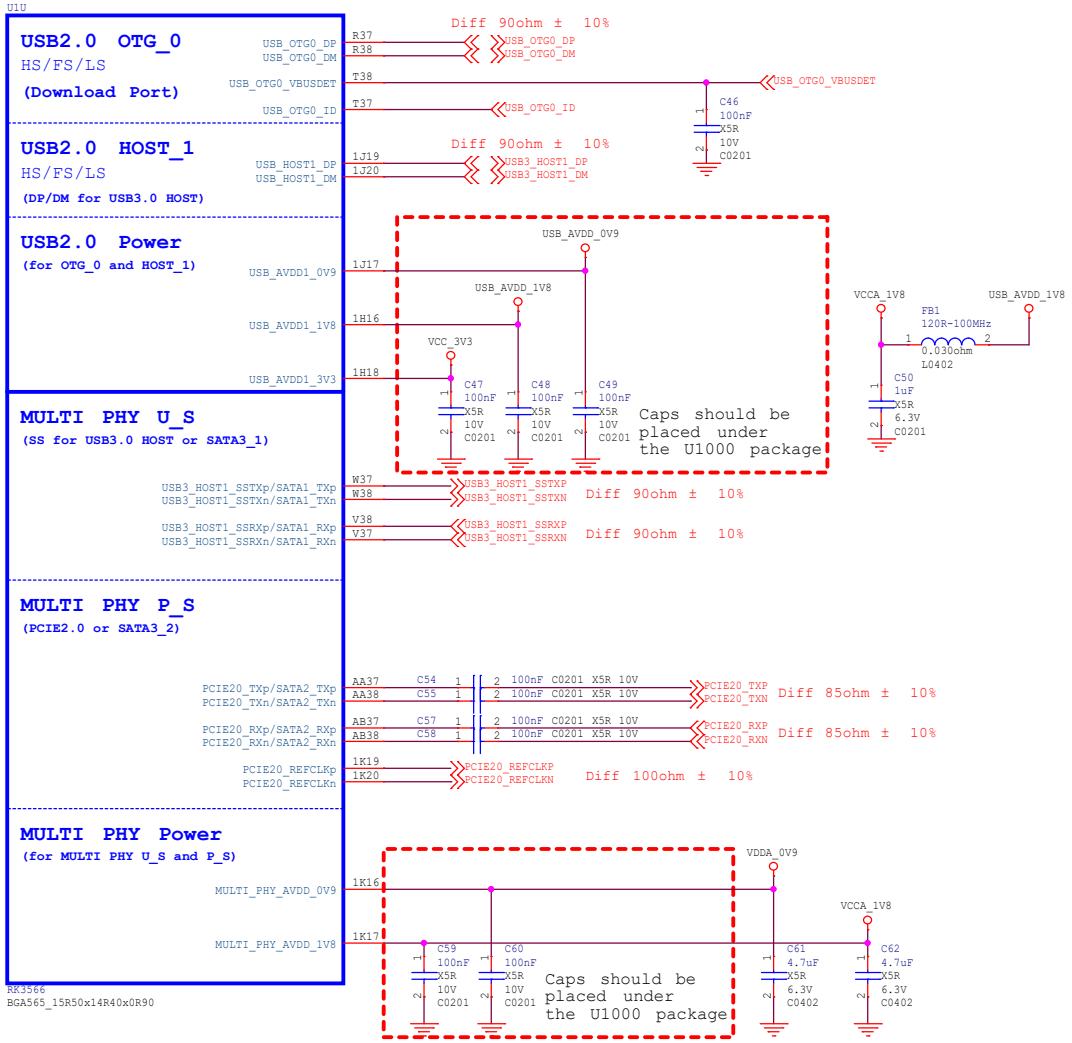
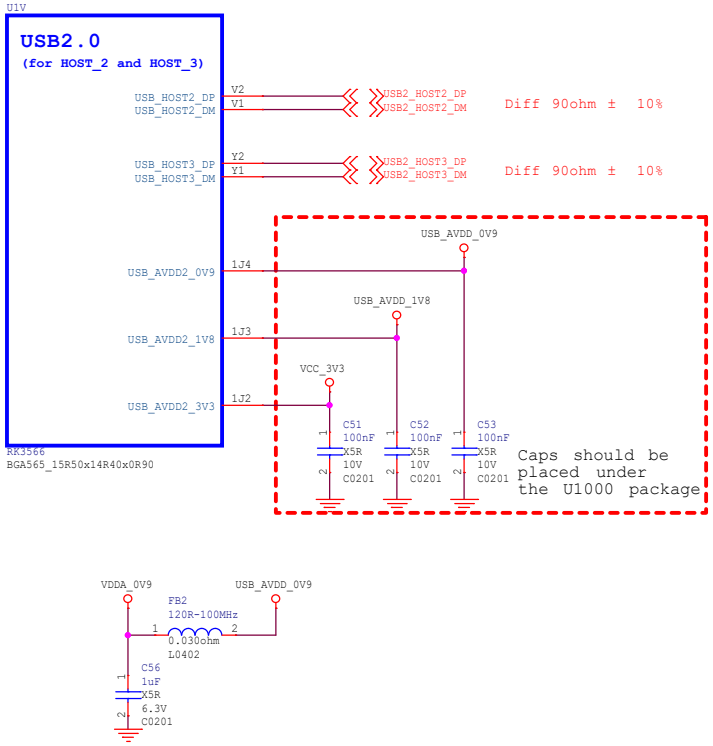
RK3566_U(USB3.0/PCIe2.0x1/SATA)



RK3566_V(USB2.0 HOST)



Size A3	Title: ROCK3 Compute Module		REV V1.1
	Page Name: RK3566_USB/PCIe/SATA_PHY		
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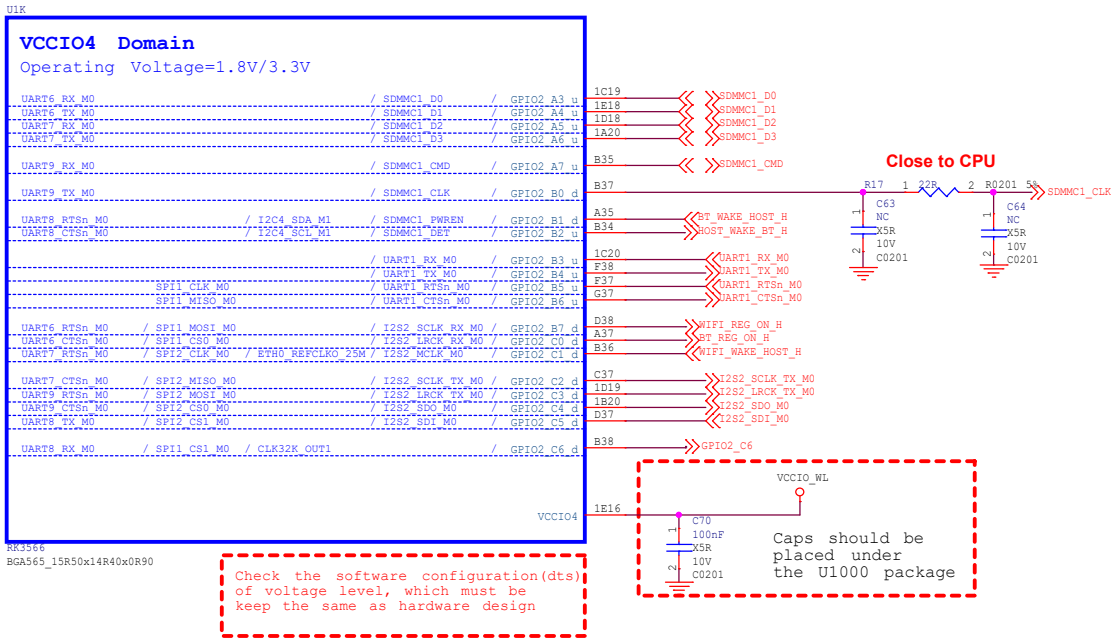
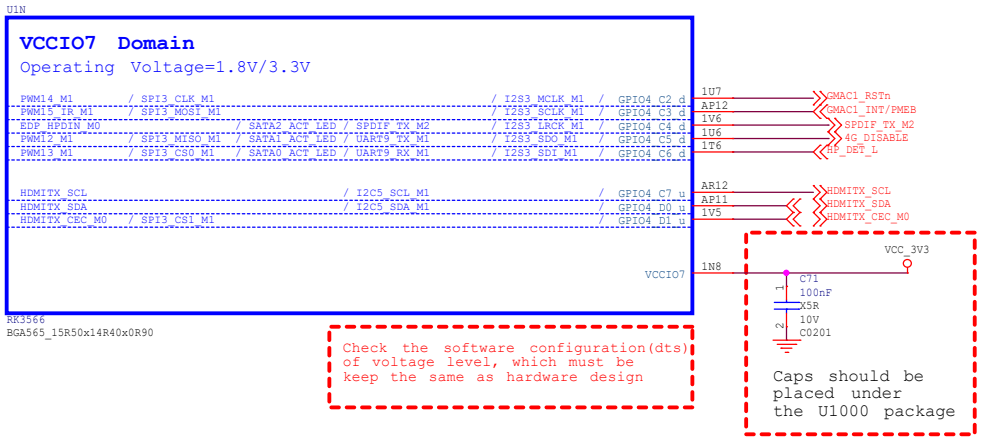
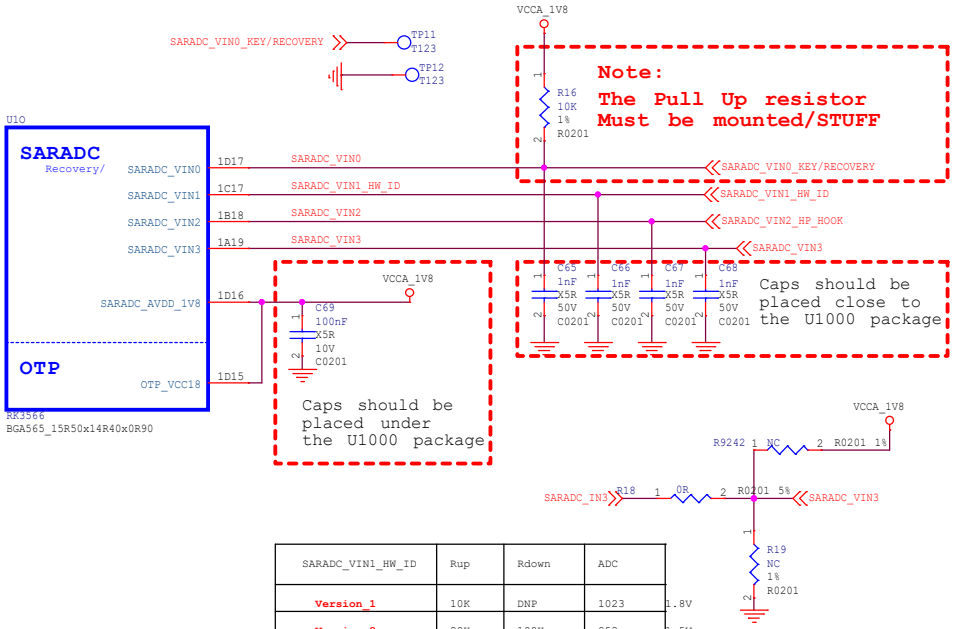
RK3566_K(VCCIO4 Domain)



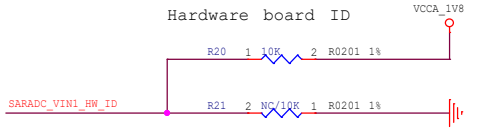
RK3566_N(VCCIO7 Domain)



RK3566_O(SARADC/OTP)



SARADC_VIN1_HW_ID	Rup	Rdown	ADC	
Version_1	10K	DNP	1023	1.8V
Version_2	20K	100K	852	1.5V
Version_3	18K	36K	681	1.2V
Version_4	51K	51K	512	0.9V
Version_5	36K	18K	340	0.6V
Version_6	100K	20K	170	0.3V
Version_7	DNP	10K	0	0V



Size A3	Title: ROCK3 Compute Module		REV V1.1
	Page Name: RK3566_SARADC/GPIO		
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RK3566_P(MIPI_CSI_RX)

U1P

MIPI CSI RX

MIPI_CSI_RX_D0p / MIPI_CSI_RX_D0n	AP18 / AR18	MIPI_CSI_RX_D0P / MIPI_CSI_RX_D0N	Diff 100ohm ± 10%
MIPI_CSI_RX_D1p / MIPI_CSI_RX_D1n	AR17 / AP17	MIPI_CSI_RX_D1P / MIPI_CSI_RX_D1N	Diff 100ohm ± 10%
MIPI_CSI_RX_D2p / MIPI_CSI_RX_D2n	AP15 / AR15	MIPI_CSI_RX_D2P / MIPI_CSI_RX_D2N	Diff 100ohm ± 10%
MIPI_CSI_RX_D3p / MIPI_CSI_RX_D3n	AR14 / AP14	MIPI_CSI_RX_D3P / MIPI_CSI_RX_D3N	Diff 100ohm ± 10%
MIPI_CSI_RX_CLK0p / MIPI_CSI_RX_CLK0n	1V9 / 1U9	MIPI_CSI_RX_CLK0P / MIPI_CSI_RX_CLK0N	Diff 100ohm ± 10%
MIPI_CSI_RX_CLK1p / MIPI_CSI_RX_CLK1n	1V8 / 1U8	MIPI_CSI_RX_CLK1P / MIPI_CSI_RX_CLK1N	Diff 100ohm ± 10%

MIPI_CSI_RX_AVDD_0V9 — 1N9 — MIPI_AVDD_0V9

MIPI_CSI_RX_AVDD_1V8 — 1P9 — MIPI_AVDD_1V8

C73 100nF X5R 10V C0201

C74 100nF X5R 10V C0201

Caps should be placed under the U1000 package

RK3566
BGA565_15R50x14R40x0R90

VDDA0V9_IMAGE — FB3 120R-100MHz (0.030ohm L0402) — MIPI_AVDD_0V9

C72 1uF X5R 6.3V C0201

Usage of MIPI CSI Dx&CLKs

Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

Usage of CIF Interface

Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

BT1120 16bit Mode:
Default: D0-D7 <--> Y0-Y7 , D8-D15 <--> C0-C7
Swap ON: D0-D7 <--> C0-C7 , D8-D15 <--> Y0-Y7

RK3566_M(VCCIO6 Domain)

U1M

VCCIO6 Domain
Operating Voltage=1.8V/3.3V

CIF_D0	EBC_SDDO0	SDMMC2_D0_M0	I2S1_MCLK_M1	VOP_BT656_D0_M1	GPIO3_C6_d
CIF_D1	EBC_SDDO1	SDMMC2_D1_M0	I2S1_SCLK_TX_M1	VOP_BT656_D1_M1	GPIO3_C7_d
CIF_D2	EBC_SDDO2	SDMMC2_D2_M0	I2S1_LRCK_TX_M1	VOP_BT656_D2_M1	GPIO3_D0_d
CIF_D3	EBC_SDDO3	SDMMC2_D3_M0	I2S1_SDO0_M1	VOP_BT656_D3_M1	GPIO3_D1_d
CIF_D4	EBC_SDDO4	SDMMC2_CMD_M0	I2S1_SDI0_M1	VOP_BT656_D4_M1	GPIO3_D2_d
CIF_D5	EBC_SDDO5	SDMMC2_CLK_M0	I2S1_SDI1_M1	VOP_BT656_D5_M1	GPIO3_D3_d
CIF_D6	EBC_SDDO6	SDMMC2_DET_M0	I2S1_SDI2_M1	VOP_BT656_D6_M1	GPIO3_D4_d
CIF_D7	EBC_SDDO7	SDMMC2_PWREN_M0	I2S1_SDI3_M1	VOP_BT656_D7_M1	GPIO3_D5_d
CIF_D8	EBC_SDDO8	GMAC1_TXD2_M1	UART1_TX_M1	PDM_CLK0_M1	GPIO3_D6_d
CIF_D9	EBC_SDDO9	GMAC1_TXD3_M1	UART1_RX_M1	PDM_SDI0_M1	GPIO3_D7_d
CIF_D10	EBC_SDDO10	GMAC1_TXCLK_M1		PDM_CLK1_M1	GPIO4_A0_d
CIF_D11	EBC_SDDO11	GMAC1_RXD2_M1		PDM_SDI1_M1	GPIO4_A1_d
CIF_D12	EBC_SDDO12	GMAC1_RXD3_M1	UART7_TX_M2	PDM_SDI2_M1	GPIO4_A2_d
CIF_D13	EBC_SDDO13	GMAC1_RXCLK_M1	UART7_RX_M2	PDM_SDI3_M1	GPIO4_A3_d
CIF_D14	EBC_SDDO14	GMAC1_TXD0_M1	UART9_TX_M1	I2S2_LRCK_TX_M1	GPIO4_A4_d
CIF_D15	EBC_SDDO15	GMAC1_TXD1_M1	UART9_RX_M2	I2S2_LRCK_RX_M1	GPIO4_A5_d
ISP_FLASHTRIGOUT	EBC_SDCE0	GMAC1_TXEN_M1	SPI3_CS0_M0	I2S1_SCLK_RX_M1	GPIO4_A6_d
CAM_CLKOUT0	EBC_SDCE1	GMAC1_RXD0_M1	SPI3_CS1_M0	I2S1_LRCK_RX_M1	GPIO4_A7_d
CAM_CLKOUT1	EBC_SDCE2	GMAC1_RXD1_M1	SPI3_MISO_M0	I2S1_SDO1_M1	GPIO4_B0_d
ISP_PRELIGHT_TRIG	EBC_SDCE3	GMAC1_RXDV_CRS_M1		I2S1_SDO2_M1	GPIO4_B1_d
I2C4_SDA_M0	EBC_VCOM	GMAC1_RXER_M1	SPI3_MOSI_M0	I2S2_SDI_M1	GPIO4_B2_d
I2C4_SCL_M0	EBC_GDOE	ETH1_REFCLKO_25M_M1	SPI3_CLK_M0	I2S2_SDO_M1	GPIO4_B3_d
ISP_FLASH_TRIGIN / I2C2_SDA_M1	EBC_GDSP			VOP_BT656_CLK_M1	GPIO4_B4_d
I2C2_SCL_M1	EBC_SDSHR			I2S1_SDO3_M1	GPIO4_B5_d
CIF_HREF	EBC_SDLE	GMAC1_MDC_M1	UART1_RTSn_M1	I2S2_MCLK_M1	GPIO4_B6_d
CIF_VSYNC	EBC_SDOE	GMAC1_MDIO_M1		I2S2_SCLK_TX_M1	GPIO4_B7_d
PWM11_IR_M1 / CIF_CLKOUT	EBC_GDCLK				GPIO4_C0_d
CIF_CLKIN	EBC_SDCLK	GMAC1_MCLKINOUT_M1	UART1_CTSn_M1	I2S2_SCLK_RX_M1	GPIO4_C1_d

1T2 I2S1_MCLK_M1
1U1 I2S1_SCLK_TX_M1
AP1 I2S1_LRCK_TX_M1
AN2 I2S1_SDO0_M1
AM2 I2S1_SDI0_M1
AM1 I2S1_SDI1_M1
1R2 I2S1_SDI2_M1
1T1 I2S1_SDI3_M1

AL2 PDM_CLK0_M1
AL1 PDM_SDI0_M1
AK2 PDM_CLK1_M1
1P2 PDM_SDI1_M1
1R1 PDM_SDI2_M1
AJ2 PDM_SDI3_M1

1N2 — R26 1K — R0201 5% — PI_nLED_Activity

AJ1 BT_nDis

AH2 SPI3_CSO_M0

1N1 I2S1_LRCK_RX_M1
1L2 SPI3_MISO_M0

AG2 I2S1_SDO2_M1

AF2 SPI3_MOSI_M0
AE2 SPI3_CLK_M0

AF1 I2C2_SDA_M1
AD1 I2C2_SCL_M1

1L1 WL_nDis
AC2 nPWR_LED

AB2 PWM11

AB1 CAM_GPIO

1V8_3.3V
R22 2.2K 5% R0201
R23 2.2K 5% R0201
I2C2_SDA_M1
I2C2_SCL_M1

R27 NC 5% R0201

VCCIO6_1 / VCCIO6_2 — 1L4 / 1L5

1V8_3.3V
C78 100nF X5R 10V C0201

Caps should be placed under the U1000 package

Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

Note:
default VCCIO of Camera is 1.8V

1V8_3.3V
D1 ESD5621W04-2/TR SOD_323
C75 4.7UF X5R 6.3V C0402
R28 NC 5% R0201

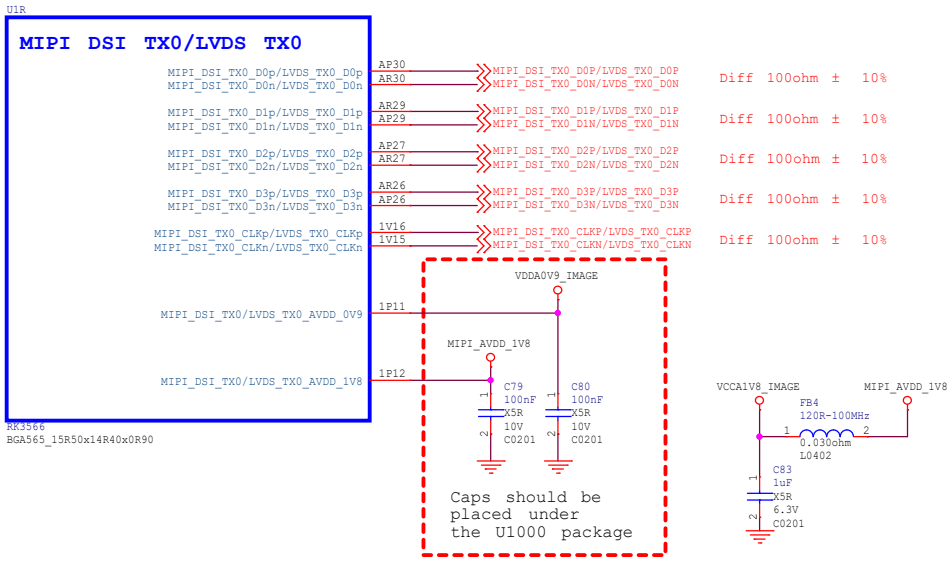
R24 0R R0603 5% — GPIO_VREF
R26 NC R0402 5% — VCC_1V8
R29 NC R0402 5% — VCC_3V3

+1V8
+3V3
R30 0R R0402 5% — VCC_1V8
R31 0R R0402 5% — VCC_3V3
C76 100nF X5R 10V C0201
C77 100nF X5R 10V C0201

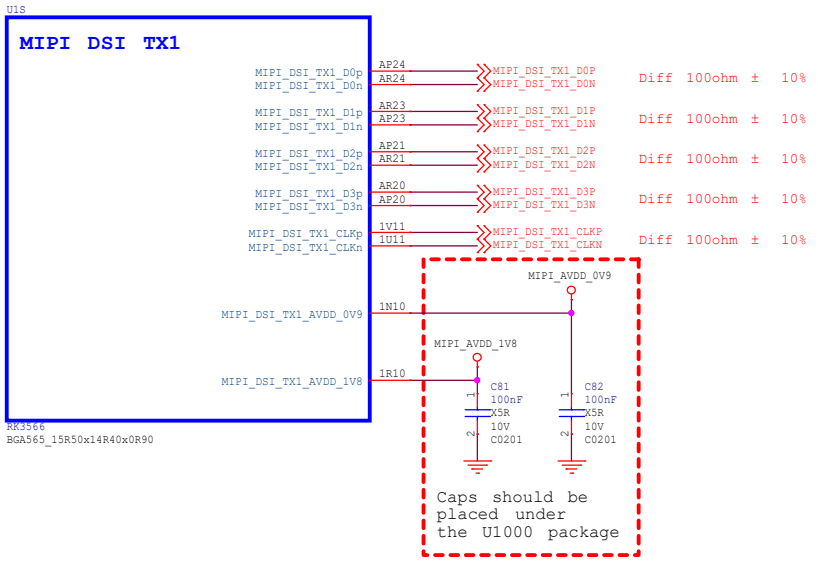
radxa

Size A3	Title: ROCK3 Compute Module		REV V1.1
	Page Name: RK3566_VI_Interface		
Date: Thursday, January 06, 2022	Sheet 11 of 25		

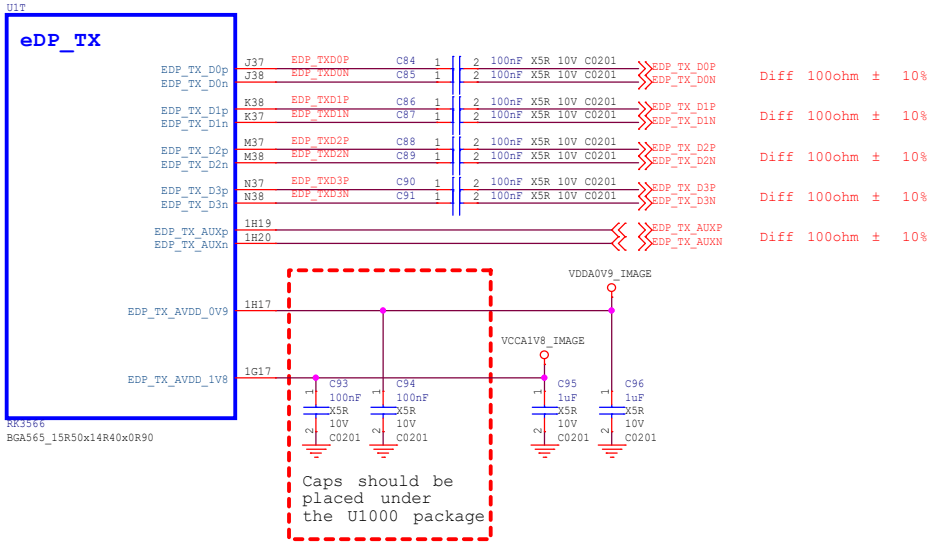
RK3566_R(MIPI_DSI_TX0/LVDS_TX0)



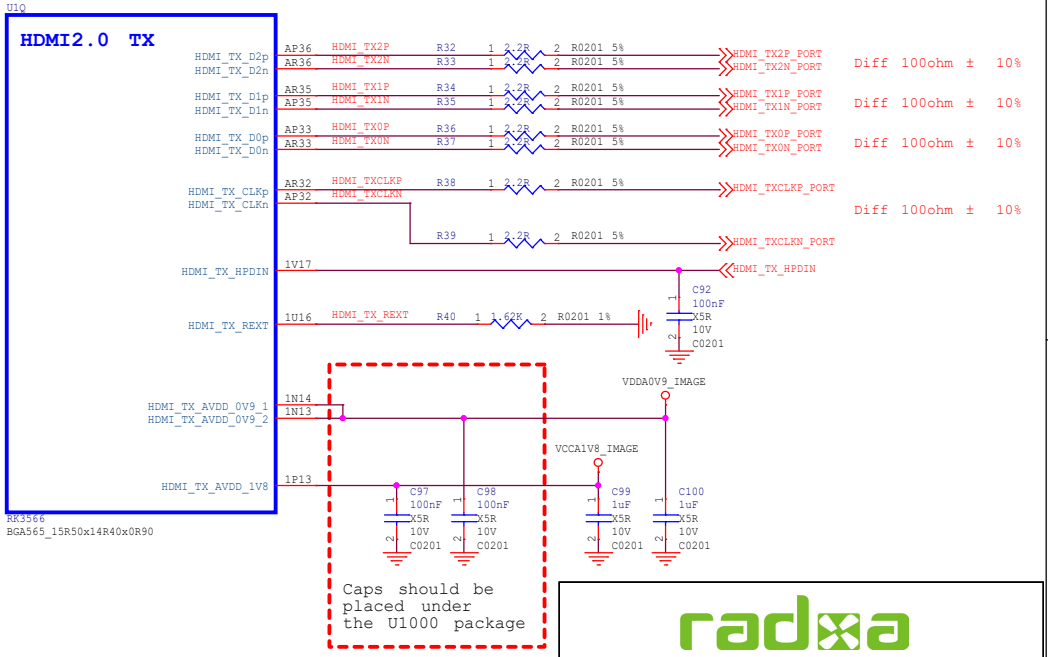
RK3566_S(MIPI_DSI_TX1)



RK3566_T(eDP TX)



RK3566_Q(HDMI2.0 TX)



radxa

Size	Title:	ROCK3 Compute Module	REV
A3	Page Name:	RK3566_VO_Interface_1	V1.1
Date:	Thursday, January 06, 2022	Sheet 12 of 25	

RK3566_L(VCCIO5 Domain)

U1L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

	VOP_BT1120_D0 / SPI1_CS0_M1			SDMMC2_D0_M1	GPIO3_A1_d
	VOP_BT1120_D1	GMAC1_TXD2_M0	I2S3_MCLK_M0	SDMMC2_D1_M1	GPIO3_A2_d
	VOP_BT1120_D2	GMAC1_TXD3_M0	I2S3_SCLK_M0	SDMMC2_D2_M1	GPIO3_A3_d
	VOP_BT1120_D3	GMAC1_RXD2_M0	I2S3_LRCK_M0	SDMMC2_D3_M1	GPIO3_A4_d
	VOP_BT1120_D4	GMAC1_RXD3_M0	I2S3_SDO_M0	SDMMC2_CMD_M1	GPIO3_A5_d
	VOP_BT1120_CLK	GMAC1_TXCLK_M0	I2S3_SDI_M0	SDMMC2_CLK_M1	GPIO3_A6_d
	VOP_BT1120_D5	GMAC1_RXCLK_M0		SDMMC2_DET_M1	GPIO3_A7_d
	VOP_BT1120_D6	ETH1_REFCLKO_25M_M0		SDMMC2_PWREN_M1	GPIO3_B0_d
PWM8_M0	VOP_BT1120_D7	GMAC1_RXD0_M0	UART4_RX_M1		GPIO3_B1_d
PWM9_M0	VOP_BT1120_D8	GMAC1_RXD1_M0	UART4_TX_M1		GPIO3_B2_d
	VOP_BT1120_D9 / I2C5_SCL_M0	GMAC1_RXDV_CRS_M0		PDM_SDI0_M2	GPIO3_B3_d
	VOP_BT1120_D10 / I2C5_SDA_M0	GMAC1_RXER_M0		PDM_SDI1_M2	GPIO3_B4_d
PWM10_M0	VOP_BT1120_D11 / I2C3_SCL_M1	GMAC1_TXD0_M0			GPIO3_B5_d
PWM11_IR_M0	VOP_BT1120_D12 / I2C3_SDA_M1	GMAC1_TXD1_M0			GPIO3_B6_d
PWM12_M0		GMAC1_TXEN_M0	UART3_TX_M1	PDM_SDI2_M2	GPIO3_B7_d
PWM13_M0		GMAC1_MCLKINOUT_M0	UART3_RX_M1	PDM_SDI3_M2	GPIO3_C0_d
	VOP_BT1120_D13 / SPI1_MOSI_M1		PCIE20_PERSTn_M1	I2S1_SDO2_M2	GPIO3_C1_d
	VOP_BT1120_D14 / SPI1_MISO_M1		UART5_TX_M1	I2S1_SDO3_M2	GPIO3_C2_d
	VOP_BT1120_D15 / SPI1_CLK_M1		UART5_RX_M1	I2S1_SCLK_RX_M2	GPIO3_C3_d
PWM14_M0	/ VOP_PWM_M1	GMAC1_MDC_M0	UART7_TX_M1	PDM_CLK1_M2	GPIO3_C4_d
PWM15_IR_M0	/ SPDIF_TX_M1	GMAC1_MDIO_M0	UART7_RX_M1	I2S1_LRCK_RX_M2	GPIO3_C5_d

VCCIO5_1
VCCIO5_2

RK3566
BGA565_15R50x14R40x0R90

1U5 GPIO3_A1
AR10 GMAC1_TXD2_M0
AP10 GMAC1_TXD3_M0
AR9 GMAC1_RXD2_M0
AP9 GMAC1_RXD3_M0
1U4 GMAC1_TXCLK_M0
1V3 GMAC1_RXCLK_M0

AR7 R41 1 NC 2 R0201 5% ETH1_REFCLKO_25M_M0
AP7 GMAC1_RXD0_M0
AR6 GMAC1_RXD1_M0
AP6 GMAC1_RXDV_CRS_M0
1U3 GPIO3_B4
1T4 GMAC1_TXD0_M0
1V2 GMAC1_TXD1_M0
AP5 GMAC1_TXEN_M0

AR4 GMAC1_MCLKINOUT_M0
AP4 GPIO3_C1
AP3 GPIO3_C2
AR2 GPIO3_C3

1P3 GMAC1_MDC_M0
1P4 GMAC1_MDIO_M0

1N5
1N6

R42 1 NC 2 R0402 5% VCC_1V8
R43 1 0R 2 R0402 5% VCC_3V3

C101
100nF
X5R
10V
C0201

Caps should be placed under the U1000 package

Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

radxa

Size	Title:	ROCK3 Compute Module	REV
A4	Page Name:	RK3566_VO_Interface_2	V1.1
Date:	Thursday, January 06, 2022	Sheet 13 of 25	

RK3566_H(VCCIO1 Domain)

U1H

VCCIO1 Domain

Operating Voltage=1.8V/3.3V

	I2C3_SDA_M0	UART3_RX_M0	AUDIOPWM_LOUT_p	GPIO1_A0_u	A22
	I2C3_SCL_M0	UART3_TX_M0	AUDIOPWM_LOUT_n	GPIO1_A1_u	B22
SCR_CLK	I2S1_MCLK_M0	UART3_RTSn_M0		GPIO1_A2_d	A23
SCR_IO	I2S1_SCLK_TX_M0	UART3_CTSn_M0		GPIO1_A3_d	B23
	I2S1_SCLK_RX_M0	UART4_RX_M0	PDM_CLK1_M0 / SPDIF_TX_M0	GPIO1_A4_d	1A13
SCR_RST	I2S1_LRCK_TX_M0	UART4_RTSn_M0		GPIO1_A5_d	B24
	I2S1_LRCK_RX_M0	UART4_TX_M0	PDM_CLK0_M0 / AUDIOPWM_ROUT_p	GPIO1_A6_d	1A14
SCR_DET	I2S1_SDO0_M0	UART4_CTSn_M0	AUDIOPWM_ROUT_n	GPIO1_A7_d	B25
	I2S1_SDO1_M0	I2S1_SDI3_M0	PDM_SDI3_M0 / PCIE20_CLKREQn_M2	GPIO1_B0_d	1B13
	I2S1_SDO2_M0	I2S1_SDI2_M0	PDM_SDI2_M0 / PCIE20_WAKEn_M2	GPIO1_B1_d	A26
	I2S1_SDO3_M0	I2S1_SDI1_M0	PDM_SDI1_M0 / PCIE20_PERSTn_M2	GPIO1_B2_d	B26
		I2S1_SDI0_M0	PDM_SDI0_M0	GPIO1_B3_d	1B14
				VCCIO1	1D13

RK3566
BGA565_15R50x14R40x0R90

Check the software configuration(dts) of voltage level, which must be keep the same as hardware design

A22 I2C3_SDA_ACODEC
B22 I2C3_SCL_ACODEC
A23 I2S1_MCLK_M0_PMIC
B23 I2S1_SCLK_TX_M0_PMIC
1A13 PDM_CLK1_M0
B24 I2S1_LRCK_TX_M0_PMIC
1A14 PDM_CLK0_M0_PMIC
B25 I2S1_SDO0_M0_PMIC
1B13 GPIO1_B0 R46 1 0R 2 R0201 5% PCIE20_CLKREQn_M2
A26 GPIO1_B1 PDM_SDI2_M0_ADC
B26 GPIO1_B2 Pcie_nRST
1B14 I2S1_SDI0_M0/PDM_SDI0_M0_PMIC

VCCIO_ACODEC
C102 100nF X5R 10V C0201
Caps should be placed under the U1000 package

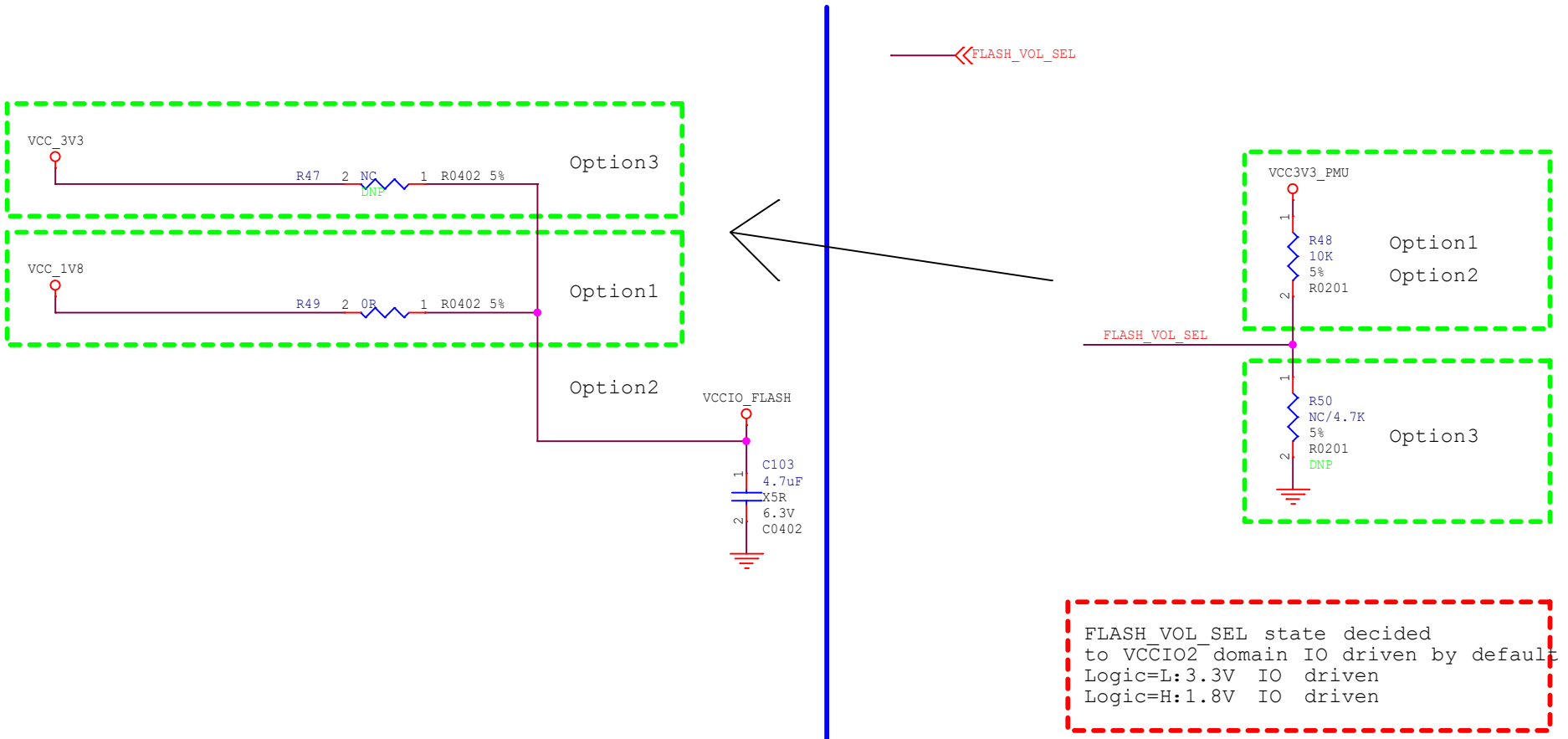
VCCIO_ACODEC = 3.3V as default

VCCIO_ACODEC
R44 2.2K 5% R0201
R45 2.2K 5% R0201
I2C3_SDA_ACODEC
I2C3_SCL_ACODEC

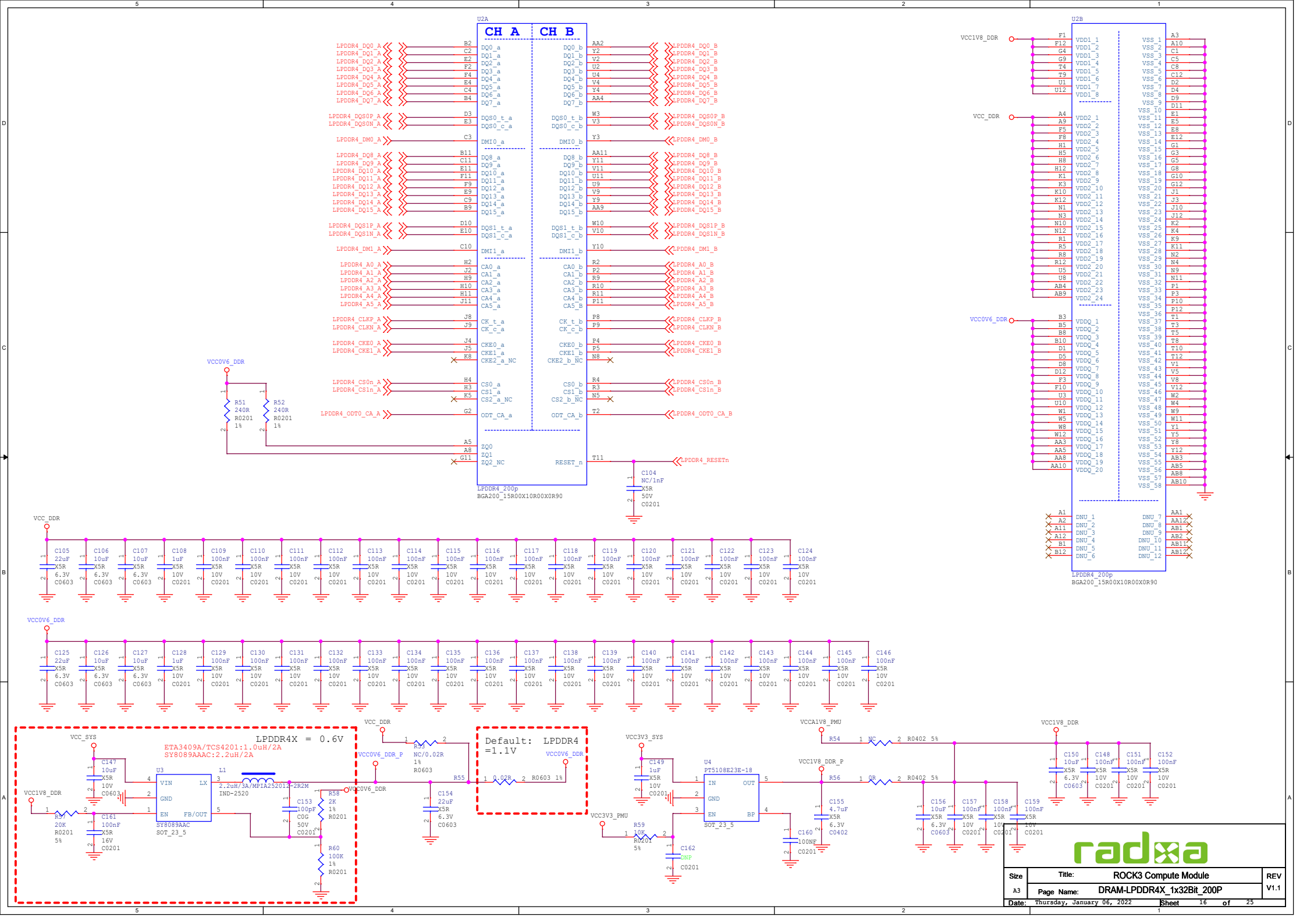
Size	Title:	ROCK3 Compute Module	REV
A4	Page Name:	RK3566_Audio_Interface	V1.1
Date:	Thursday, January 06, 2022	Sheet 14 of 25	

Flash Power Manage

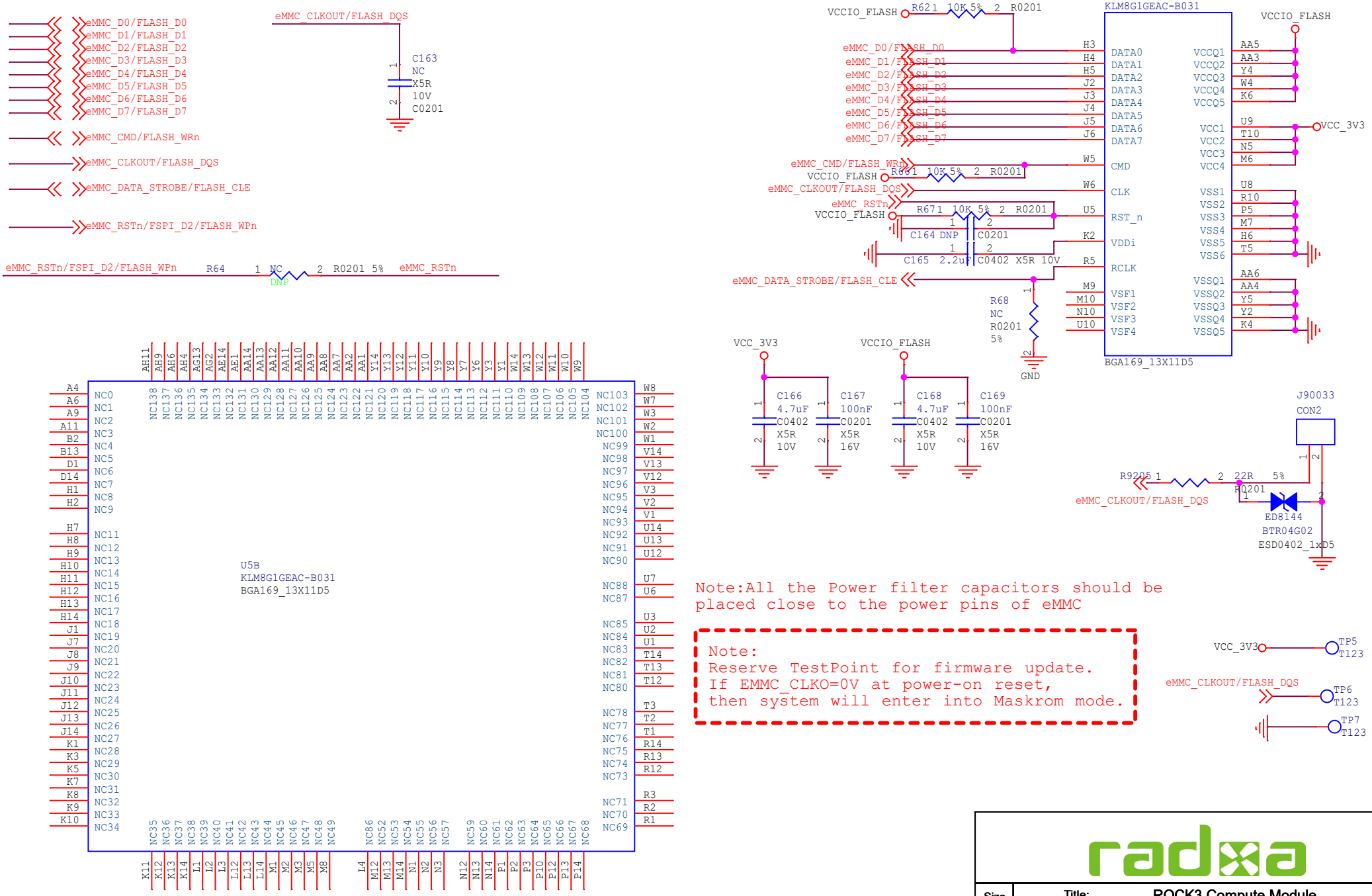
	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)



Size: A4	Title: ROCK3 Compute Module	REV: V1.1
	Page Name: Power_Flash_Power_Manage	
Date: Thursday, January 06, 2022	Sheet 15 of 25	


U2A
CH A
CH B
LPDDR4_200p
BGA200_15R00X10R00X0R90
U2B
LPDDR4_200p
BGA200_15R00X10R00X0R90
VCC0V6_DDR
R51 240R R0201 1%
R52 240R R0201 1%
C104 NC/1nF X5R 50V C0201
VCC_DDR
VCC1V8_DDR
VCC0V6_DDR
VCC_SYS
LPDDR4X = 0.6V
ETA3409A/TCS4201:1.0uH/2A
SY8089AAAC:2.2uH/2A
U3
SY8089AAC
SOT_23_5
L1
2.2uH/3A/MPIA252012-2R2M
IND-2520
R57 20K R0201 5%
C161 100nF X5R 16V C0201
C153 100pF C0G 50V C0201
R58 2K 1% R0201
R60 100K 1% R0201
R55 0.02R R0603 1%
C154 22uF X5R 6.3V C0603
Default: LPDDR4 =1.1V
VCC3V3_SYS
VCC3V3_PMU
U4
PT5108E23E-18
SOT_23_5
R59 10K R0201 5%
C160 100NF C0201
C162 DNP C0201
VCCA1V8_PMU
VCC1V8_DDR_P
R54 NC R0402 5%
R56 0R R0402 5%
C155 4.7uF X5R 6.3V C0402
C156 10uF X5R 6.3V C0603
C157 100nF X5R 10V C0201
C158 100nF X5R 10V C0201
C159 100nF X5R 10V C0201
C150 10uF X5R 6.3V C0603
C148 100nF X5R 10V C0201
C151 100nF X5R 10V C0201
C152 100nF X5R 10V C0201
radxa
Size A3
Title: ROCK3 Compute Module
REV V1.1
Page Name: DRAM-LPDDR4X_1x32Bit_200P
Date: Thursday, January 06, 2022
Sheet 16 of 25

eMMC FLASH



Size: A4	Title: ROCK3 Compute Module	REV: V1.1
	Page Name: Memory-eMMC/SPI	
Date: Thursday, January 06, 2022	Sheet 17 of 25	

FSPI_CLK/FLASH_ALE
FSPI_D0/FLASH_RDY
FSPI_D1/FLASH_RDn
eMMC_RSTn/FSPI_D2/FLASH_WPn
FSPI_D3/FLASH_CS1n
FSPI_CS0n/FLASH_CS0n

VCCIO_FLASH
R71
10K
5%
R0201
eMMC_RSTn/FSPI_D2/FLASH_WPn

VCCIO_FLASH
R73
10K
5%
R0201
FSPI_D3/FLASH_CS1n

default VCC = VCCIO_FLASH 1.8V

U4300
25Q64DWZPIG
WSON_8_6X5_9
FSPI_CS0n/FLASH_CS0n
FSPI_D1/FLASH_RDn
eMMC_RSTn/FSPI_D2/FLASH_WPn
CS
DO(D1)
WP(D2)
VSS
VCC
HOLD(D3)
CLK
DI(D0)
EPAD
FSPI_D3/FLASH_CS1n
FSPI_CLK/FLASH_ALE
FSPI_D0/FLASH_RDY
R72
22R
R0201
5%
EEPROM_nWP

VCCIO_FLASH
C170
100nF
X5R
10V
C0201
C171
1uF
X5R
6.3V
C0201

J90034
CON2
R9206
22R
5%
R0201
FSPI_CLK/FLASH_ALE
ED8145
BTR04G02
ESD0402_1xD5

HDMI_TXDDC_SCL_PORT
HDMI_TXDDC_SDA_PORT
HDMI_TX_CEC_PORT
HDMI_TX_HPD_PORT
HDMITX_SCL
HDMITX_SDA
HDMITX_CEC_M0
HDMI_TX_HPDIN

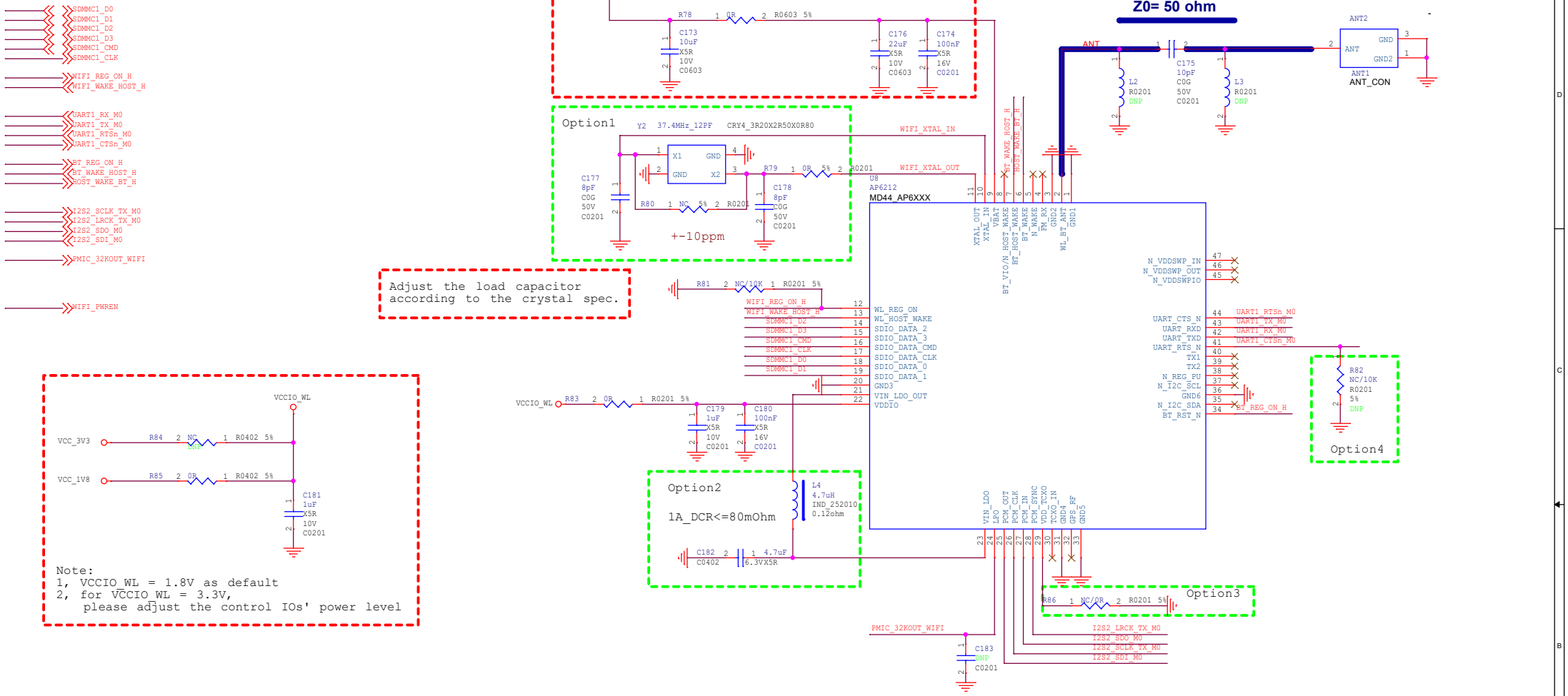
HDMI

VCC_3V3
U7
D2
B5819WS SOD_323
VCC5V_MIDU
A2
VCCB
VCCA
B2
HDMI_TXDDC_SDA_PORT
HDMI_TXDDC_SCL_PORT
HDMI_TX_CEC_PORT
A1
B1
C1
D1
B1
B2
B3
B4
A1
A2
A3
A4
A3
B3
C3
D3
HDMITX_SDA
HDMITX_SCL
HDMITX_CEC_M0
VCC_3V3
C2
OE
GND
D2
UM3204H
C172
100nF
C0201
GND

HDMI_TX_HPDIN
R76
1K
5%
R0201
HDMI_TX_HPD_PORT
R77
100K
5%
R0201

Size	Title:	ROCK3 Compute Module	REV
A4	Page Name:	Flash-SPI-HDMI	V1.1
Date:	Thursday, January 06, 2022	Sheet 18 of 25	

SDIO WIFI/BT Module-1T1R

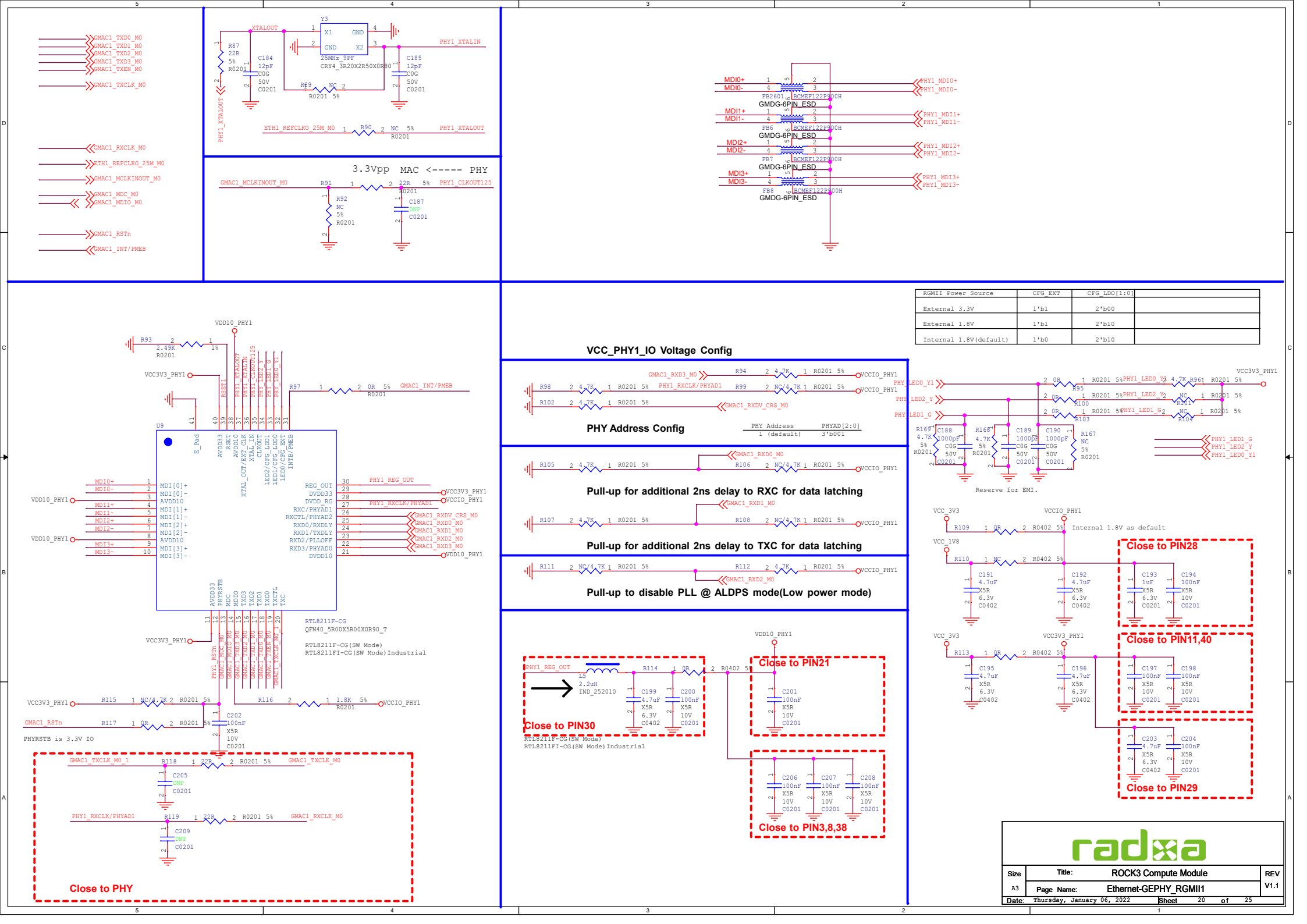


Note:
Yes: option circuit be mounted
No: option circuit not be mounted

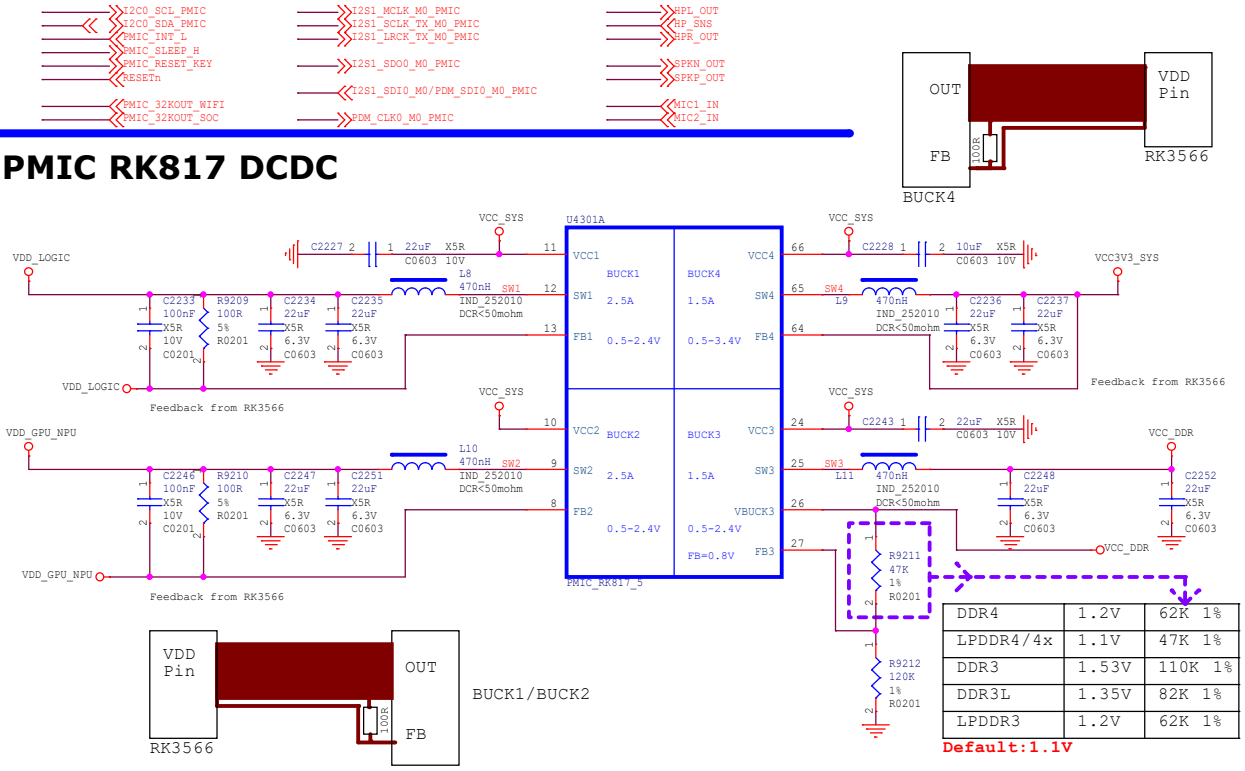
OPTION	WIFI				BT	Crystals	VCCIO_SDIO	OPTION1	OPTION2	OPTION3	OPTION4
	a	b/g/n	ac	5GHz							
AW-CM256SM	Yes	Yes	Yes	Yes	4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	No
AP6236/AP6212	No	Yes	No	No	4.2/4.0	26MHz	1.71-3.6V	Yes	Yes	No	No
AP6256/AP6255	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	No
RTL8189ETV Module F89FTSM12-W3	No	Yes	No	No	No	Module Integrated	1.8-3.3V	No	No	No	No
RTL8723DS Module 6223A-SRD	No	Yes	No	No	4.2	Module Integrated	1.62-3.6V	No	No	No	Yes
RTL8821CS Module 6221A-SRC	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	No

radxa

Size	Title:	ROCK3 Compute Module	REV
A3	Page Name:	WIFI/BT-SDIO_1T1R+UART	V1.1
Date:	Thursday, January 06, 2022	Sheet 19 of 25	


GMAC1_TXD0_M0
GMAC1_TXD1_M0
GMAC1_TXD2_M0
GMAC1_TXD3_M0
GMAC1_TXEN_M0
GMAC1_TXCLK_M0
GMAC1_RXCLK_M0
ETH1_REFCLKO_25M_M0
GMAC1_MCLKINOUT_M0
GMAC1_MDC_M0
GMAC1_MDIO_M0
GMAC1_RSTn
GMAC1_INT/PMEB
Y3
25MHz_9PF
CRY4_3R20X2R50X0R80
R87 22R 5% R0201
C184 12pF C0G 50V C0201
C185 12pF C0G 50V C0201
R89 NC R0201 5%
XTALOUT
PHY1_XTALIN
PHY1_XTALOUT
ETH1_REFCLKO_25M_M0
R90 NC 5% R0201
3.3Vpp MAC <----- PHY
R91 22R 5% R0201
R92 NC 5% R0201
C187 DNP C0201
PHY1_CLKOUT125
MDI0+
MDI0-
MDI1+
MDI1-
MDI2+
MDI2-
MDI3+
MDI3-
FB260Ω BCMEF122P900H GMDG-6PIN_ESD
FB6
FB7
FB8
PHY1_MDI0+
PHY1_MDI0-
PHY1_MDI1+
PHY1_MDI1-
PHY1_MDI2+
PHY1_MDI2-
PHY1_MDI3+
PHY1_MDI3-
VDD10_PHY1
R93 2.49K 1% R0201
VCC3V3_PHY1
R97 0R 5% R0201
GMAC1_INT/PMEB
U9
E_Pad
AVDD33
RSET
AVDD10
XTAL_OUT/EXT_CLK
XTAL_IN
CLKOUT
LED2/CFG_LDO1
LED1/CFG_LDO0
LED0/CFG_EXT
INTB/PMEB
MDI[0]+
MDI[0]-
AVDD10
MDI[1]+
MDI[1]-
MDI[2]+
MDI[2]-
AVDD10
MDI[3]+
MDI[3]-
REG_OUT
DVDD33
DVDD_RG
RXC/PHYAD1
RXCTL/PHYAD2
RXD0/RXDLY
RXD1/TXDLY
RXD2/PLLOFF
RXD3/PHYAD0
DVDD10
PHY1_REG_OUT
VCC3V3_PHY1
VCCIO_PHY1
PHY1_RXCLK/PHYAD1
GMAC1_RXDV_CRS_M0
GMAC1_RXD0_M0
GMAC1_RXD1_M0
GMAC1_RXD2_M0
GMAC1_RXD3_M0
PHYRSTB
MDC
MDIO
TXD3
TXD2
TXD1
TXD0
TXCTL
TXC
RTL8211F-CG
QFN40_5R00X5R00X0R90_T
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
PHY1_RSTn
GMAC1_MDC_M0
GMAC1_MDIO_M0
GMAC1_TXD3_M0
GMAC1_TXD2_M0
GMAC1_TXD1_M0
GMAC1_TXD0_M0
GMAC1_TXCTL_M0
GMAC1_TXCLK_M0_1
R115 NC/4.7K R0201 5%
R116 1.8K 5% R0201
R117 0R R0201 5%
GMAC1_RSTn
C202 100nF X5R 10V C0201
PHYRSTB is 3.3V IO
R118 22R R0201 5%
GMAC1_TXCLK_M0
C205 DNP C0201
R119 22R R0201 5%
PHY1_RXCLK/PHYAD1
GMAC1_RXCLK_M0
C209 DNP C0201
Close to PHY
VCC_PHY1_IO Voltage Config
R94 4.7K R0201 5%
R98 4.7K R0201 5%
R99 NC/4.7K R0201 5%
R102 4.7K R0201 5%
GMAC1_RXD3_M0
PHY1_RXCLK/PHYAD1
GMAC1_RXDV_CRS_M0
PHY Address Configuration
PHY Address
PHYAD[2:0]
1 (default)
3'b001
R105 4.7K R0201 5%
R106 NC/4.7K R0201 5%
GMAC1_RXD0_M0
Pull-up for additional 2ns delay to RXC for data latching
R107 4.7K R0201 5%
R108 NC/4.7K R0201 5%
GMAC1_RXD1_M0
Pull-up for additional 2ns delay to TXC for data latching
R111 NC/4.7K R0201 5%
R112 4.7K R0201 5%
GMAC1_RXD2_M0
Pull-up to disable PLL @ ALDPS mode(Low power mode)
L5 2.2uH IND_252010
R114 0R R0402 5%
C199 4.7uF X5R 6.3V C0402
C200 100nF X5R 10V C0201
C201 100nF X5R 10V C0201
Close to PIN30
Close to PIN21
C206 100nF X5R 10V C0201
C207 100nF X5R 10V C0201
C208 100nF X5R 10V C0201
Close to PIN3,8,38
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
RGMII Power Source | CFG_EXT | CFG_LDO[1:0]
External 3.3V | 1'b1 | 2'b00
External 1.8V | 1'b1 | 2'b10
Internal 1.8V(default) | 1'b0 | 2'b10
PHY_LED0_Y
PHY_LED2_Y
PHY_LED1_G
R95 0R
R100 0R
R103 0R
R96 4.7K
R101 NC
R104 NC
R165 4.7K 5% R0201
R168 4.7K 5% R0201
R167 NC 5% R0201
C188 1000pF C0G 50V C0201
C189 1000pF C0G 50V C0201
C190 1000pF C0G 50V C0201
PHY1_LED0_Y
PHY1_LED2_Y
PHY1_LED1_G
Reserve for EMI.
VCC_3V3
VCC_1V8
VCCIO_PHY1
R109 0R R0402 5%
R110 NC R0402 5%
Internal 1.8V as default
C191 4.7uF X5R 6.3V C0402
C192 4.7uF X5R 6.3V C0402
C193 1uF X5R 6.3V C0201
C194 100nF X5R 10V C0201
Close to PIN28
R113 0R R0402 5%
C195 4.7uF X5R 6.3V C0402
C196 4.7uF X5R 6.3V C0402
C197 100nF X5R 10V C0201
C198 100nF X5R 10V C0201
Close to PIN11,40
C203 4.7uF X5R 6.3V C0402
C204 100nF X5R 10V C0201
Close to PIN29
radxa
Size A3
Title: ROCK3 Compute Module
REV V1.1
Page Name: Ethernet-GEPHY_RGMII1
Date: Thursday, January 06, 2022
Sheet 20 of 25

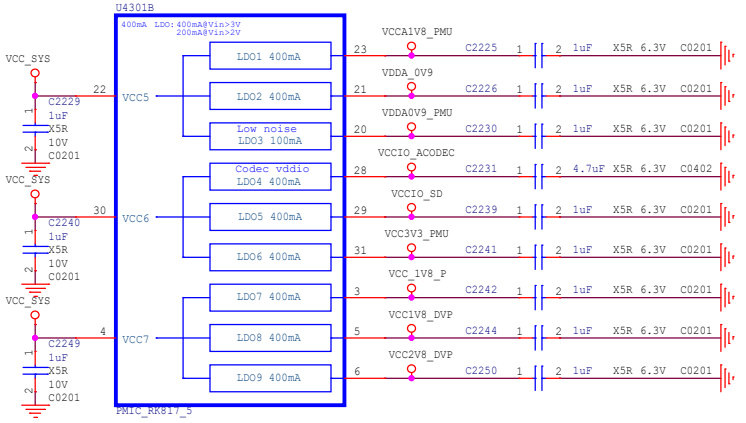
PMIC RK817 DCDC



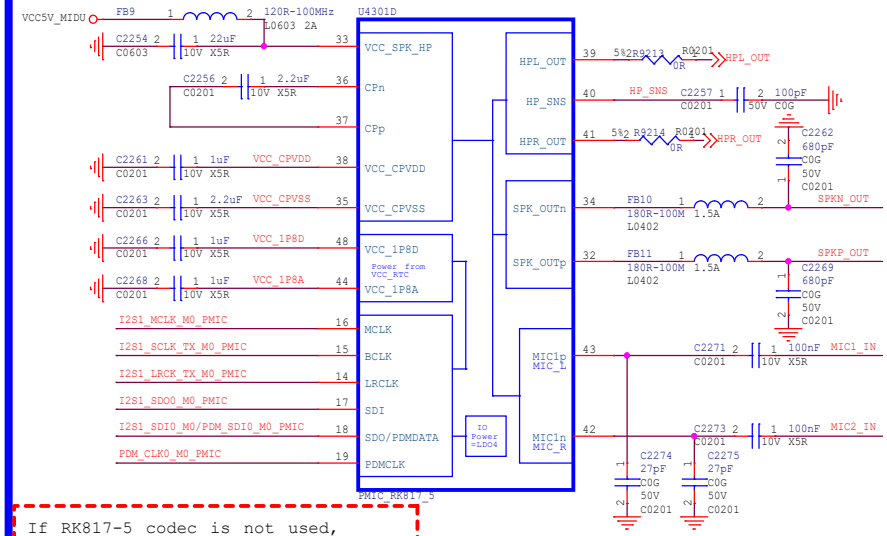
DDR4	1.2V	62K 1%
LPDDR4/4x	1.1V	47K 1%
DDR3	1.53V	110K 1%
DDR3L	1.35V	82K 1%
LPDDR3	1.2V	62K 1%

Default:1.1V

PMIC RK817 LDO

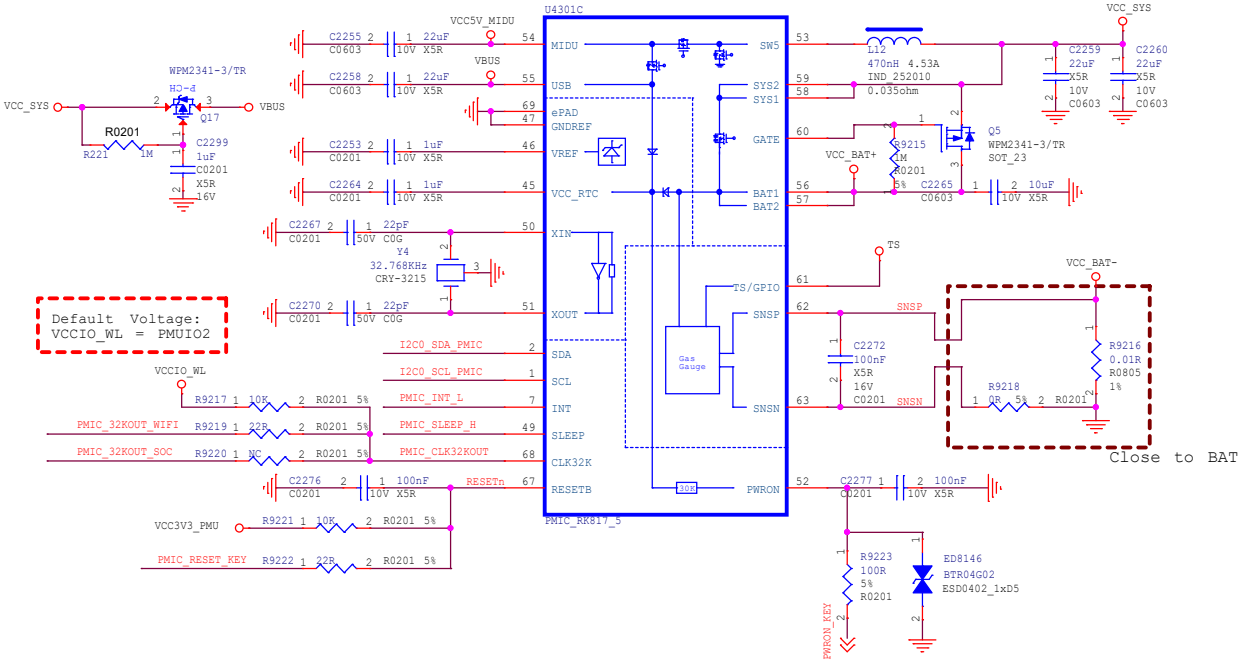


PMIC RK817 CODEC

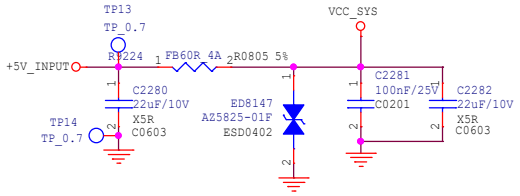


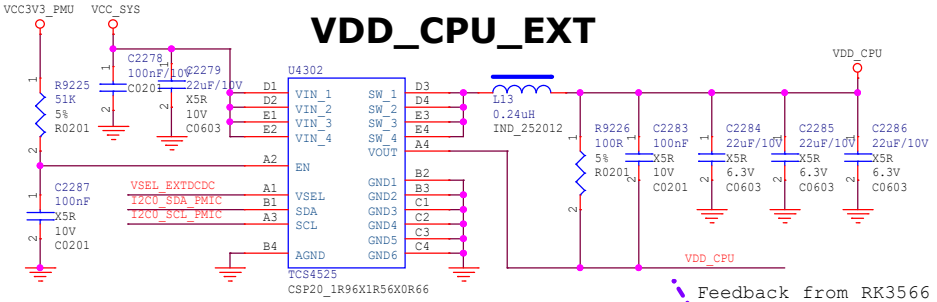
If RK817-5 codec is not used,
then Pin 14,15,16,17,19,40 Tie VSS
Pin 18,36,37,38,35,39,41,34,32,43,42
Leave floating

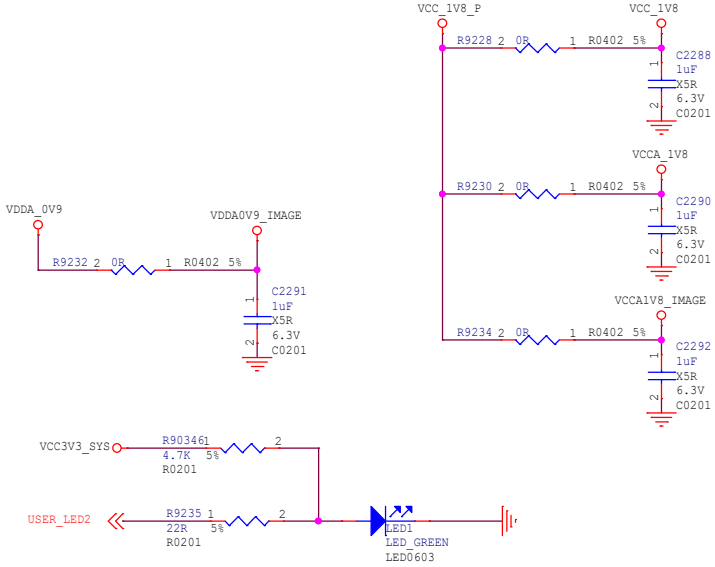
PMIC RK817 Management

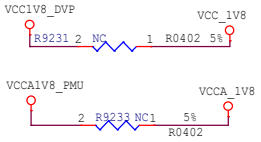


Size A3	Title: ROCK3 Compute Module		REV V1.1
	Page Name: Power_Part1_PMIC		
Date: Thursday, January 06, 2022	Sheet 21 of 25		

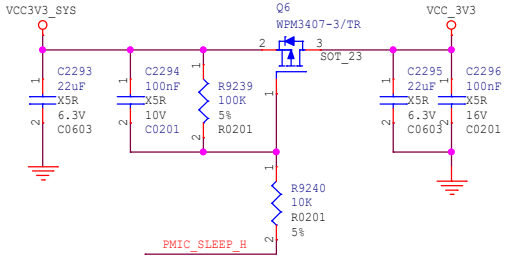


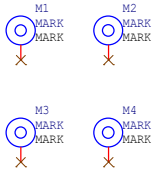




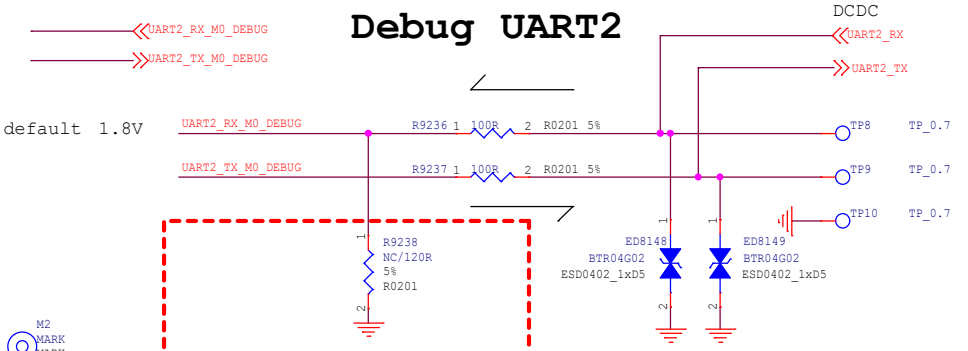


VCC_3V3 (Power OFF under SLEEP)





Debug UART2



Size B	Title: ROCK3 Compute Module	REV V1.1
	Page Name: Power_IN-Debug UART	
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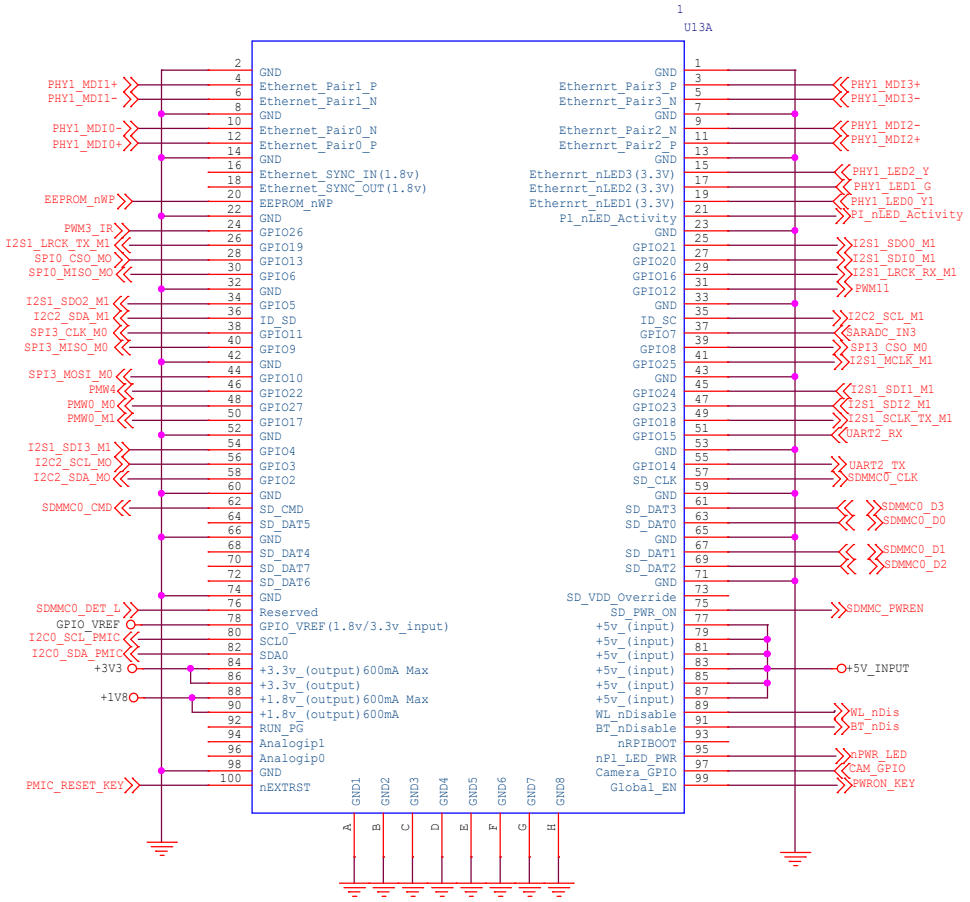
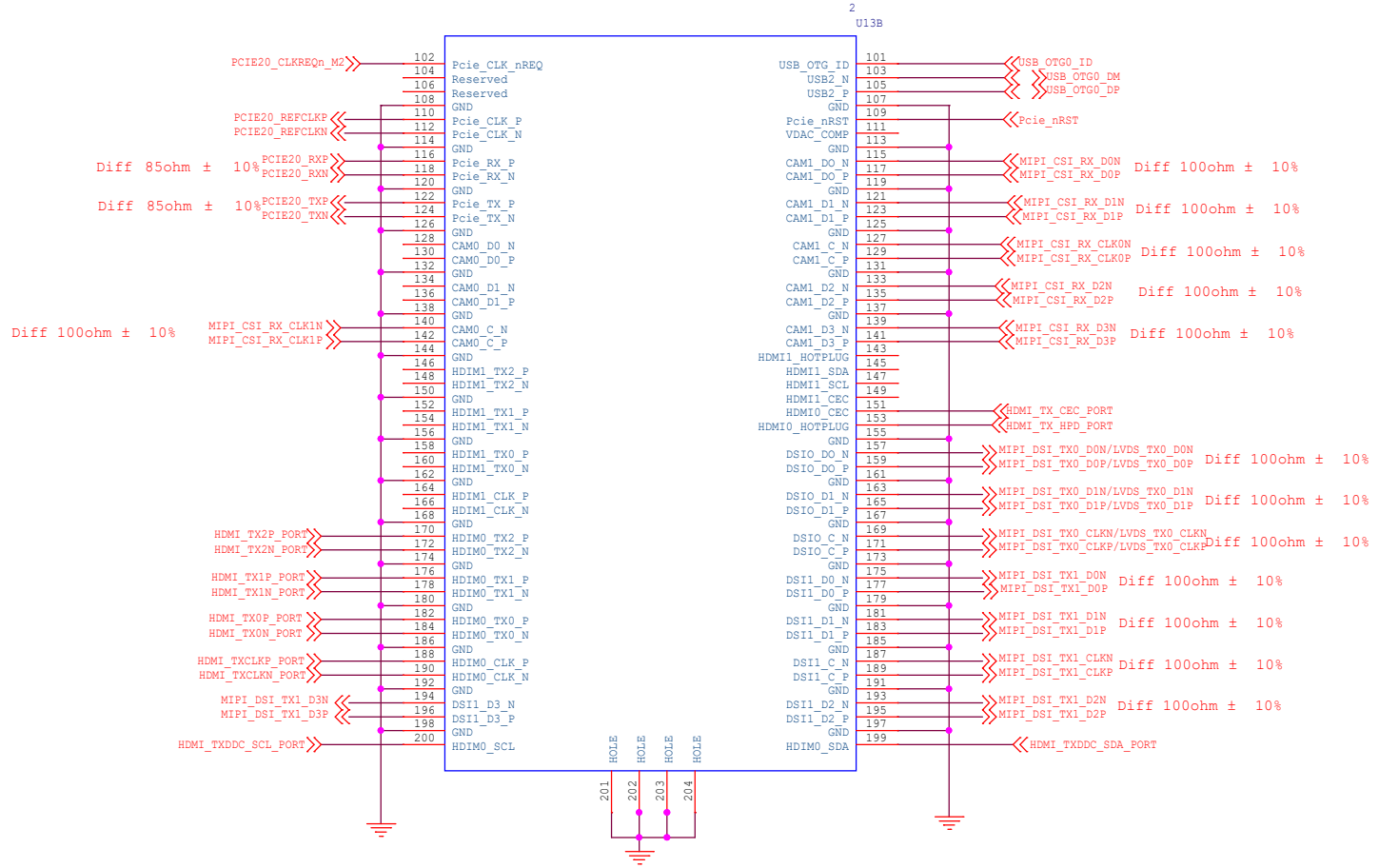


Size: B	Title: ROCK3 Compute Module	REV: V1.1
	Page Name: GPIO+VCC_Connector	
Date: Thursday, January 06, 2022	Sheet 23 of 25	



Size B	Title: ROCK3 Compute Module	REV V1.1
	Page Name: High Speed Serial_Connector	
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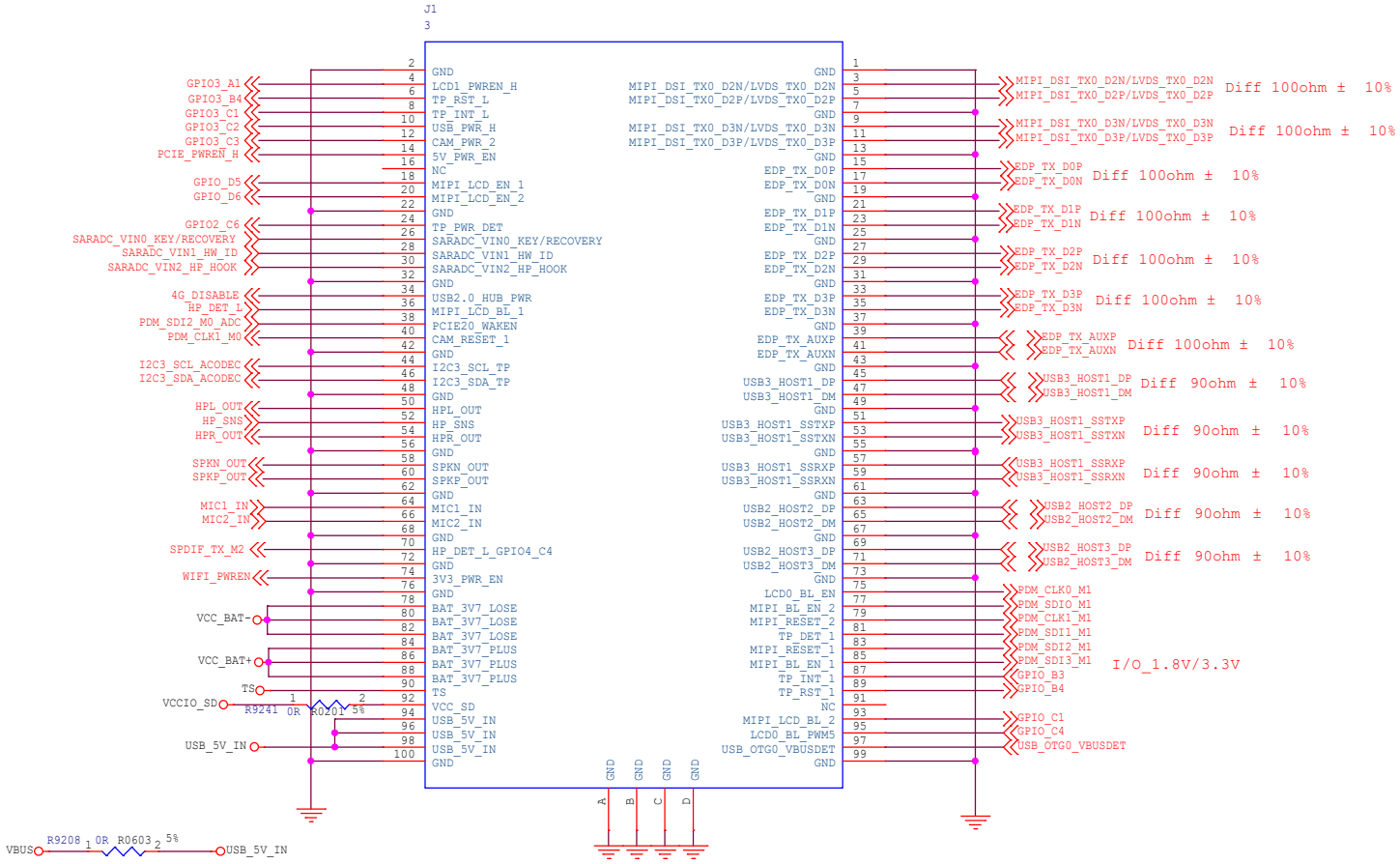

Size: B	Title: ROCK3 Compute Module	REV: V1.1
	Page Name: IO_Connector	
Date: Thursday, January 06, 2022	Sheet 25 of 25	