


# Tablet Schematics For RK3566

## **RK\_TABLET\_RK3566\_LP4D200P132SD6\_V1.0**

### **Main Functions Introduction**

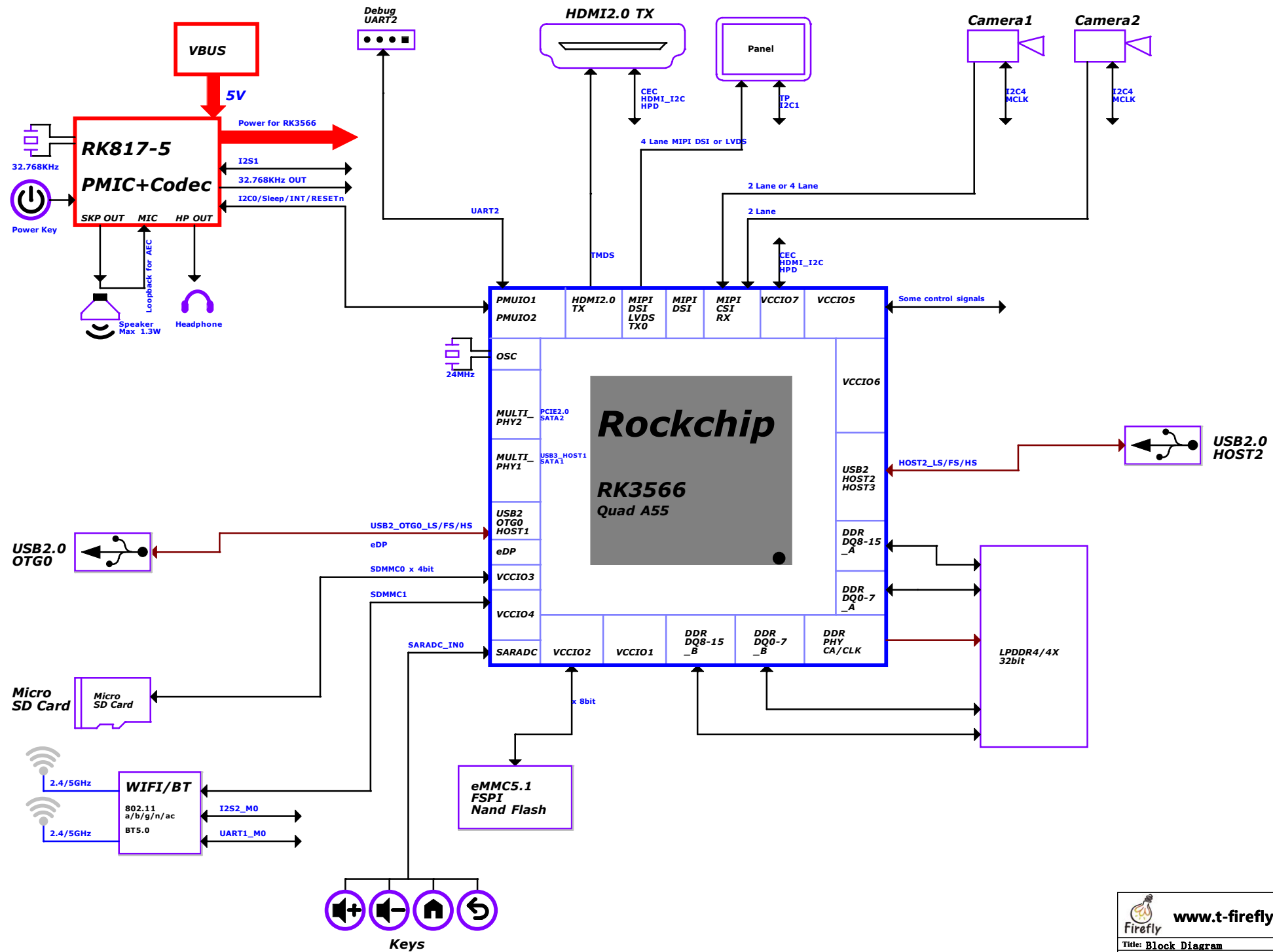
- 1) PMIC: RK817-5+Charger+DiscretePower
- 2) RAM: LPDDR4 1x32Bit(Default:2GB)
- 3) ROM: eMMC5.1(Default:16GB),Option Nand Flash
- 4) Support: Micro SD Card3.0
- 5) Support: 1 x USB2.0 OTG
- 6) Support: 4Lanes MIPI CSI Camera(Max 8M) or 2Lane+2Lane MIPI CSI Camera
- 7) Support: HDMI2.0 TX
- 8) Support: 4Lanes MIPI DS Touch Connector
- 9) Support: a/b/g/n/ac 2X2 WIFI
- 10) Support: Headphone output and Speaker out(1.3W@8ohm)
- 11) Support: Gyroscope-sensor G-sensor M-sensor PS-sensor
- 12) Support: Array Key(VOL+,VOL)

 <b>Firefly</b>	<b>www.t-firefly.com</b>
<b>Title: Cover Page</b>	
<b>File: ROC-3566-PC</b>	REV: V0.1
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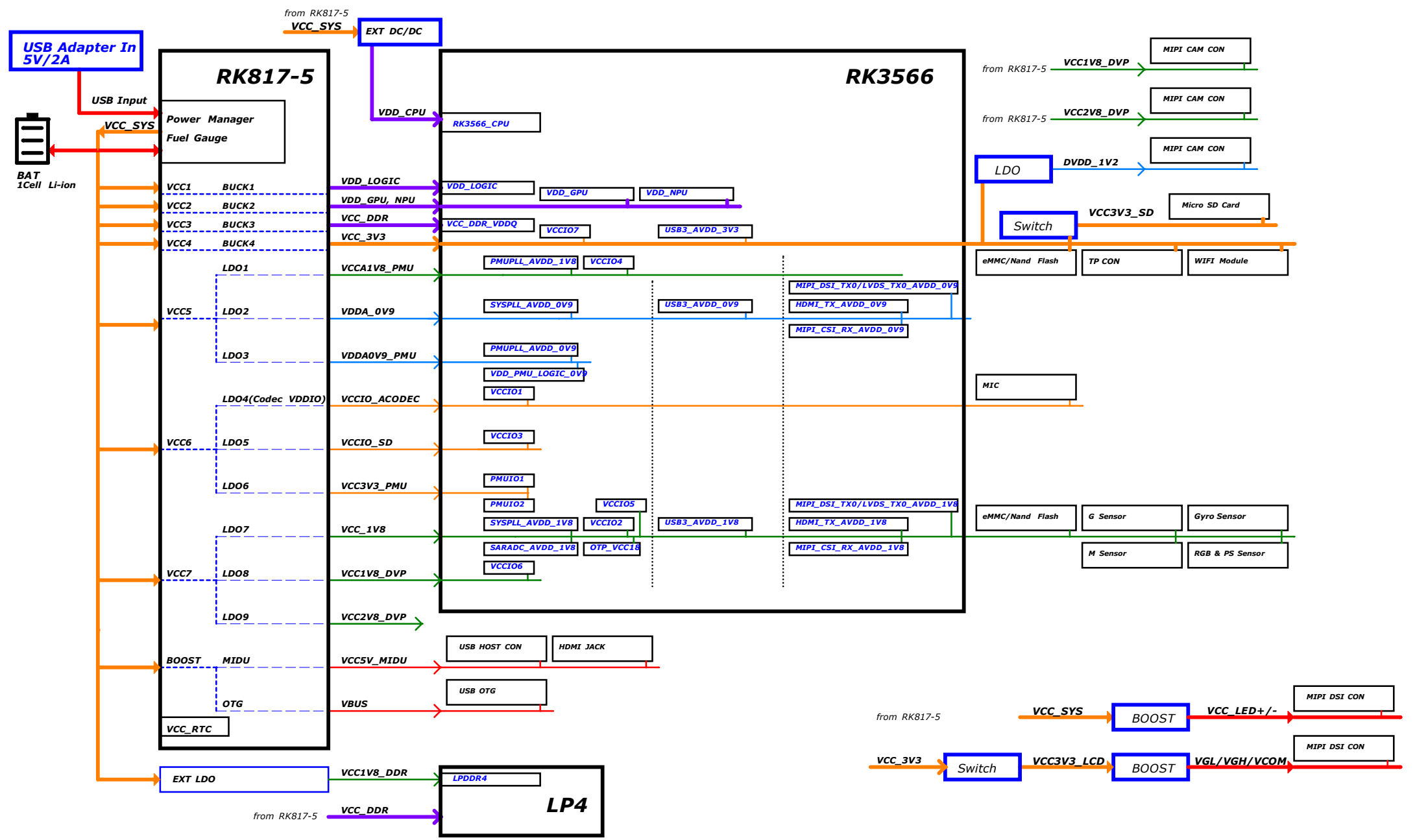




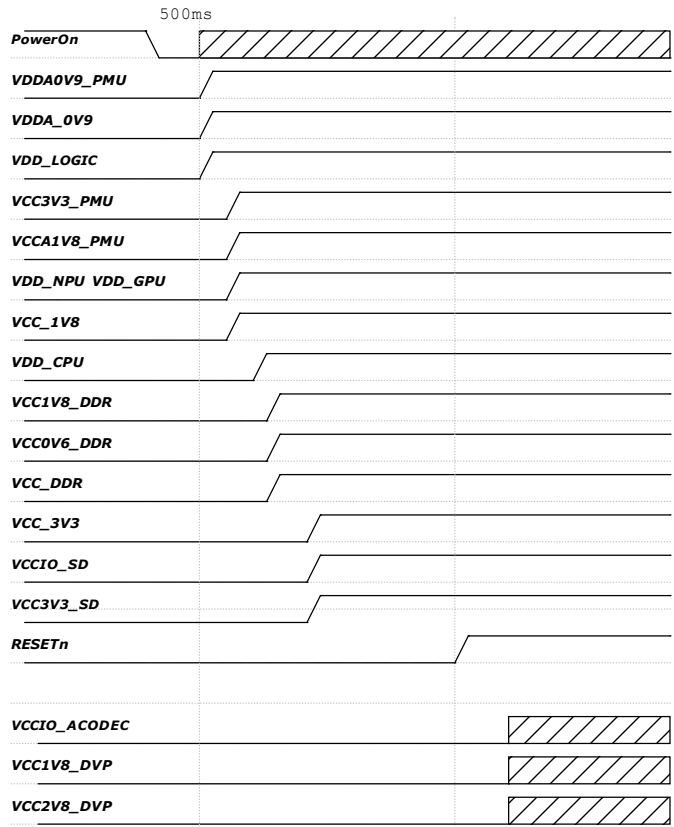
# RK3566 Ref Block Diagram



# Power Diagram



# Power Sequence & Power Path assignment




Power Source	PMIC Channel	Supply Limit	Power Supply Name	Time Slot	Default Voltage	Work Status	Sleep Status
VCC_SYS	RK817-5_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	ON
VCC_SYS	RK817-5_BUCK2	2.5A	VDD_NPU,VDD_GPU	Slot:2	0.9V	ON	OFF
VCC_SYS	RK817-5_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	ON
VCC_SYS	RK817-5_BUCK4	1.5A	VCC_3V3	Slot:4	3.3V	ON	OFF
VCC_SYS	RK817-5_LDO1	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	ON
	RK817-5_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	OFF
	RK817-5_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	ON
VCC_SYS	RK817-5_LDO4	0.4A	VCCIO_ACODEC	N/A	1.8V	ON	OFF
	RK817-5_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	OFF
	RK817-5_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	ON
VCC_SYS	RK817-5_LDO7	0.4A	VCC_1V8	Slot:2	1.8V	ON	OFF
	RK817-5_LDO8	0.4A	VCC1V8_DVP	N/A	1.8V	ON	OFF
	RK817-5_LDO9	0.4A	VCC2V8_DVP	N/A	2.8V	ON	OFF
VCC_BAT	RK817-5_RESETh			Slot:4+5			
VCC_BAT	RK817-5_BOOST RK817-5_OTG	1.5A	VCC5V_MIDU VBUS	N/A	5.0V	ON	OFF
VCC_3V3	Switch		VCC3V3_SD	Slot:4	3.3V	ON	OFF
VCC_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	OFF

## IO Power Domain Map

**Refer to the actual design!**

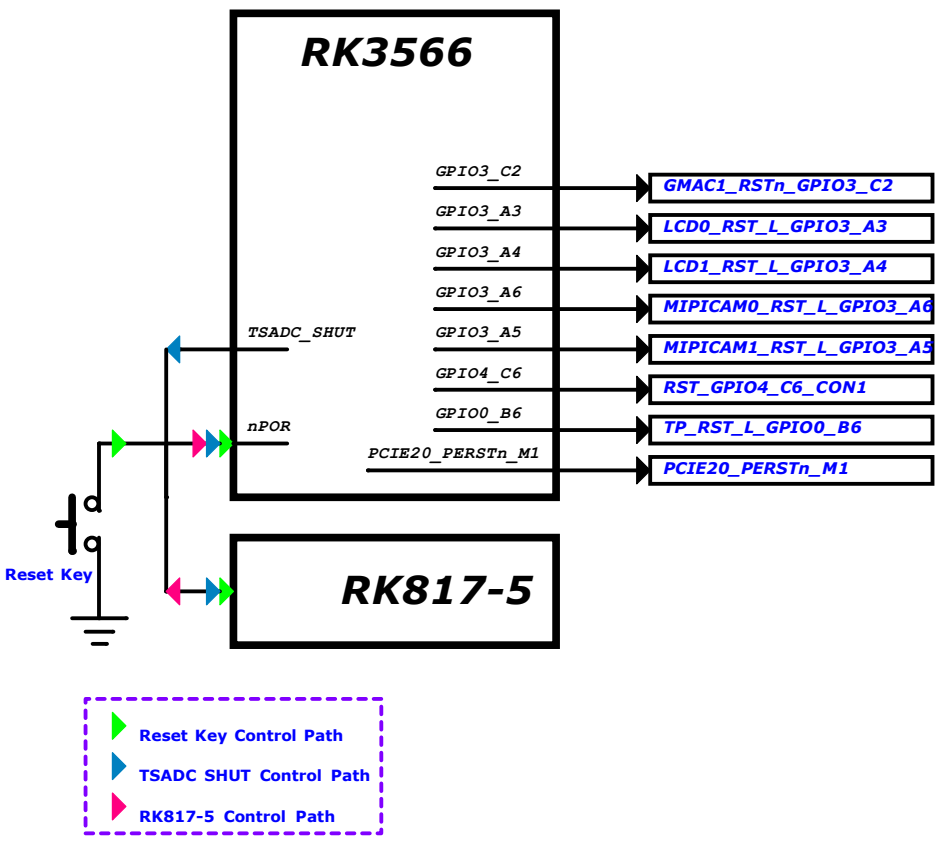
IO Domain	Pin Num	Support IO Voltage		Assignment IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	1P16	YES	NO	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	1N15	YES	YES	VCC3V3_PMU	VCC3V3_PMU	3.3V	
VCCIO1	1D13	YES	YES	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	1C13	YES	YES	VCCIO_FLASH	VCC_1V8	1.8V	FLASH_VOL_SEL = 1 --> VCCIO_FLASH = 1.8V
VCCIO3	1F17	YES	YES	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	1E16	YES	YES	VCCIO4	VCCA1V8_PMU	1.8V	
VCCIO5	1N5 1N6	YES	YES	VCCIO5	VCC_1V8	1.8V	
VCCIO6	1L4 1L5	YES	YES	VCCIO6	VCC1V8_DVP	1.8V	
VCCIO7	1N8	YES	YES	VCCIO7	VCC_3V3	3.3V	



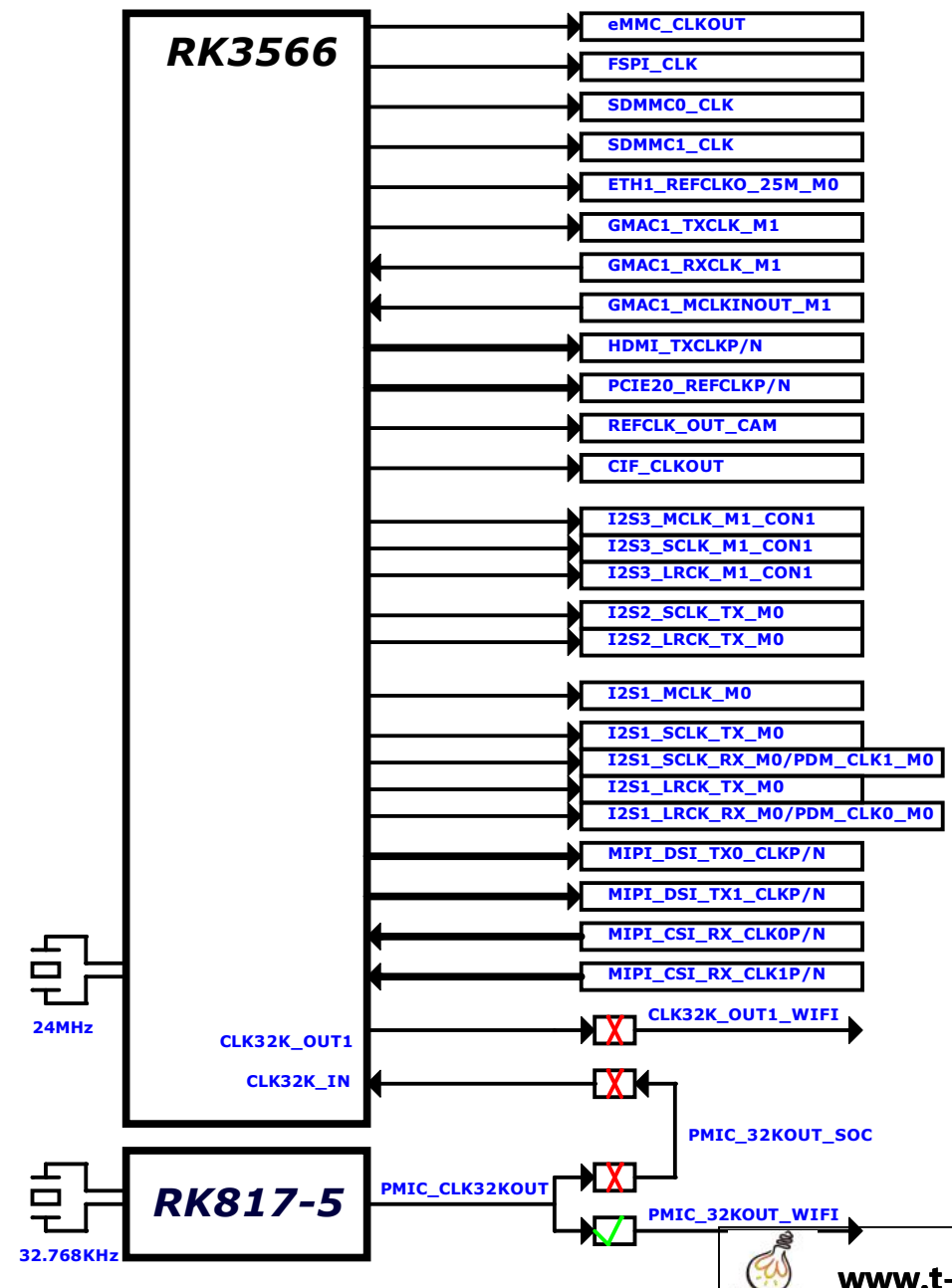
**www.t-firefly.com**

Title: Power Sequence/IO Domain Map  
 File: ROC-3566-PC  
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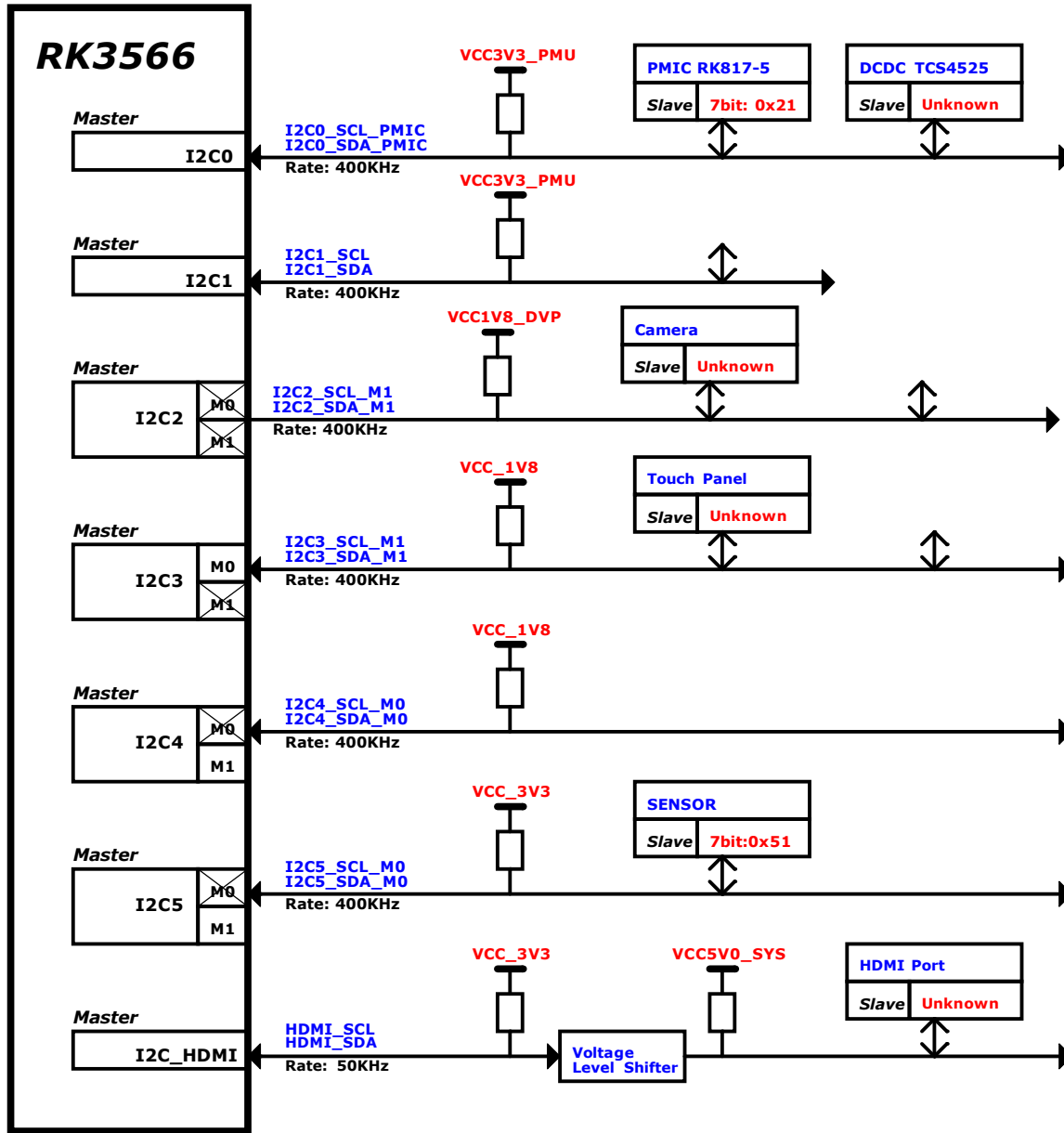
# RESET Signal MAP



# Clock Map

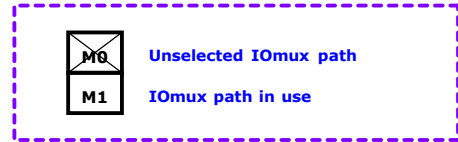
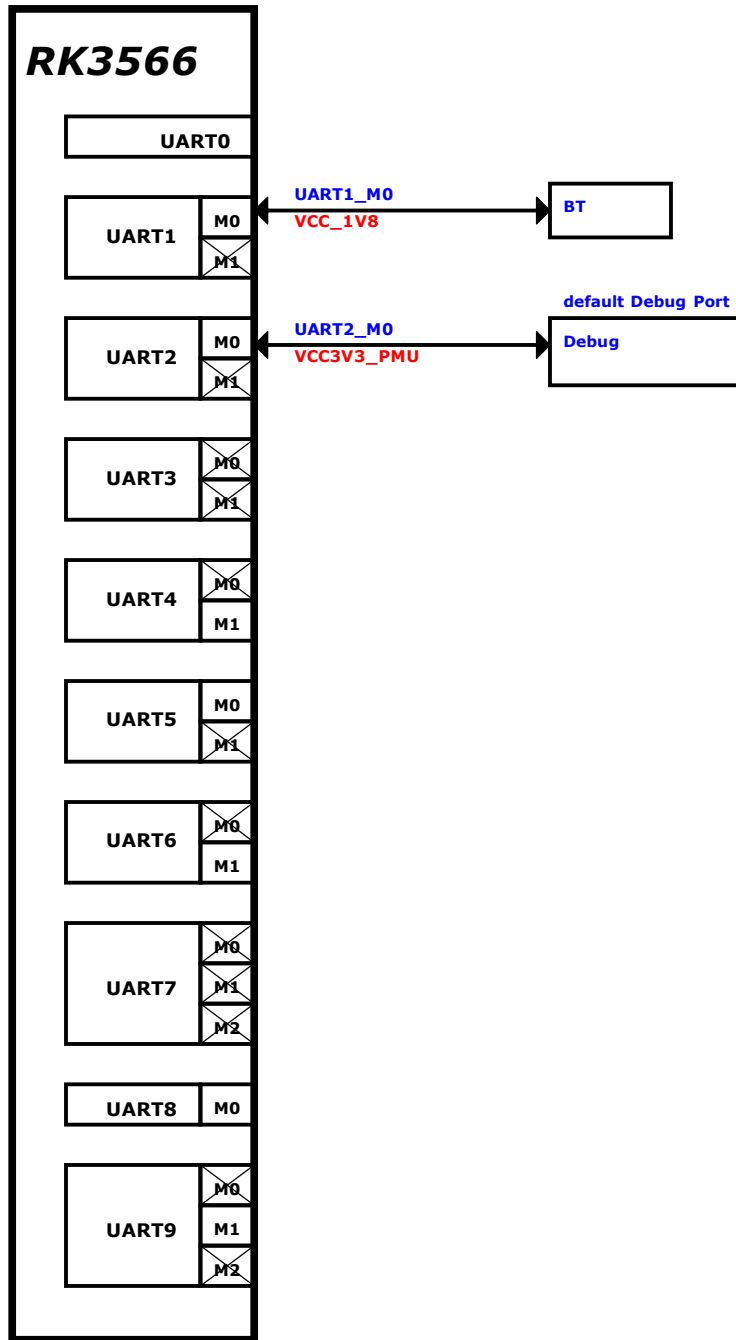



# I2C MAP





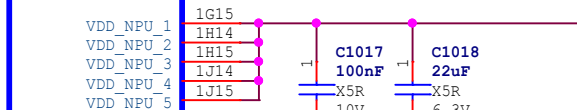
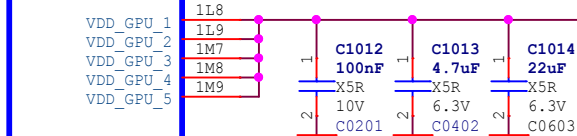
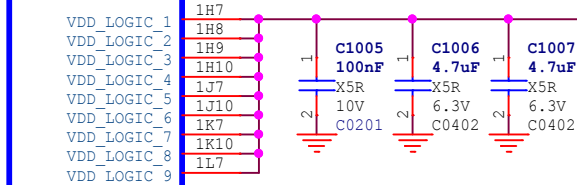
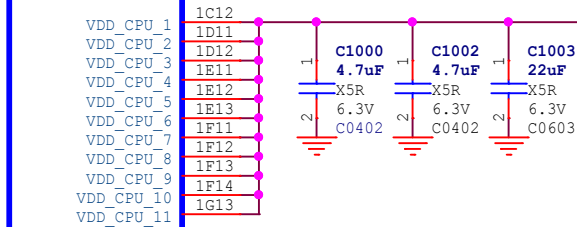
# UART MAP



		<a href="http://www.t-firefly.com">www.t-firefly.com</a>
<b>Title: UART Map</b>		
<b>File: ROC-3566-PC</b>		REV: V0.1
Create Date: Monday, August 31, 2020	Page Num: 9	
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# RK3566\_ABCDE (Power&GND)

U1000A

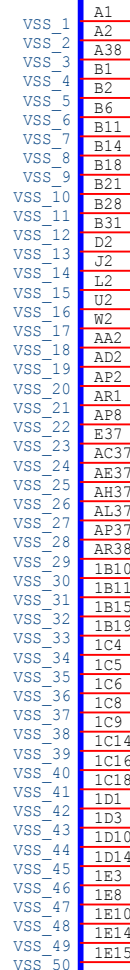


RK3566  
BGA565\_15R50X14R40X0R90

Caps should be placed under the U1000 package

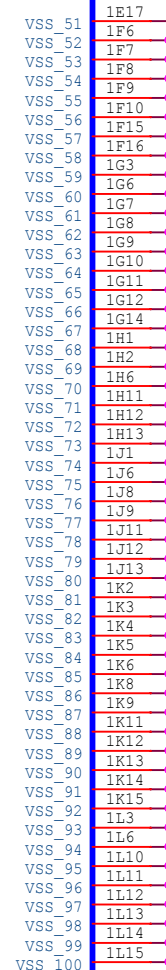
Caps should be placed close to the U1000 package

U1000B



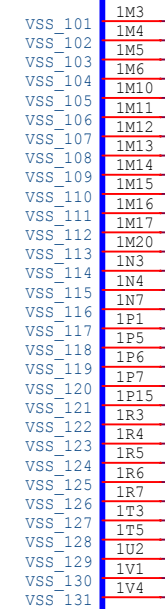
RK3566  
BGA565\_15R50X14R40X0R90

U1000C



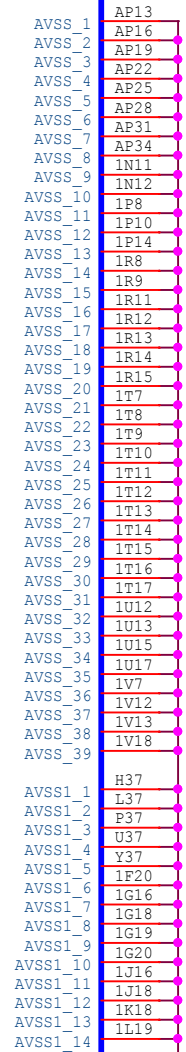
RK3566  
BGA565\_15R50X14R40X0R90

U1000D



RK3566  
BGA565\_15R5x14R4x0R90

U1000E



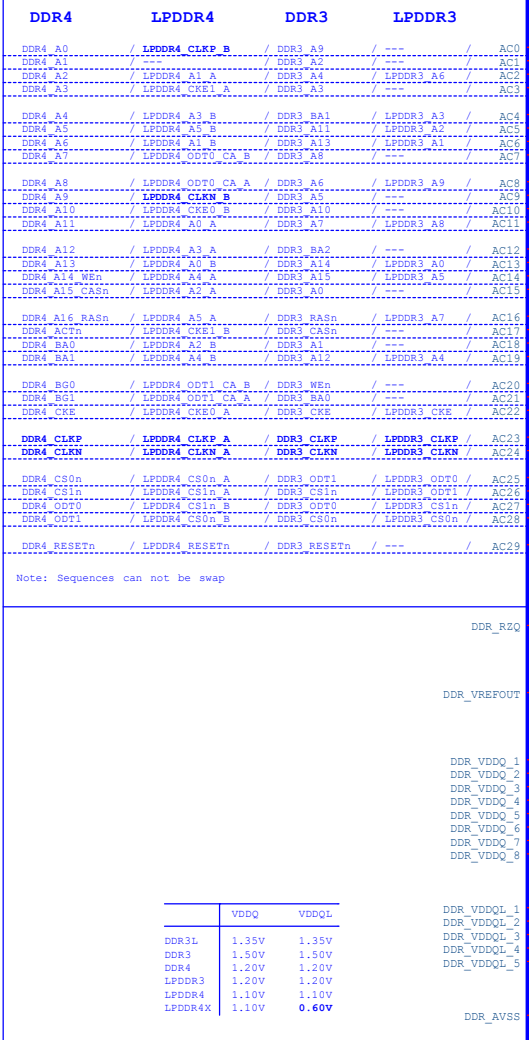
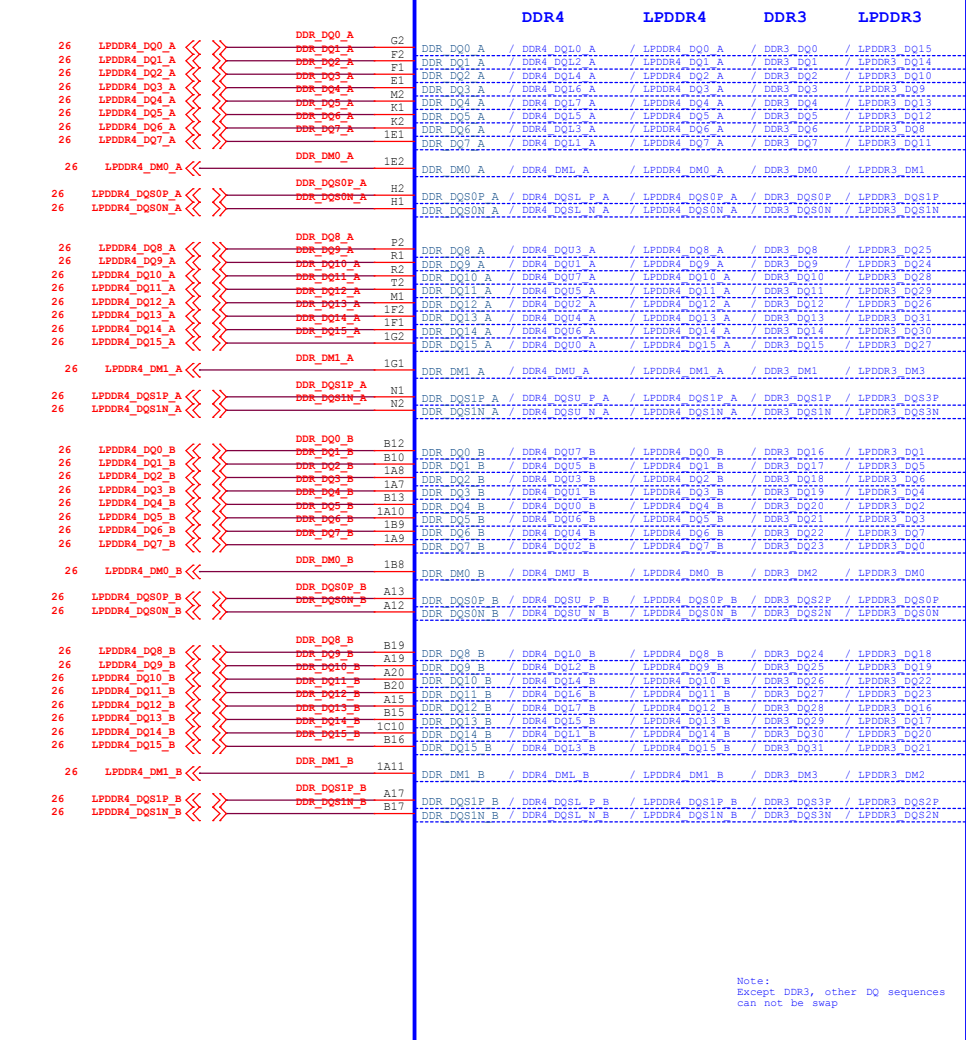
RK3566  
BGA565\_15R50X14R40X0R90



Title: RK3566 Power/GND	
File: ROC-3566-PC	REV: V0.1
Create Date: Monday, March 30, 2020	Page Num: 10
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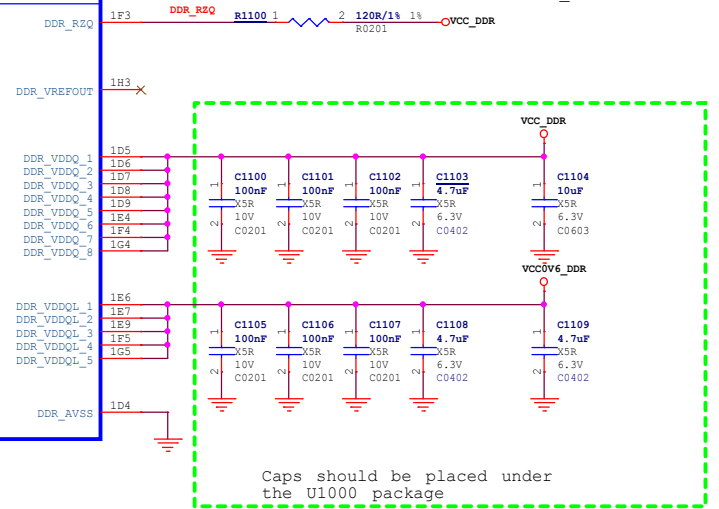
# RK3566\_F (DDR PHY)

U1000F



Note: Sequences can not be swap


USE LP4/LP4X, R1100 PULL UP TO VCC\_DDR



	VDDQ	VDDQL
DDR3L	1.35V	1.35V
DDR4	1.50V	1.50V
DDR4	1.20V	1.20V
LPDDR3	1.20V	1.20V
LPDDR4	1.10V	1.10V
LPDDR4X	1.10V	0.60V

Note: Except DDR3, other DQ sequences can not be swap

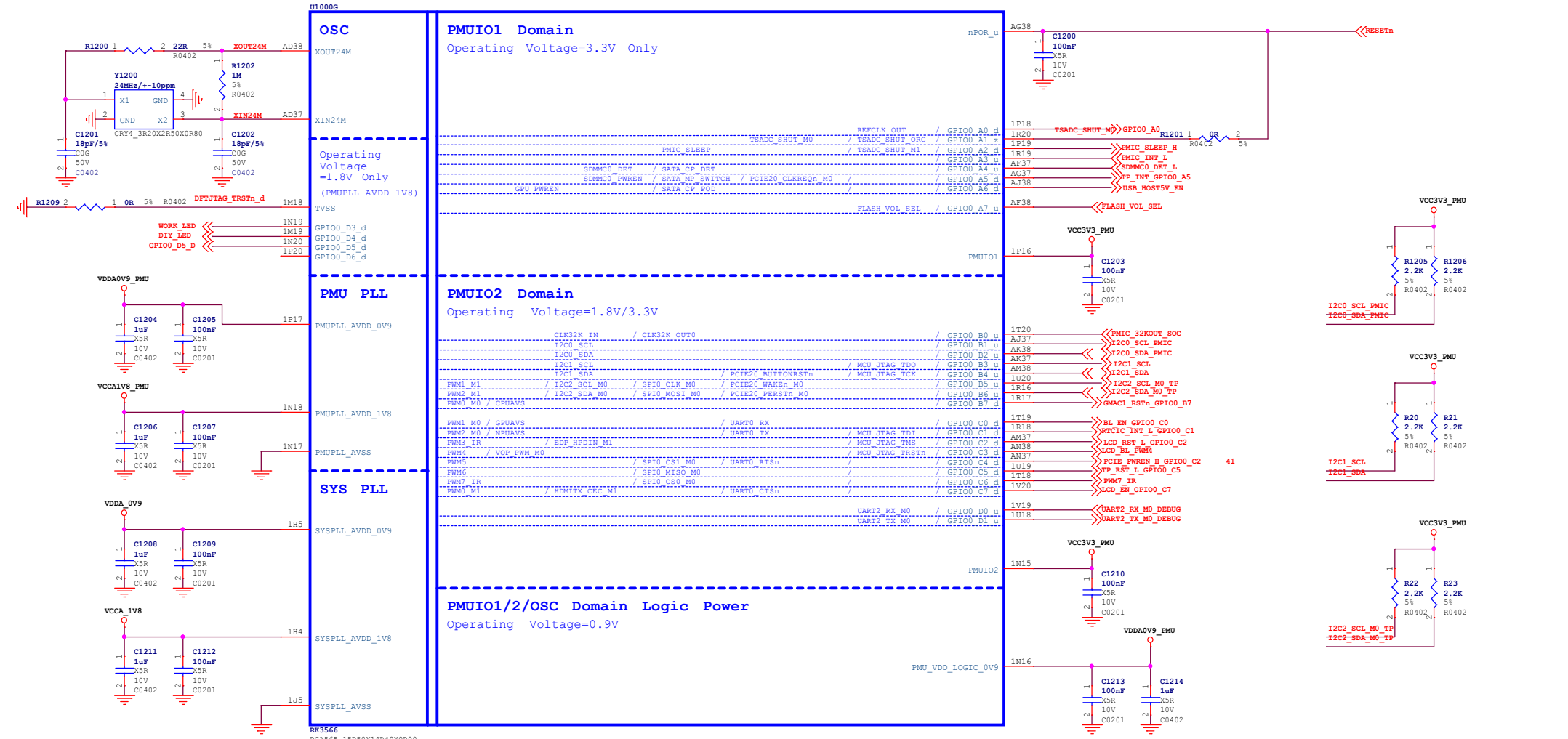
Caps should be placed under the U1000 package


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**Title: RK3566 DDR PHY**  
**File: ROC-3566-PC**
REV: V0.1

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# RK3566\_G (OSC/PLL/PMUIO1/2)



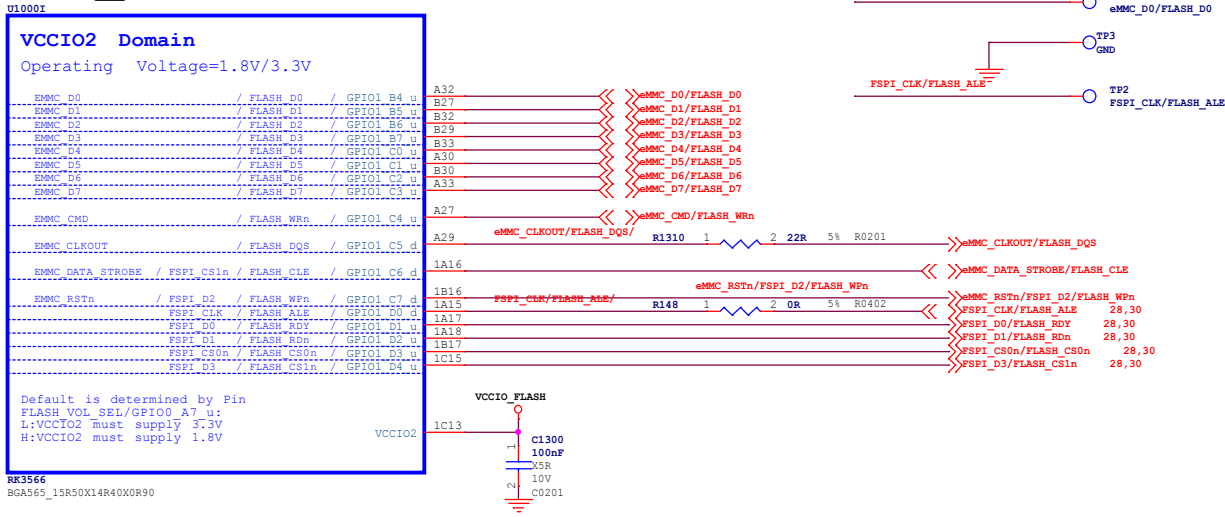
**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package.  
Other caps should be placed close to the U1000 package



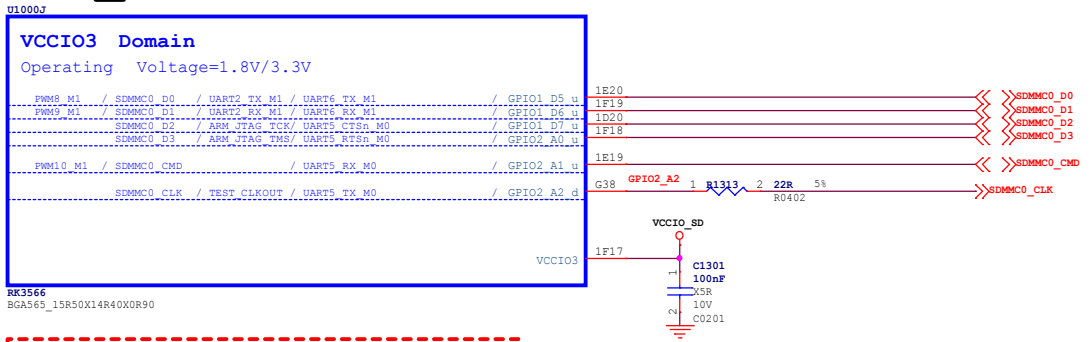
**www.t-firefly.com**

<b>Title: RK3566_OSC/PLL/PMUIO</b>	
<b>File: ROC-3566-PC</b>	REV: V0.1
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# RK3566\_I (VCCIO2 Domain)



# RK3566\_J (VCCIO3 Domain)



**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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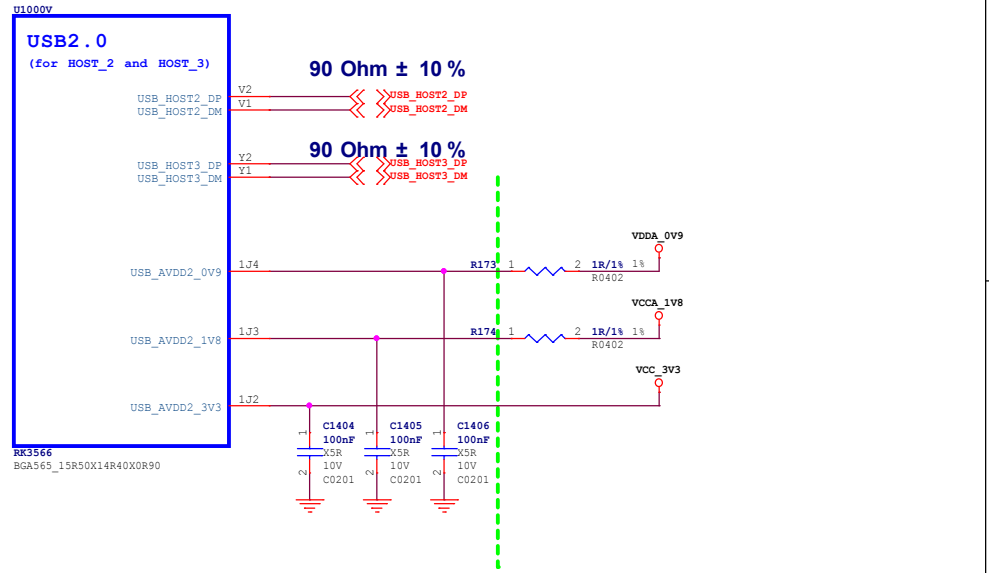
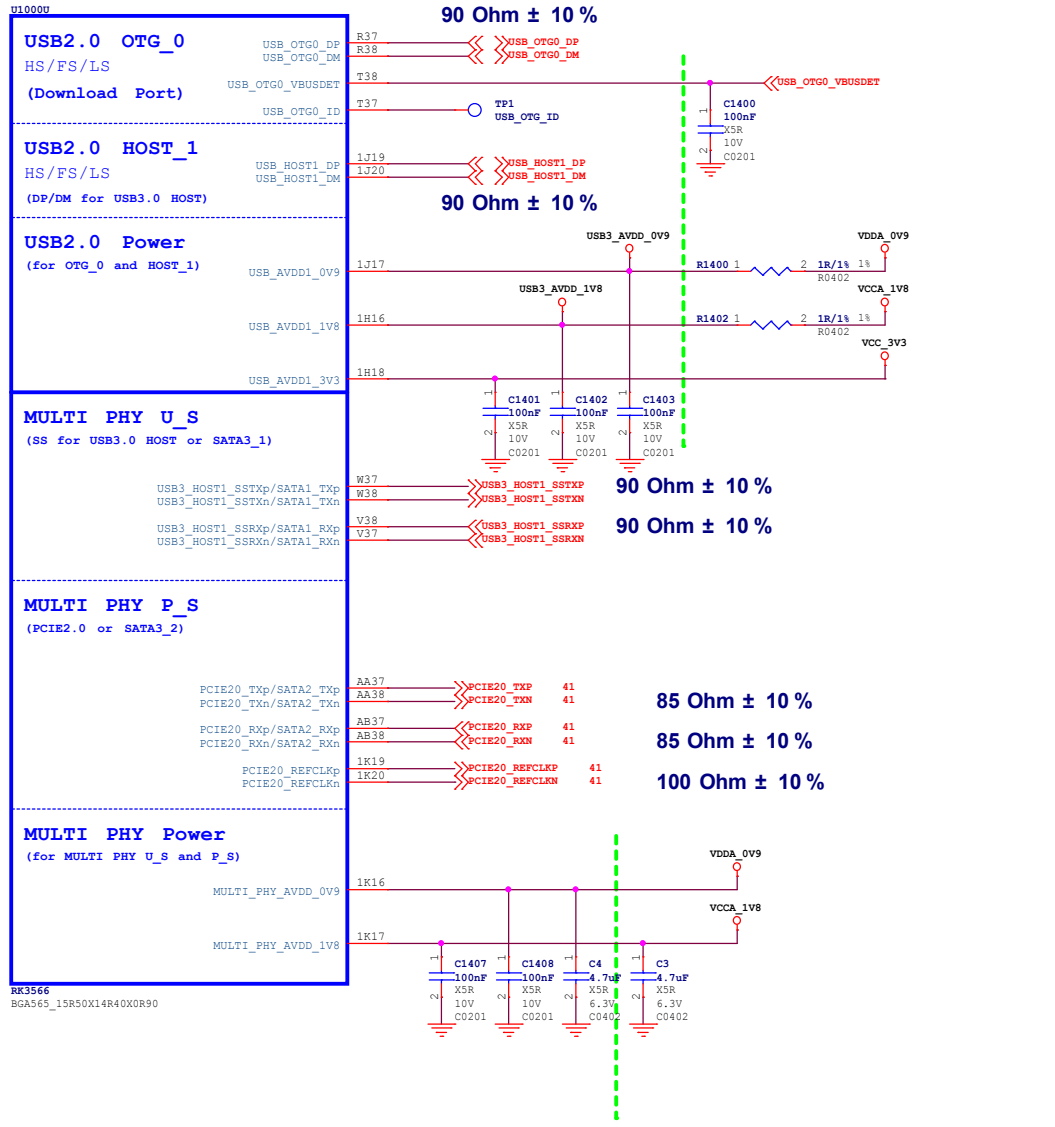
**Title: RK3566 Flash/SD Controller**

**File: ROC-3566-PC** REV: V0.1

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# RK3566\_U (USB3.0/SATA/QSGMII/PCIe2.0 x1)

# RK3566\_V (USB2.0 HOST)



**Note:**  
 Caps of between dashed green lines and U1000 should be placed under the U1000 package.  
 Other caps should be placed close to the U1000 package.

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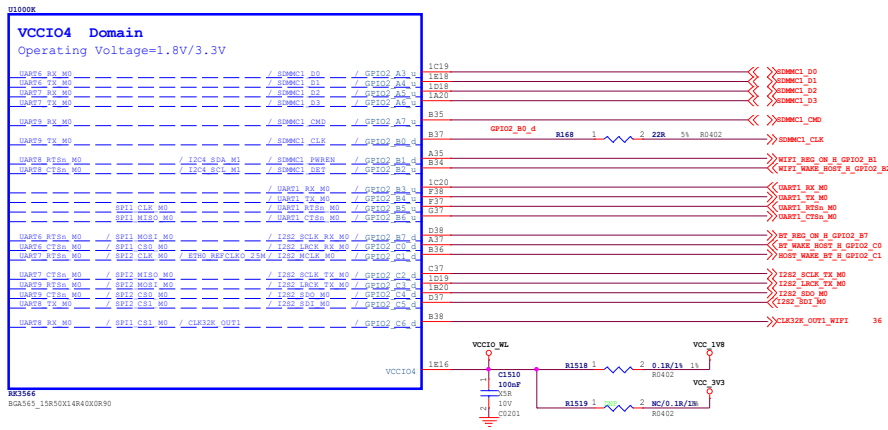
 **www.t-firefly.com**

**Title:** RK3566\_USB/PCIe/SATA\_PHY  
**File:** ROC-3566-PC  
**REV:** V0.1

**Create Date:** Monday, March 30, 2020  
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# RK3566\_K (VCCIO4 Domain)



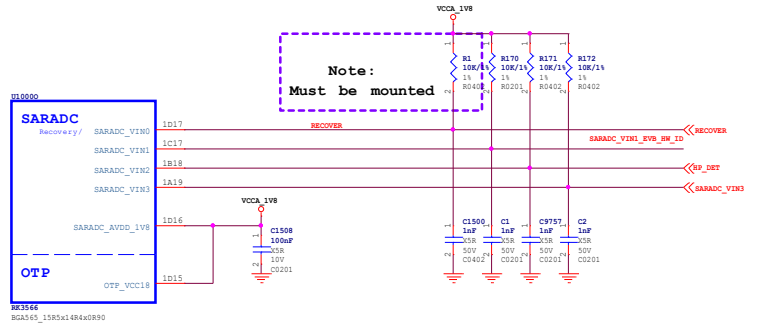
For WIFI  
For BT  
For BT

# RK3566\_N (VCCIO7 Domain)



**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package

# RK3566\_O (SARADC/OTP)



**Note:**  
Must be mounted

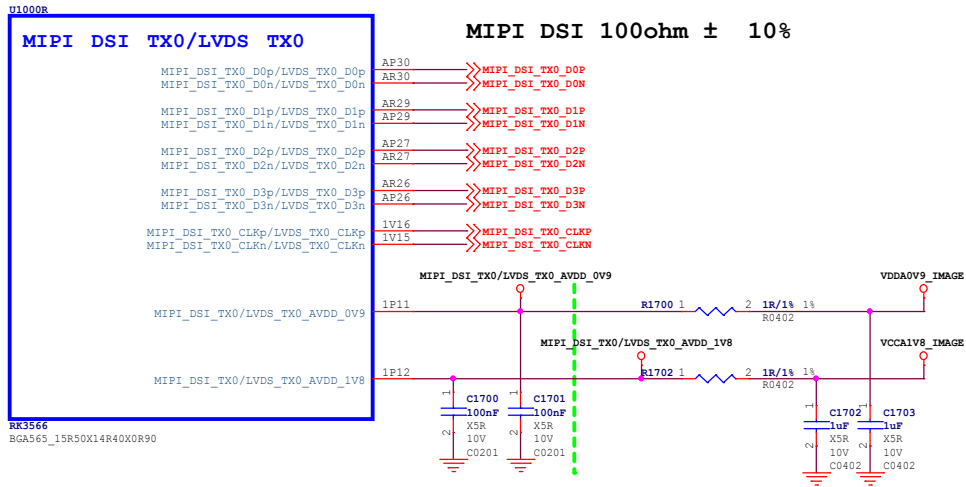
SARADC_VINI_EVB_HW_ID	Up	Down	ADC	
EVB1	10K	20K	1023	1.8V
EVB2	20K	100K	852	1.5V
EVB3	18K	36K	681	1.2V
EVB4	51K	51K	512	0.9V
EVB5	36K	18K	340	0.6V
EVB6	100K	20K	170	0.3V
EVB7	20K	10K	0	0V
EVB8				



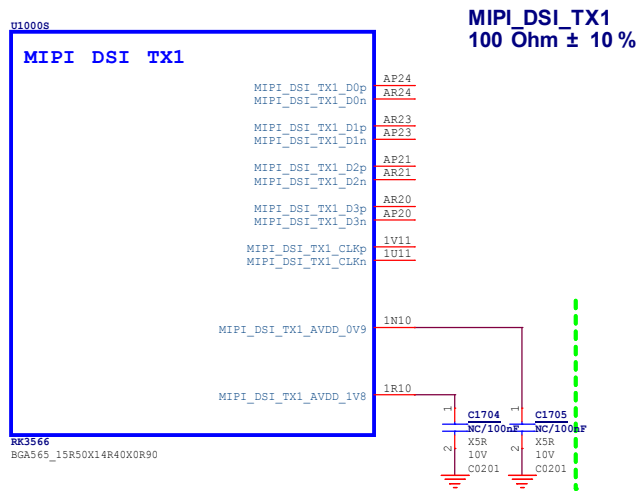




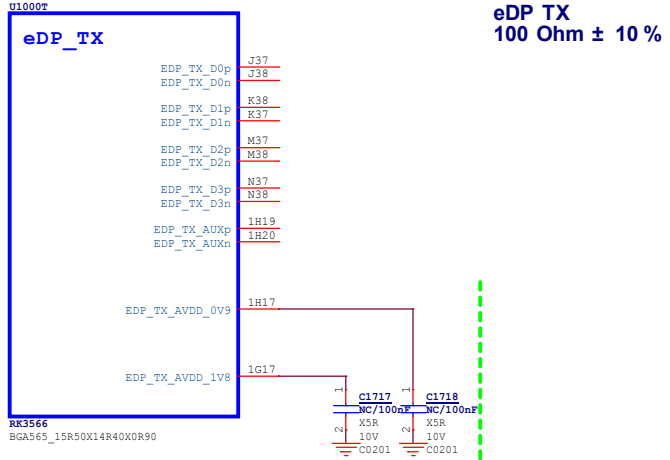
# RK3566\_R (MIPI\_DSI\_TX0/LVDS\_TX0)



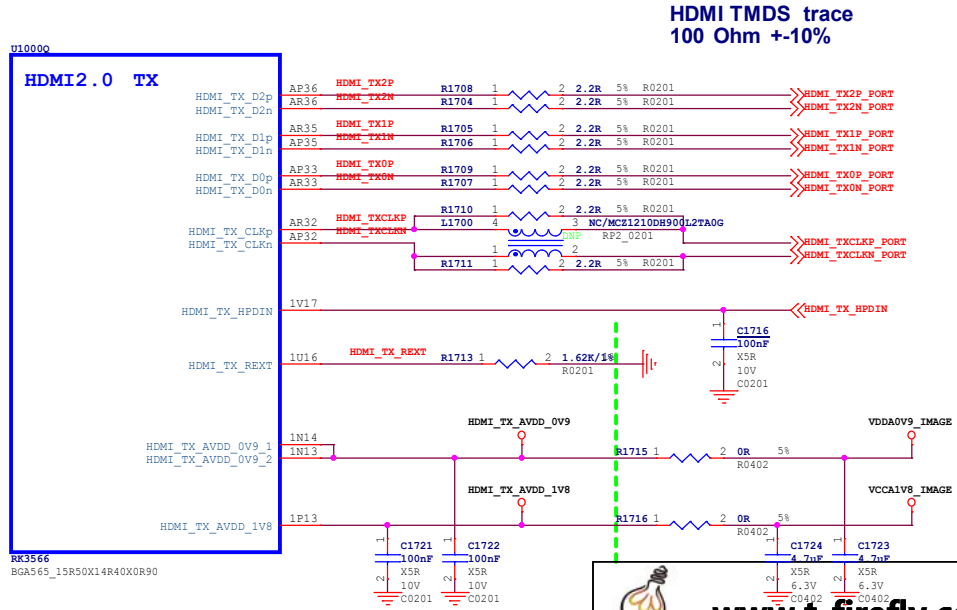
# RK3566\_S (MIPI\_DSI\_TX1)



# RK3566\_T (eDP/DP TX)



# RK3566\_Q (HDMI2.0 TX)



Boxed capacitors should be placed under the U1000 package.  
Other caps should be placed close to the U1000 package

**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package.  
Other caps should be placed close to the U1000 package

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**Title: RK3566\_V0 Interface 1**

**File: ROC-3566-PC**

**Create Date: Monday, March 30, 2020**

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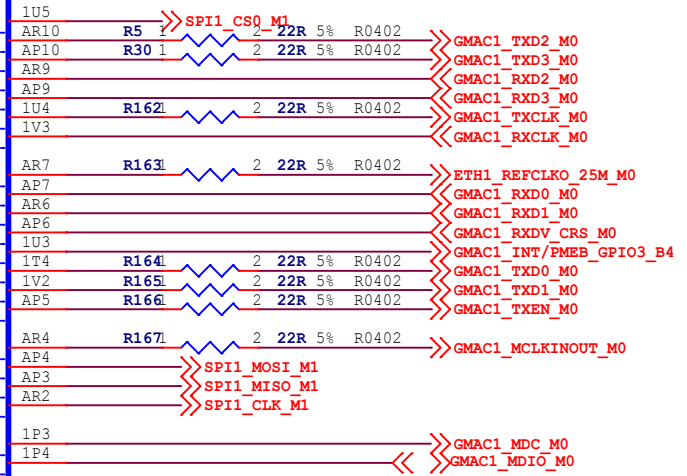
# RK3566\_L (VCCIO5 Domain)

U1000L

## VCCIO5 Domain

Operating Voltage=1.8V/3.3V

VOP BT1120 D0	/ SPI1 CS0 M1			/ SDMMC2 D0 M1	/ GPIO3 A1 d
VOP BT1120 D1		/ GMAC1 TXD2 M0	/ I2S3 MCLK M0	/ SDMMC2 D1 M1	/ GPIO3 A2 d
VOP BT1120 D2		/ GMAC1 TXD3 M0	/ I2S3 SCLK M0	/ SDMMC2 D2 M1	/ GPIO3 A3 d
VOP BT1120 D3		/ GMAC1 RXD2 M0	/ I2S3 LRCK M0	/ SDMMC2 D3 M1	/ GPIO3 A4 d
VOP BT1120 D4		/ GMAC1 RXD3 M0	/ I2S3 SDO M0	/ SDMMC2 CMD M1	/ GPIO3 A5 d
VOP BT1120 CLK		/ GMAC1 TXCLK M0	/ I2S3 SDI M0	/ SDMMC2 CLK M1	/ GPIO3 A6 d
VOP BT1120 D5		/ GMAC1 RXCLK M0		/ SDMMC2 DET M1	/ GPIO3 A7 d
VOP BT1120 D6		/ ETH1 REFCLK0 25M M0		/ SDMMC2 PWREN M1	/ GPIO3 B0 d
PWM8 M0	/ VOP BT1120 D7	/ GMAC1 RXD0 M0	/ UART4 RX M1		/ GPIO3 B1 d
PWM9 M0	/ VOP BT1120 D8	/ GMAC1 RXD1 M0	/ UART4 TX M1		/ GPIO3 B2 d
	/ VOP BT1120 D9	/ I2C5 SCL M0	/ GMAC1 RXDV CRS M0	/ PDM SDI0 M2	/ GPIO3 B3 d
	/ VOP BT1120 D10	/ I2C5 SDA M0	/ GMAC1 RXER M0	/ PDM SDI1 M2	/ GPIO3 B4 d
PWM10 M0	/ VOP BT1120 D11	/ I2C3 SCL M1	/ GMAC1 TXD0 M0		/ GPIO3 B5 d
PWM11 IR M0	/ VOP BT1120 D12	/ I2C3 SDA M1	/ GMAC1 TXD1 M0		/ GPIO3 B6 d
PWM12 M0		/ GMAC1 TXEN M0	/ UART3 TX M1	/ PDM SDI2 M2	/ GPIO3 B7 d
PWM13 M0		/ GMAC1 MCLKINOUT M0	/ UART3 RX M1	/ PDM SDI3 M2	/ GPIO3 C0 d
	/ VOP BT1120 D13	/ SPI1 MOSI M1	/ PCIE20 PERStn M1	/ I2S1 SDO2 M2	/ GPIO3 C1 d
	/ VOP BT1120 D14	/ SPI1 MISO M1	/ UART5 TX M1	/ I2S1 SDO3 M2	/ GPIO3 C2 d
	/ VOP BT1120 D15	/ SPI1 CLK M1	/ UART5 RX M1	/ I2S1 SCLK RX M2	/ GPIO3 C3 d
PWM14 M0	/ VOP PWM M1	/ GMAC1 MDC M0	/ UART7 TX M1	/ PDM CLK1 M2	/ GPIO3 C4 d
PWM15 IR M0	/ SPDIF TX M1	/ GMAC1 MDIO M0	/ UART7 RX M1	/ I2S1 LRCK RX M2	/ GPIO3 C5 d



RK3566  
BGA565\_15R50X14R40X0R90

### Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package



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# RK3566\_H (VCCIO1 Domain)

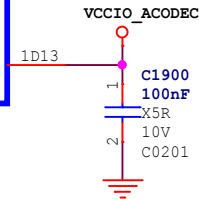
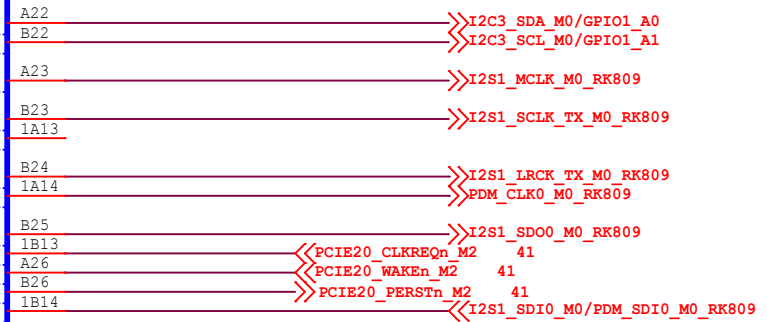
U1000H

## VCCIO1 Domain

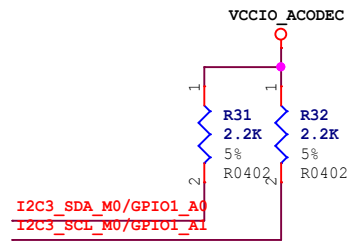
Operating Voltage=1.8V/3.3V

/ I2C3 SDA M0	/ UART3 RX M0	/ AUDIOPWM LOUT p	/ GPIO1 A0 h
/ I2C3 SCL M0	/ UART3 TX M0	/ AUDIOPWM LOUT n	/ GPIO1 A1 u
SCR_CLK	/ I2S1 MCLK M0	/ UART3 RTSn M0	/ GPIO1 A2 d
SCR_IO	/ I2S1 SCLK TX M0	/ UART3 CTSn M0	/ GPIO1 A3 d
	I2S1 SCLK RX M0	/ UART4 RX M0	/ PDM CLK1 M0
		/ SPDIF TX M0	/ GPIO1 A4 d
SCR_RST	/ I2S1 LRCK TX M0	/ UART4 RTSn M0	/ GPIO1 A5 d
	I2S1 LRCK RX M0	/ UART4 TX M0	/ PDM CLK0 M0
		/ AUDIOPWM ROUT p	/ GPIO1 A6 d
SCR_DET	/ I2S1 SDO0 M0	/ UART4 CTSn M0	/ GPIO1 A7 d
	I2S1 SDO1 M0	/ I2S1 SDI3 M0	/ PDM SDI3 M0
		/ PCIE20 CLKREqn M2	/ GPIO1 B0 d
	I2S1 SDO2 M0	/ I2S1 SDI2 M0	/ PDM SDI2 M0
		/ PCIE20 WAKEn M2	/ GPIO1 B1 d
	I2S1 SDO3 M0	/ I2S1 SDI1 M0	/ PDM SDI1 M0
		/ PCIE20 PERSTn M2	/ GPIO1 B2 d
		/ I2S1 SDI0 M0	/ PDM SDI0 M0
			/ GPIO1 B3 d

RK3566  
BGA565\_15R50X14R40X0R90

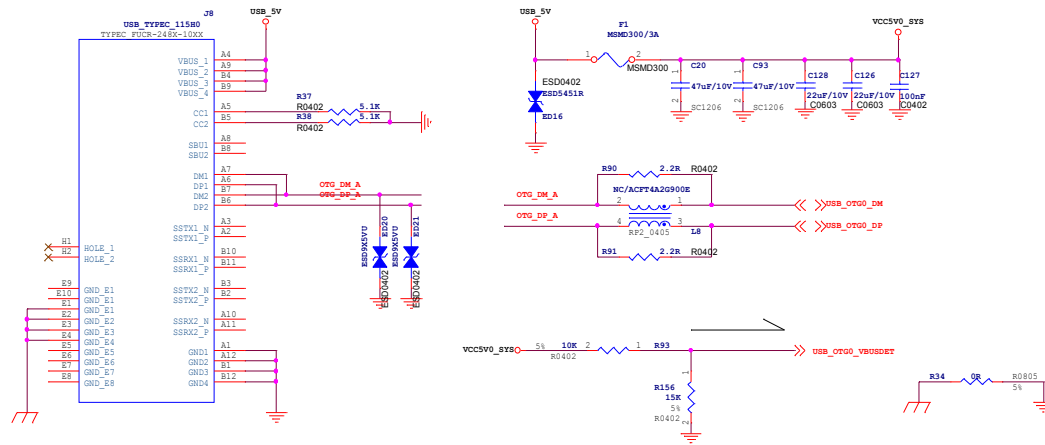


**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package

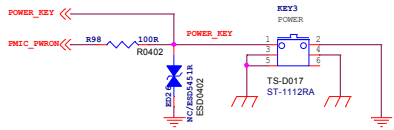


Title: RK3566 Audio Interface	
File: ROC-3566-PC	REV: V0.1
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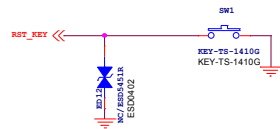
# POWER CONTROL



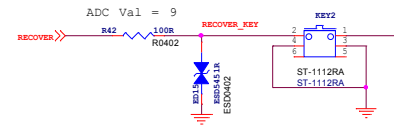
## POWER



## RESET

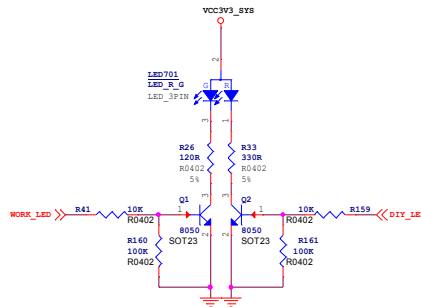
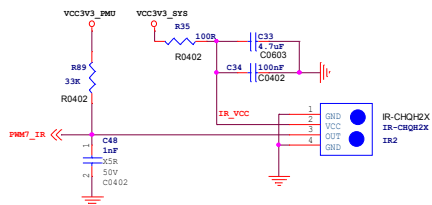


## RECOVER



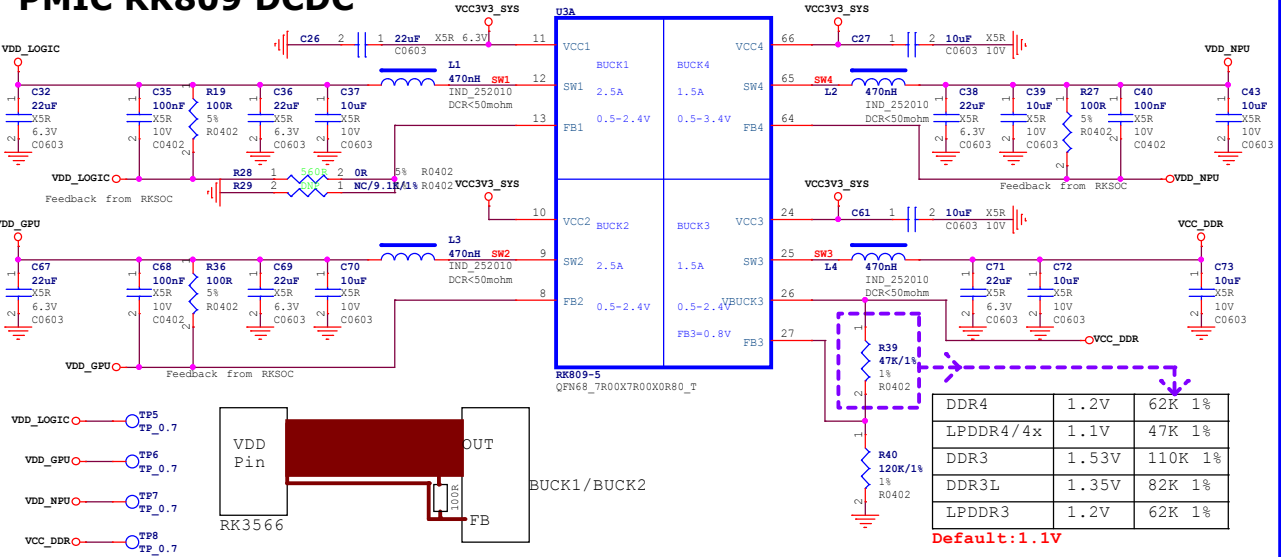
## LED DISPLAY

### IR

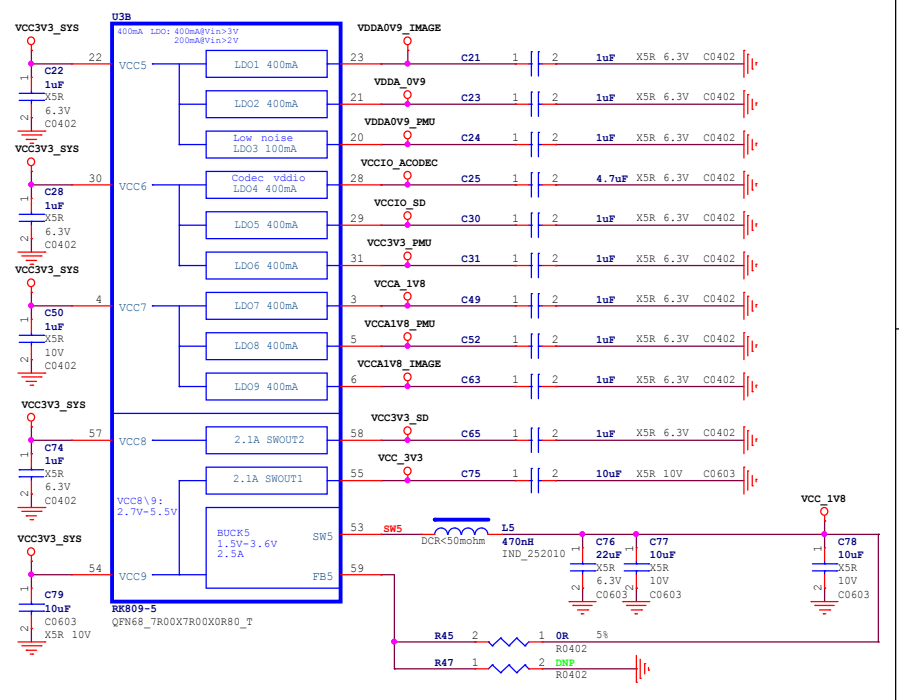


- >>>I2C0\_SCL\_PMIC
- >>>I2C0\_SDA\_PMIC
- >>>PMIC\_INT\_L
- >>>PMIC\_SLEEP\_H
- >>>PMIC\_PWRON
- >>>RESETn
- >>>PMIC\_32KOUT\_WIFI
- >>>PMIC\_32KOUT\_SOC
- >>>PCIE\_32KHZ
- >>>RST\_KEY
- >>>I2S1\_MCLK\_M0\_RK809
- >>>I2S1\_SCLK\_TX\_M0\_RK809
- >>>I2S1\_LRCK\_TX\_M0\_RK809
- >>>I2S1\_SDIO\_M0\_RK809
- >>>I2S1\_SDIO\_M0/PDM\_SDIO\_M0\_RK809
- >>>PDM\_CLK0\_M0\_RK809
- >>>HPL\_OUT
- >>>HP\_SNS
- >>>HPR\_OUT
- >>>SPKN\_OUT
- >>>SPKP\_OUT
- >>>MIC1\_IN
- >>>MIC2\_IN

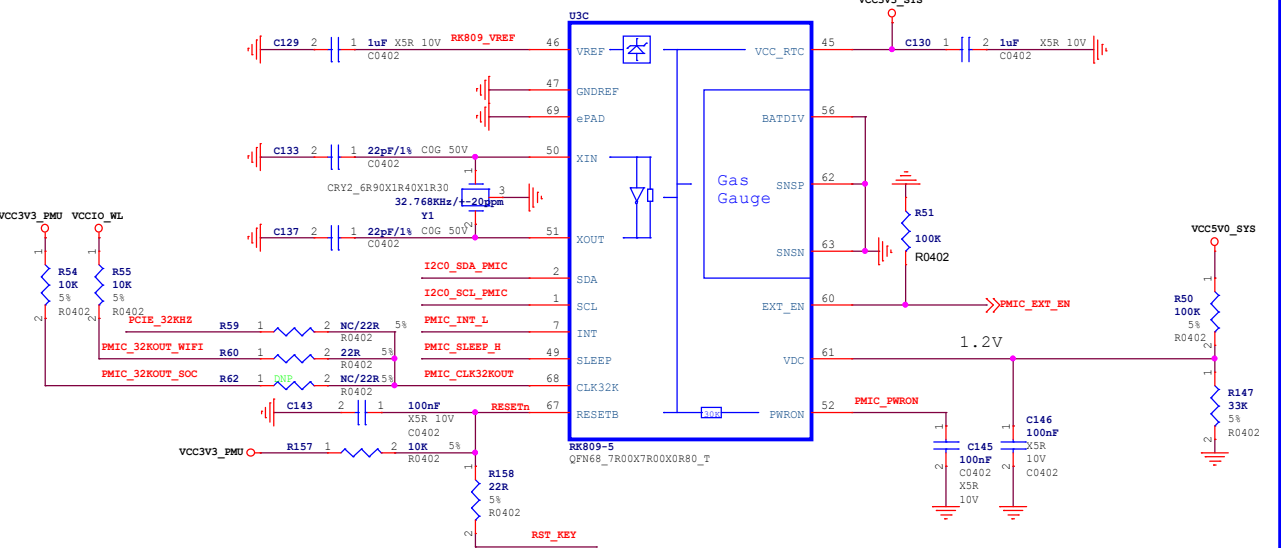
## PMIC RK809 DCDC



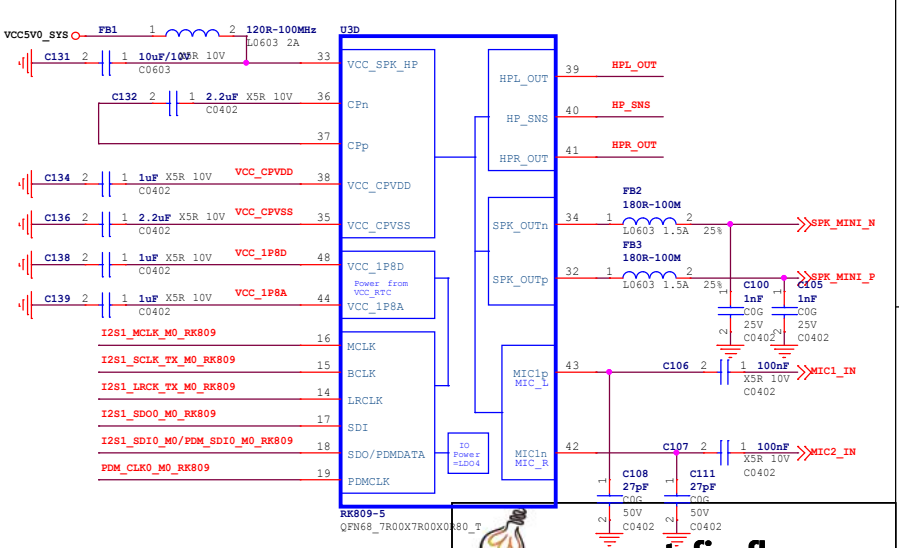
## PMIC RK809 LDO



## PMIC RK809 Management

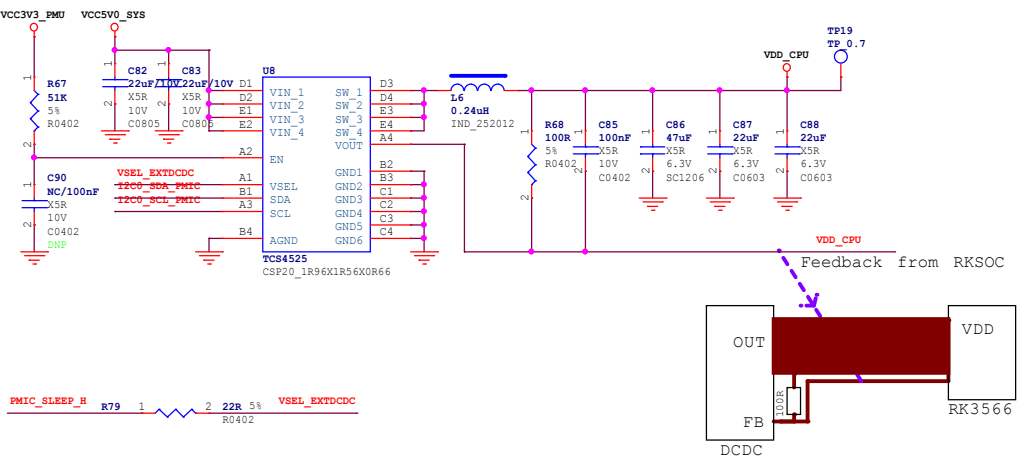


## PMIC RK809 CODEC

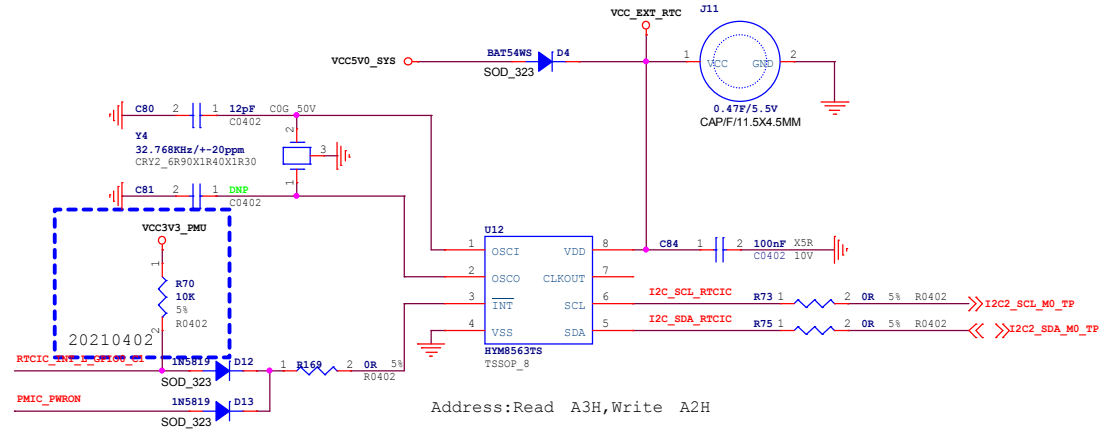


I2C0\_SCL\_PMIC  
 I2C0\_SDA\_PMIC  
 PMIC\_SLEEP\_H  
 RTCIC\_INT\_1\_GPIO0\_C1  
 PMIC\_PWRON  
 PMIC\_EXT\_EN

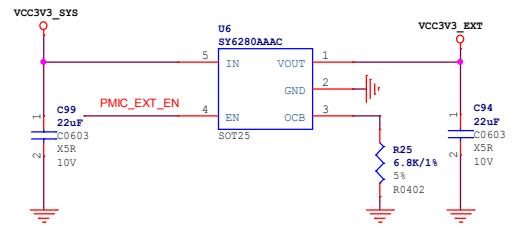
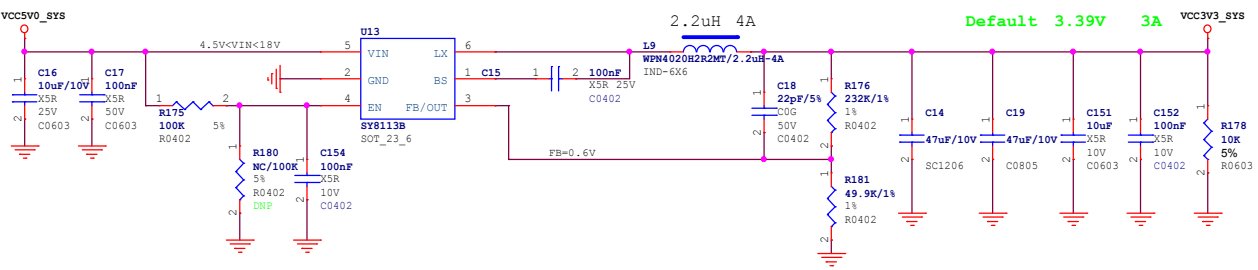
### VDD\_CPU\_EXT



### RTC IC



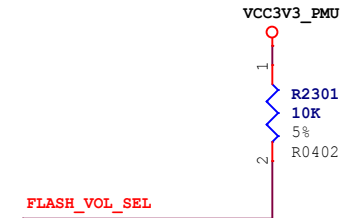
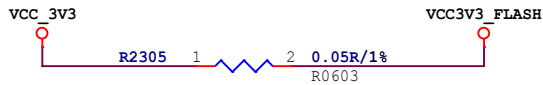
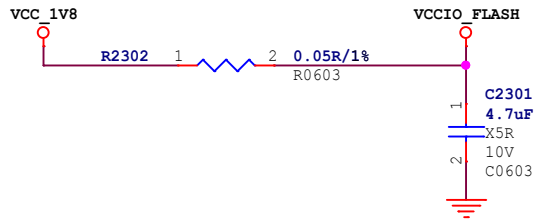
### VCC3V3\_SYS




# Flash Power Manage

← FLASH\_VOL\_SEL

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)



Note:  
 FLASH\_VOL\_SEL state decided to VCCIO2 domain IO driven by default  
 Logic=L: 3.3V IO driven  
 Logic=H: 1.8V IO driven



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**Title: Power Flash Power Manage**

**File: ROC-3566-PC** REV: V0.1

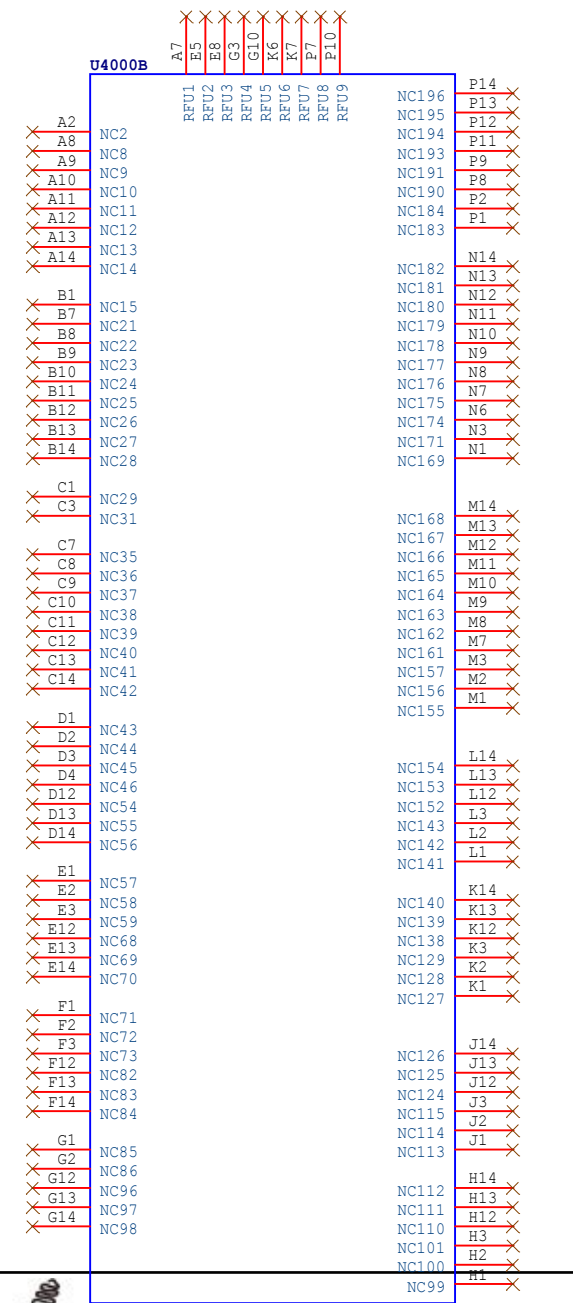
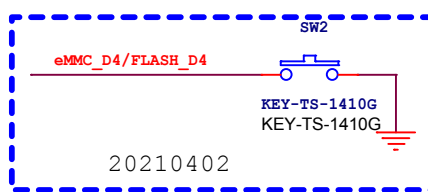
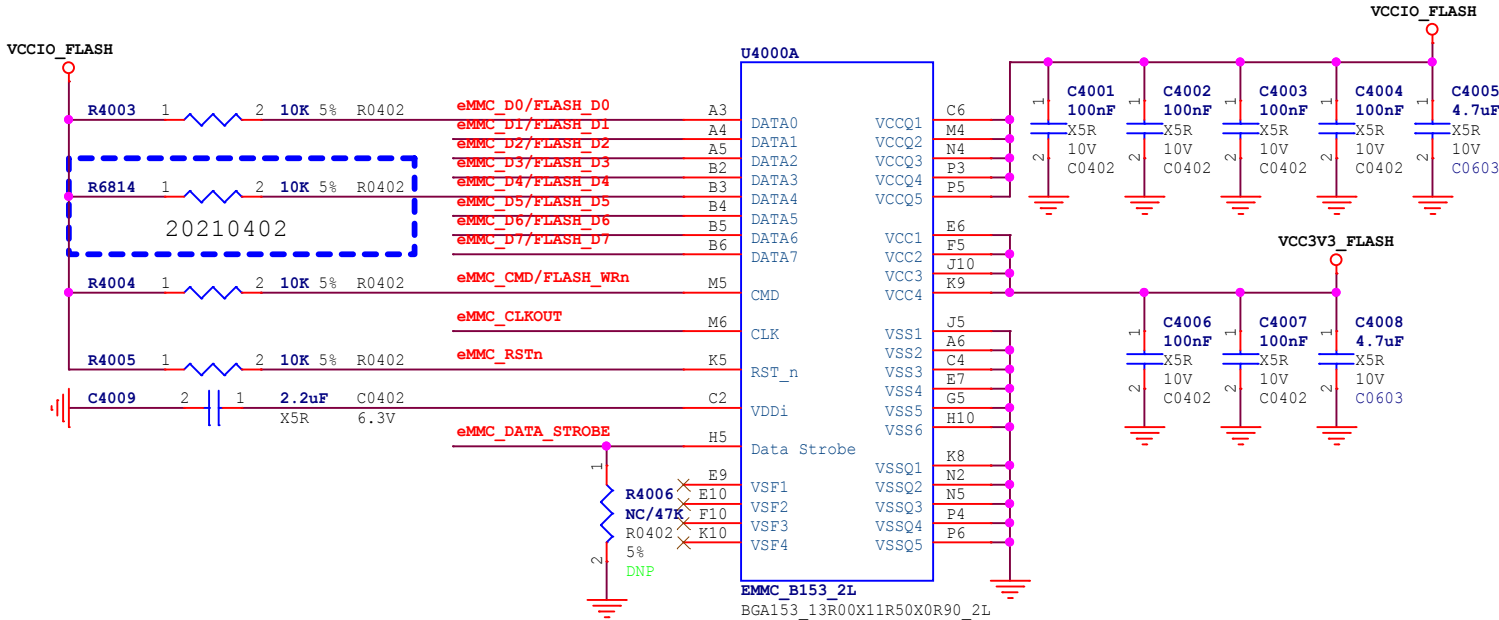
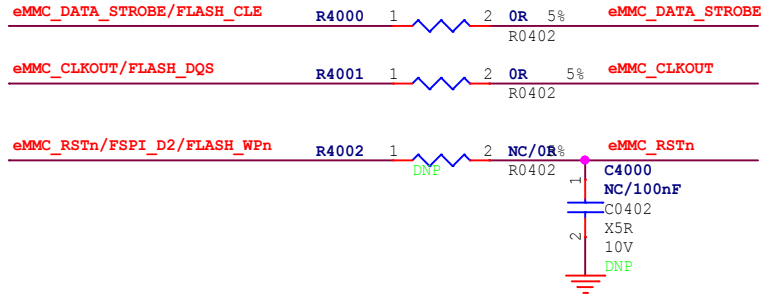
Create Date: Tuesday, May 19, 2020 Page Num: 23

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>>eMMC\_D0/FLASH\_D0  
 >>eMMC\_D1/FLASH\_D1  
 >>eMMC\_D2/FLASH\_D2  
 >>eMMC\_D3/FLASH\_D3  
 >>eMMC\_D4/FLASH\_D4  
 >>eMMC\_D5/FLASH\_D5  
 >>eMMC\_D6/FLASH\_D6  
 >>eMMC\_D7/FLASH\_D7  
  
 >>eMMC\_CMD/FLASH\_WRn  
  
 >>eMMC\_CLKOUT/FLASH\_DQS  
  
 >>eMMC\_DATA\_STROBE/FLASH\_CLE  
  
 >>eMMC\_RSTn/FSPI\_D2/FLASH\_WPn

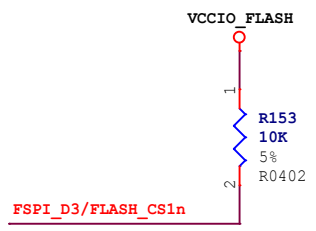
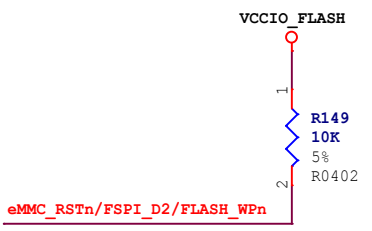
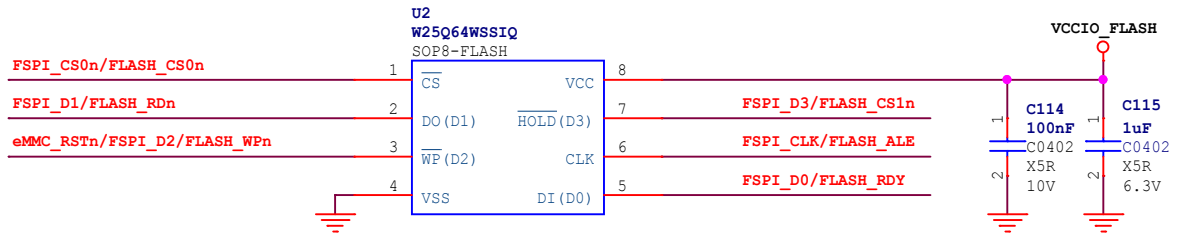


<b>Title:</b> Flash-eMMC Flash		REV: V0.1
<b>File:</b> ROC-3566-PC		
<b>Create Date:</b> Thursday, May 07, 2020	<b>Page Num:</b> 25	
<b>Modify Date:</b> Monday, April 19, 2021	<b>Page Total:</b> 37	

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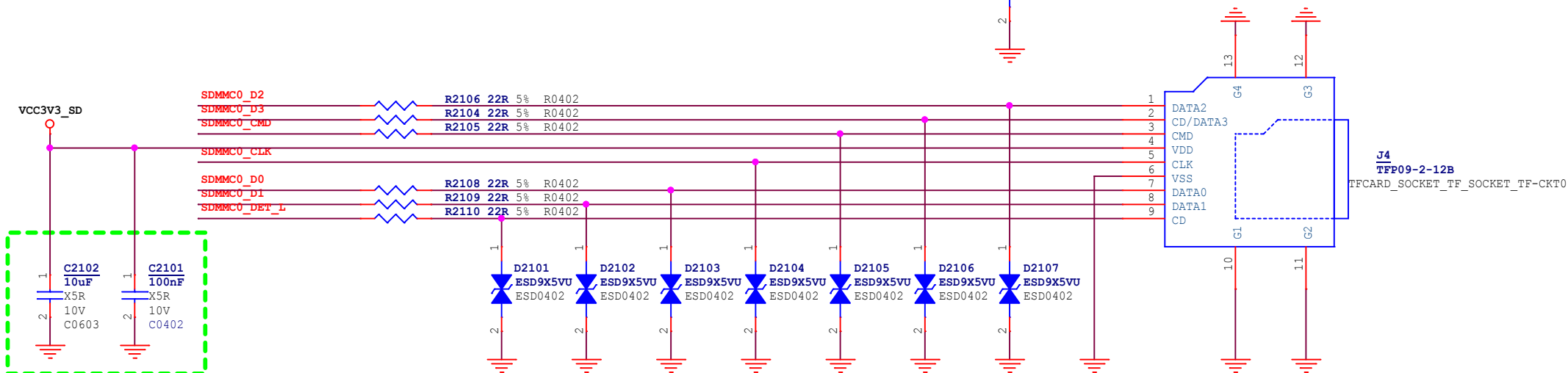
>>FSPI\_CLK/FLASH\_ALE 14,28  
 >>FSPI\_D0/FLASH\_RDY 14,28  
 >>FSPI\_D1/FLASH\_RDn 14,28  
 >>eMMC\_RSTn/FSPI\_D2/FLASH\_WPn 14,27,28  
 >>FSPI\_D3/FLASH\_CS1n 14,28  
 >>FSPI\_CS0n/FLASH\_CS0n 14,28

default VCC = 1.8V




<b>Title:</b> Flash-SPI FLASH	
<b>File:</b> ROC-3566-PC	REV: V0.1
<b>Create Date:</b> Saturday, January 09, 2021	<b>Page Num:</b> 26
<b>Modify Date:</b> Monday, April 19, 2021	<b>Page Total:</b> 37

>>SDMMC0\_D0  
 >>SDMMC0\_D1  
 >>SDMMC0\_D2  
 >>SDMMC0\_D3  
 >>SDMMC0\_CMD  
 >>SDMMC0\_CLK  
 <<SDMMC0\_DET\_L



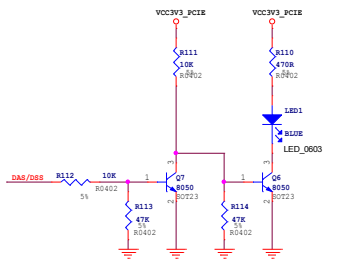
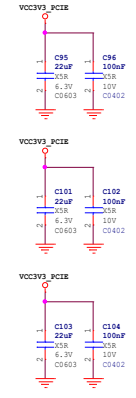
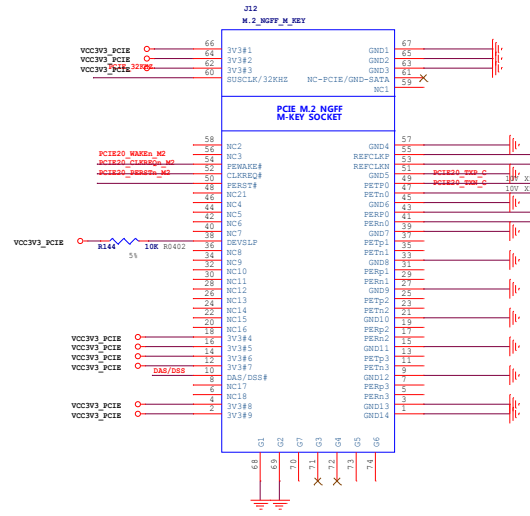
Close to MicroSD Card

MicroSD Card

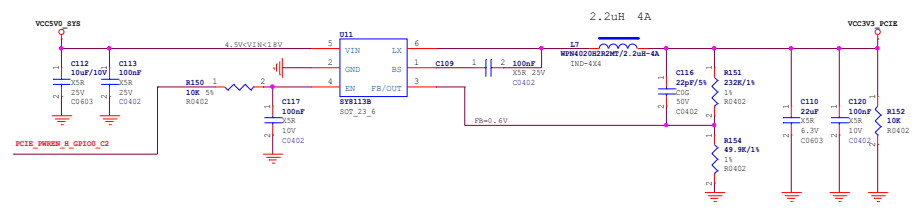
		<a href="http://www.t-firefly.com">www.t-firefly.com</a>	
<b>Title: Flash-MicroSD Card</b>			
<b>File: ROC-3566-PC</b>			REV: V0.1
Create Date: Thursday, January 07, 2021		Page Num: 27	
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- >>> PCIE20\_TXP 15
- >>> PCIE20\_RXN 15
- >>> PCIE20\_RXP 15
- >>> PCIE20\_RXN 15
- >>> PCIE20\_REFCLKP 15
- >>> PCIE20\_REFCLKN 15
- >>> PCIE20\_CLKREQ\_M2 20
- >>> PCIE20\_WAKE\_M2 20
- >>> PCIE20\_PERRST\_M2 20
- >>> PCIE\_PWRSEN\_B\_GPI00\_C2 13
- <<< PCIE\_32KHZ

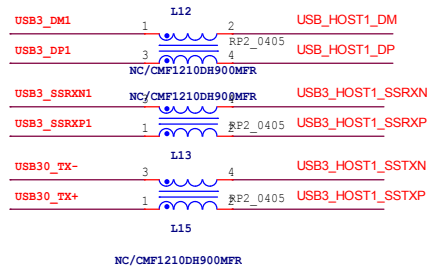
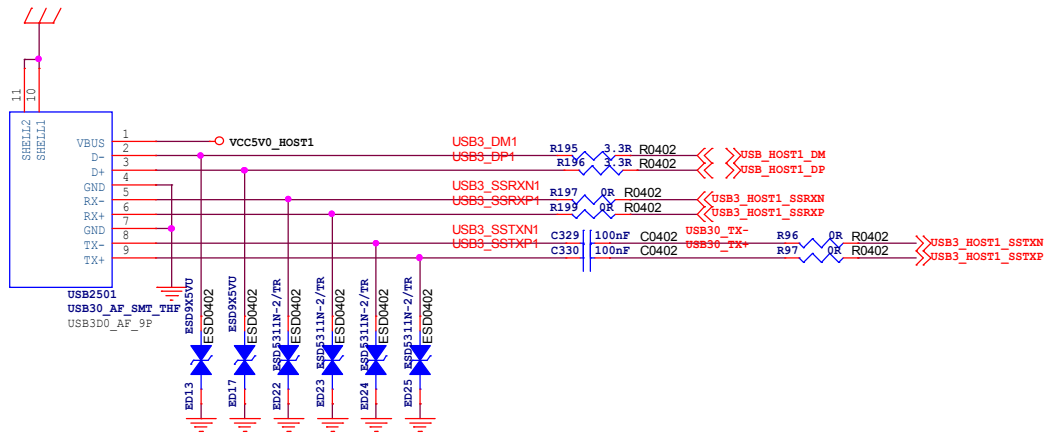
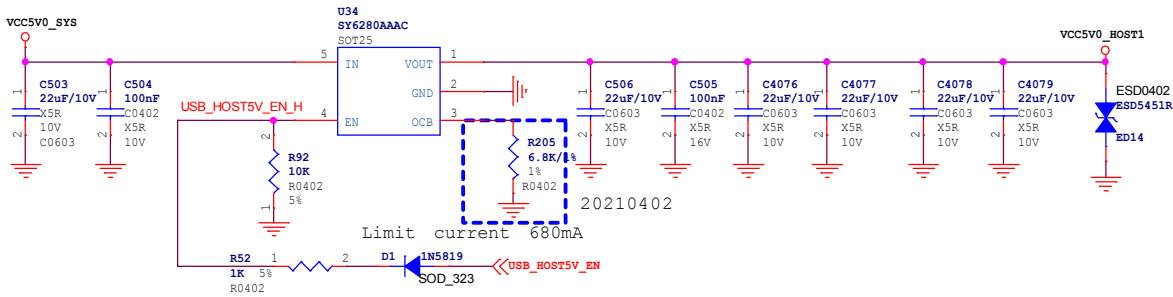
# PCIe2.0 x 1



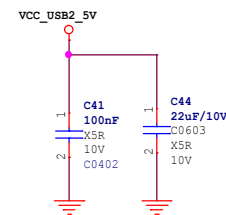
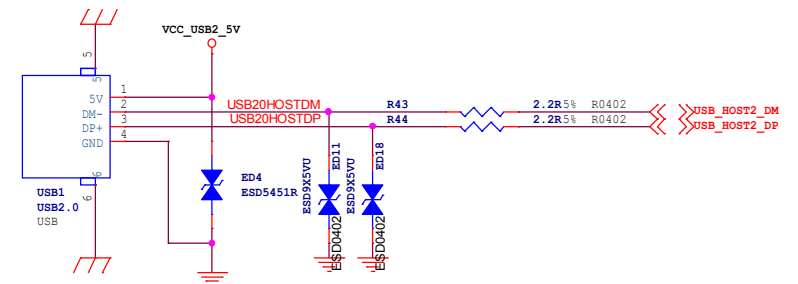
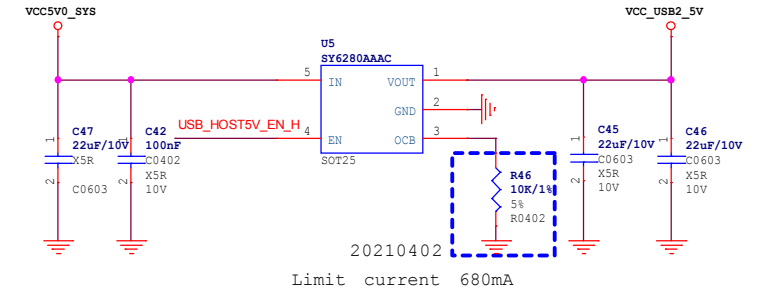
Clock --> PCIe2.0 CON




# USB3.0



# USB2.0



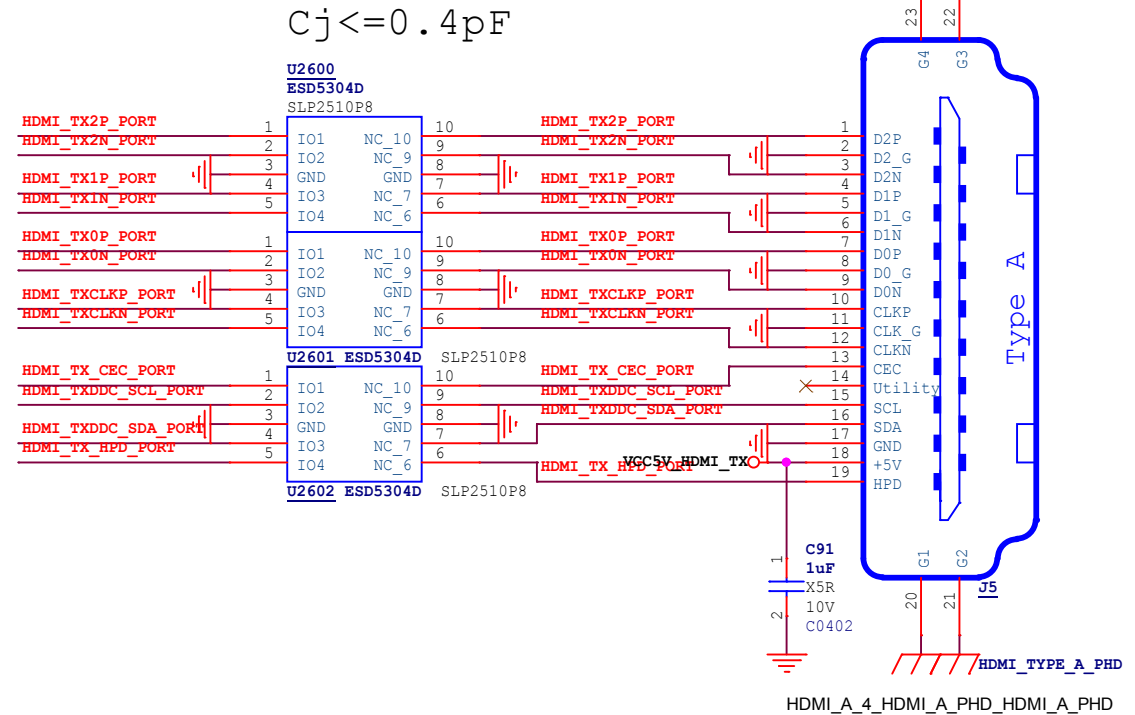
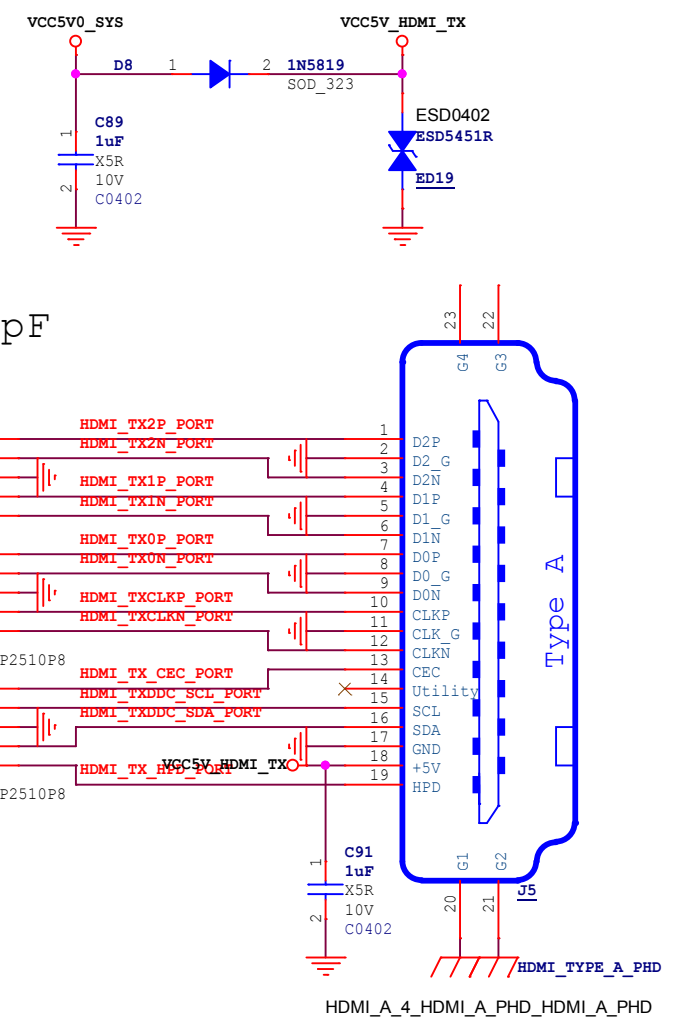
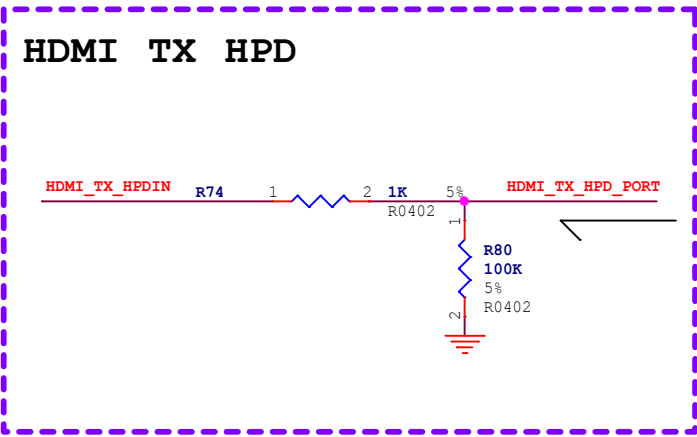
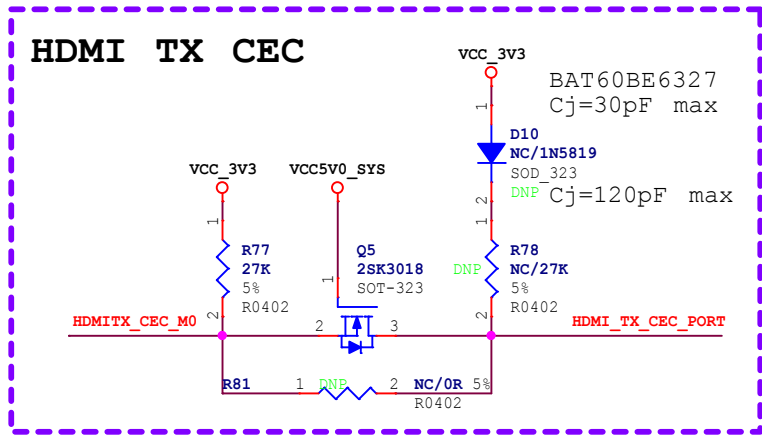
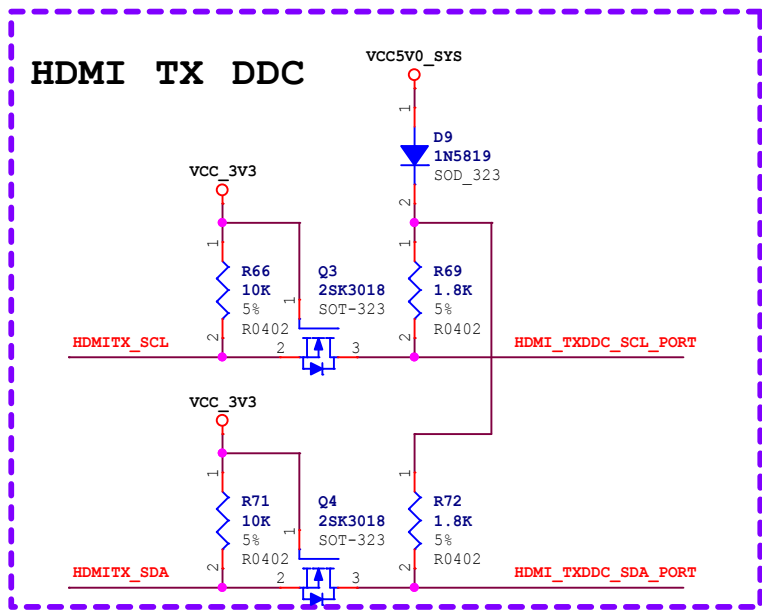


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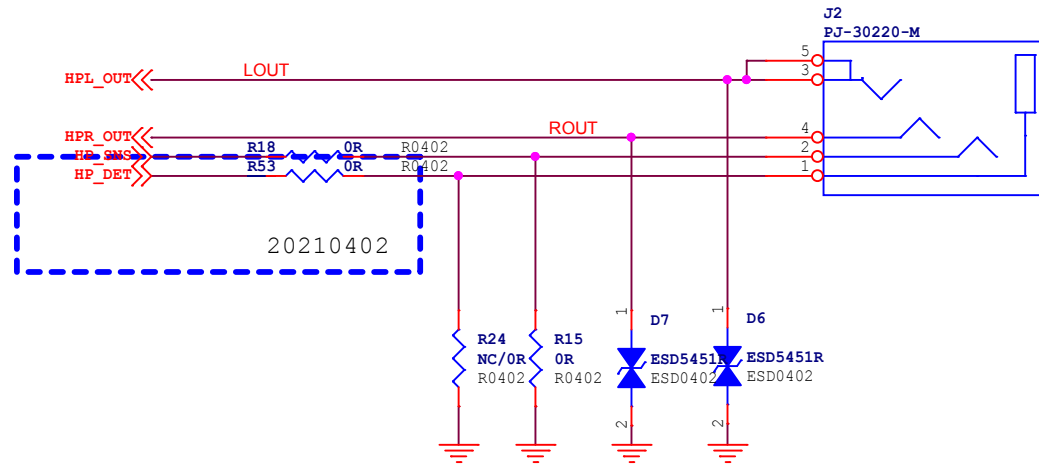
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<b>File: ROC-3566-PC</b>		
Create Date: Wednesday, January 06, 2021	Page Num: 29	
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- >>HDMI\_TX2P\_PORT
- >>HDMI\_TX2N\_PORT
- >>HDMI\_TX1P\_PORT
- >>HDMI\_TX1N\_PORT
- >>HDMI\_TX0P\_PORT
- >>HDMI\_TX0N\_PORT
- >>HDMI\_TXCLKP\_PORT
- >>HDMI\_TXCLKN\_PORT
- <<HDMI\_TX\_SCL
- <<HDMI\_TX\_SDA
- <<HDMI\_TX\_CEC\_M0
- <<HDMI\_TX\_HPDIN

3.3V  
3.3V  
3.3V



Title: HDMI2.0 TX		REV: V0.1
File: ROC-3566-PC		
Create Date: Wednesday, January 06, 2021	Page Num: 30	
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Title: Audio Port

File: ROC-3566-PC

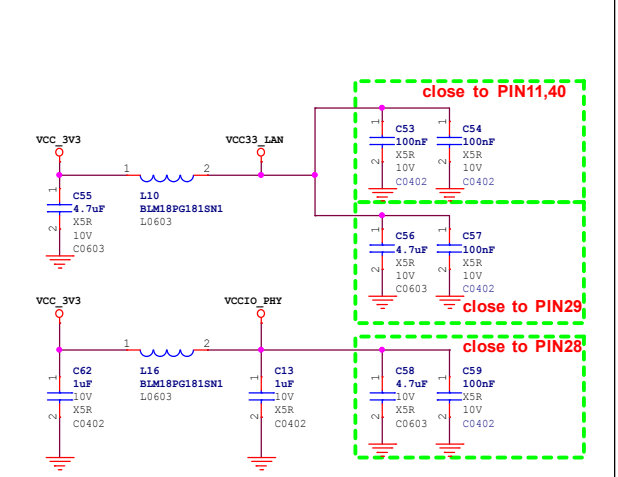
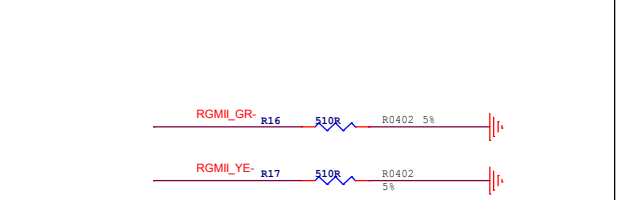
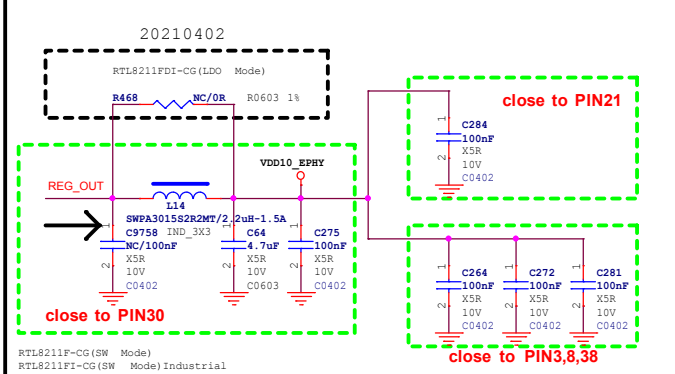
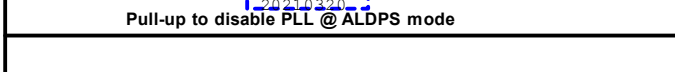
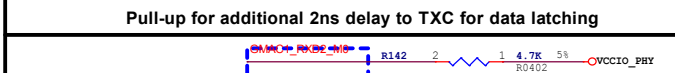
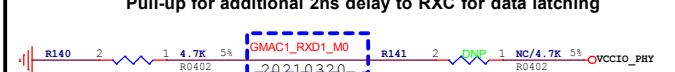
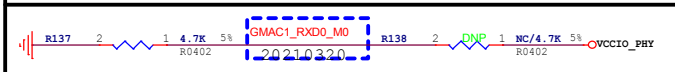
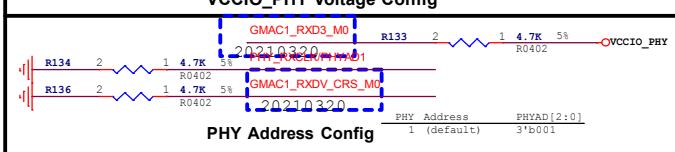
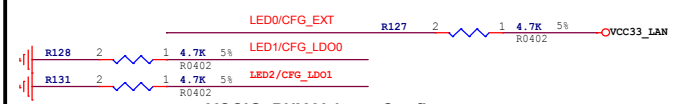
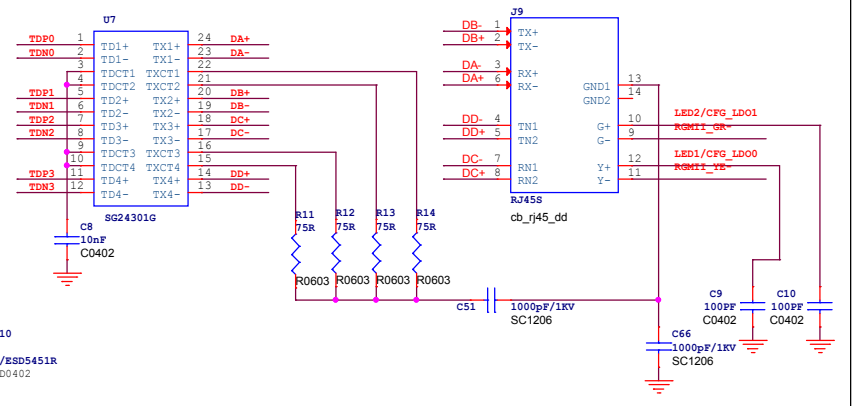
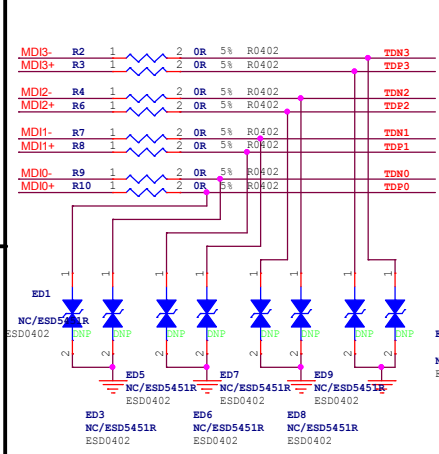
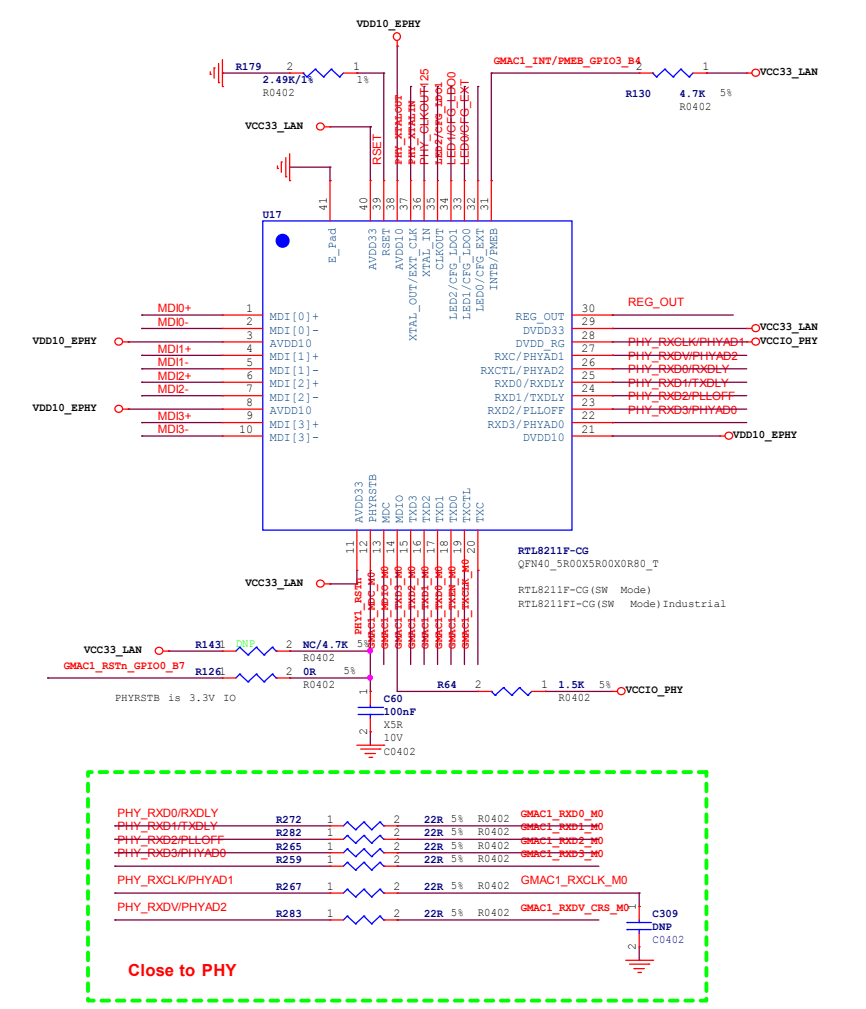
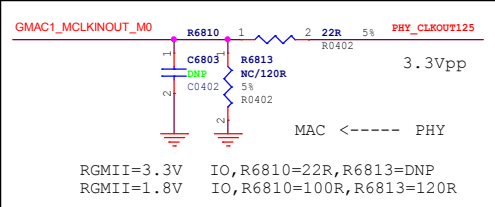
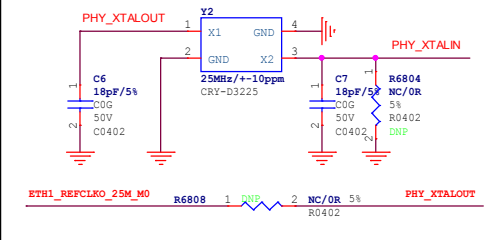
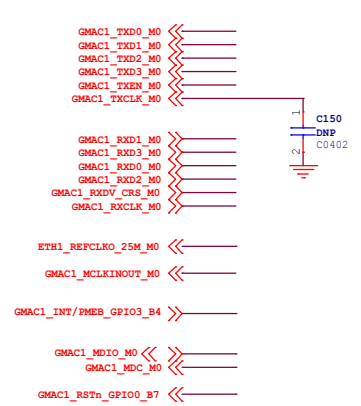
REV: V0.1


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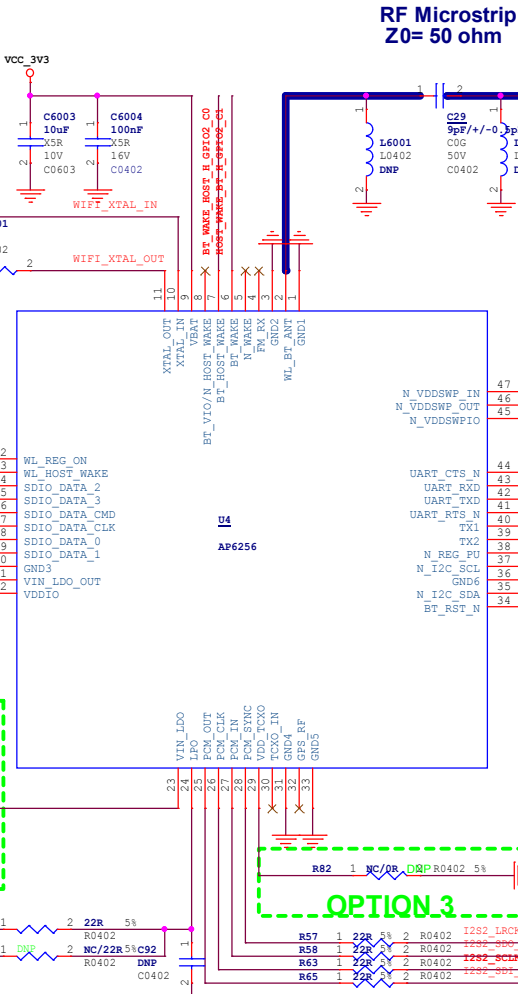
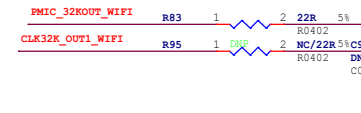
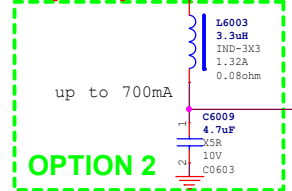
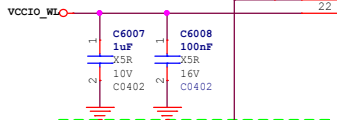
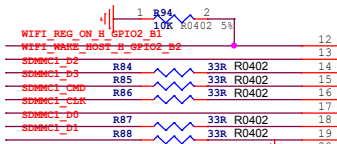
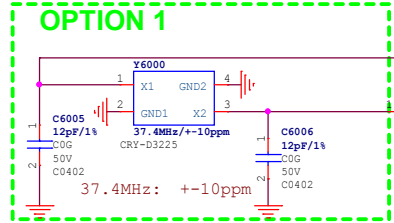
<b>Title: 10/100/1000M-ExternalPHY</b>	
<b>File: ROC-3566-PC</b>	REV: V0.1
<b>Create Date: Wednesday, January 06, 2021</b>	Page Num: 32
<b>Modify Date: Monday, April 19, 2021</b>	Page Total: 37



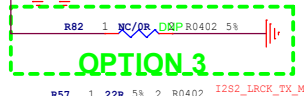
# WiFi/BT Module



**NOTE:**  
 If WiFi/BT is needed to wake up SOC,  
 WIFI\_REG\_ON is needed to wake up SOC,  
 WIFI\_WAKE\_HOST is needed to pull high.  
 So WIFI\_REG\_ON must be connected to  
 PMUIO.  
 WIFI\_WAKE\_HOST is also connected to  
 PMUIO



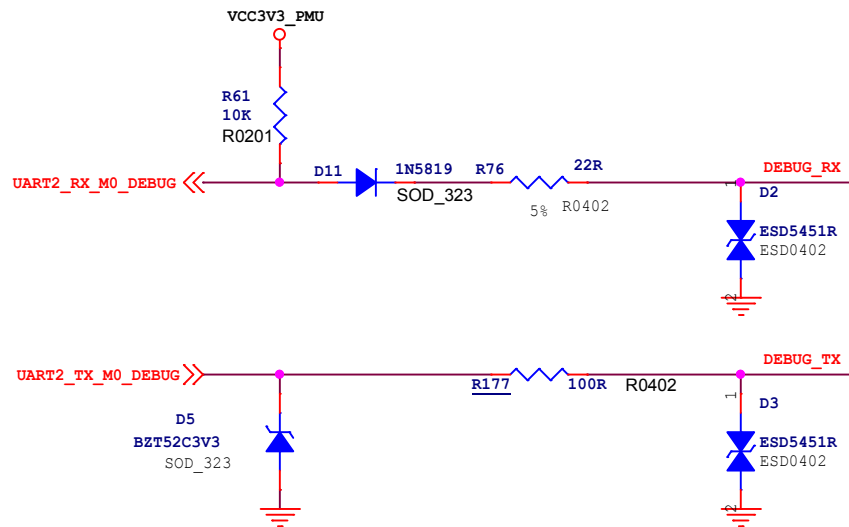
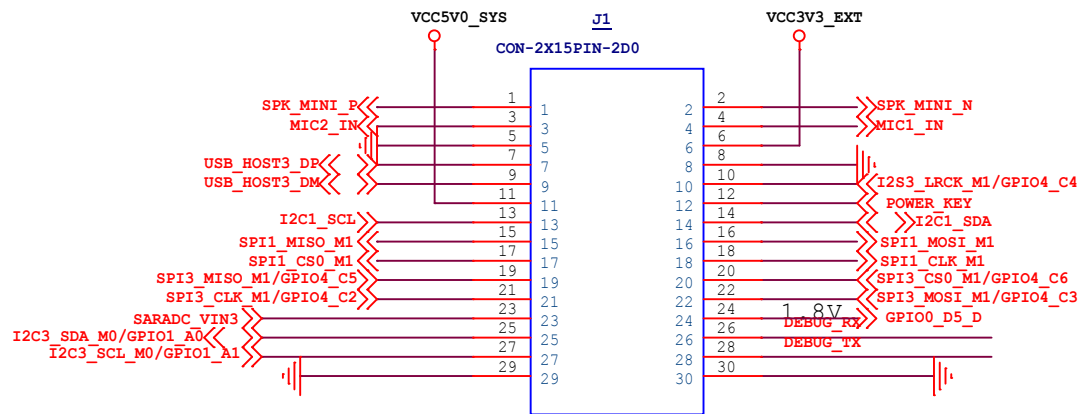
**IF use BT to wake up system,  
 BT\_RST is needed to pull high.  
 So BT\_RST must be connected to PMUIO.  
 BT\_WAKE\_HOST is also connected to PMUIO.**




OPTION	WIFI				BT	Crystals	VCCIO_SDIO	OPTION1	OPTION2	OPTION3	OPTION4
	a	b/g/n	ac	5GHz							
AP6236/AP6212	No	Yes	No	No	4.2/4.0	26MHz	1.71-3.63V	Yes	Yes	No	No
AP6256/AP6255	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.62-3.63V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	No
RTL8189FTV Module F89FTSM12-W3	No	Yes	No	No	No	Module Integrated	1.8-3.3V	No	No	No	No
RTL8723DS Module 6223A-SRD	No	Yes	No	No	4.2	Module Integrated	1.62-3.63V	No	No	No	Yes
QCA9377 Module 8223A-SR	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	No
RTL8821CS Module 6221A-SRC	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	No

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**Title:** WIFI/BT-SDIO 1T1R+UART  
**File:** ROC-3566-PC  
**Rev:** V0.1  
**Create Date:** Thursday, January 07, 2021  
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**Page Num:** 33  
**Page Total:** 37

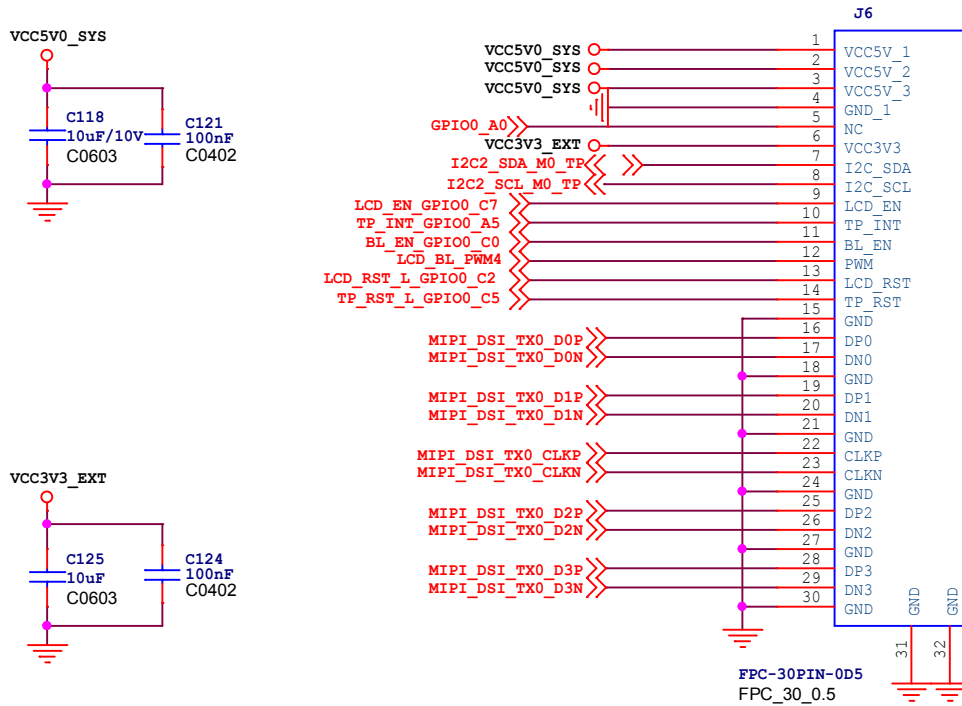





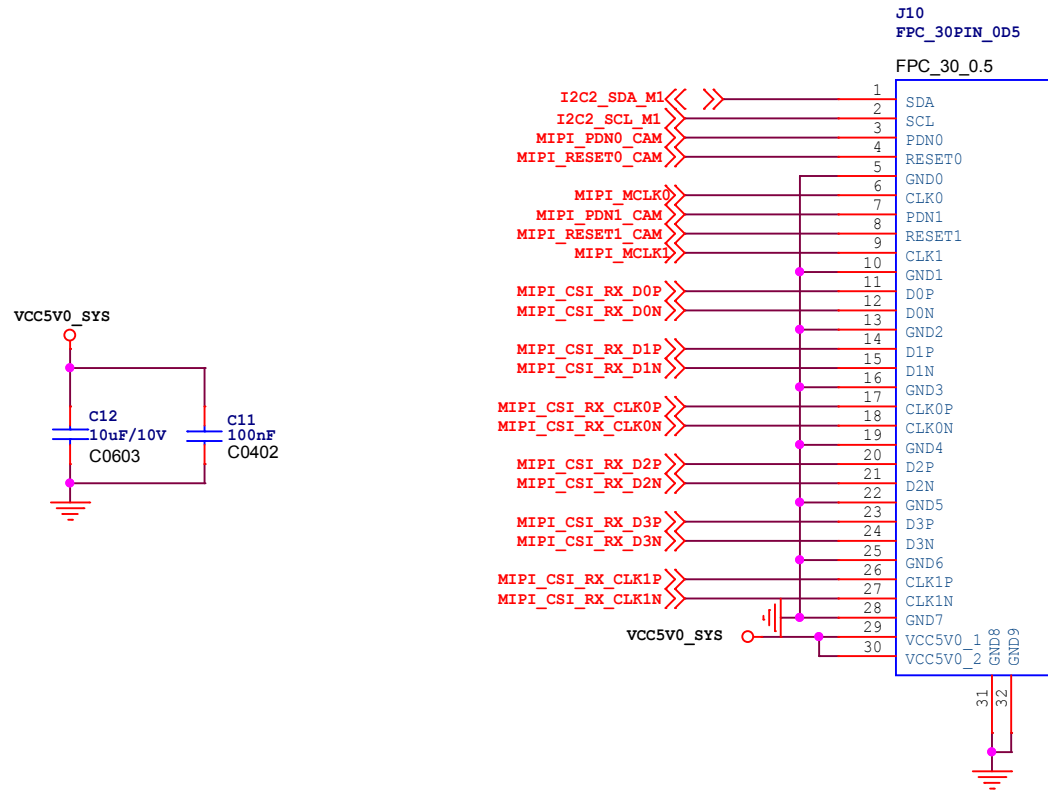

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<b>Title:</b> Connector	
<b>File:</b> ROC-3566-PC	REV: V0.1
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<b>Modify Date:</b> Monday, April 19, 2021	<b>Page Total:</b> 37

# MIP Display Interface



		<a href="http://www.t-firefly.com">www.t-firefly.com</a>	
<b>Title: MIPI-DSI</b>			
<b>File: ROC-3566-PC</b>			REV: V0.1
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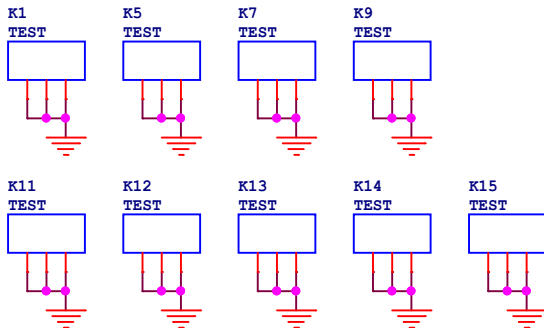
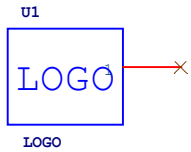
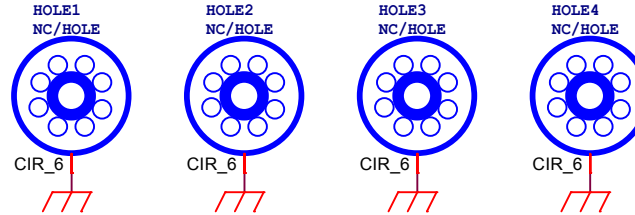
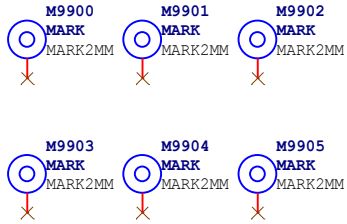
**Title:** MIPI-CSI


**File:** ROC-3566-PC REV: V0.1

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## PCB Mark Point



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<b>Title: Mark/Hole/Heatsink</b>			
<b>File: ROC-3566-PC</b>			REV: V0.1
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