EVB Schematics For RK3568

RK_EVB1_RK3568_DDR4P216SD6_V1.0

Main Functions Introduction

1) PMIC: RK809-5+DiscretePower
2) RAM: DDR4 2x16Bit
3) ROM: eMMC5.1+SPI Falsh,Option Nand Flash
4) Support: Micro SD Card3.0
5) Support: 1 x USB3.0 OTG + 1 x USB3.0 HOST + 2 x USB2.0 HOST
6) Support: 1 x SATA3.0 Connector (7pin) + 4 pin Power Connector
7) Support: 1 x 2Lanes PCIe3.0 Connector (RC Mode)
8) Support: 1 x 4Lanes MIPI CSI Camera or 2 x 2Lanes MIPI CSI Camera
9) Support: Parallel CIF Connector(Option-Ext Board)
10) Support: 1 x HDMI2.0 TX
11) Support: eDP to VGA TX or 1 x 4Lanes eDP with Touch Connector(Option)
12) Support: 2 x 4Lanes MIPI DSI or 1 x 4Lanes MIPI DSI + 1 x LVDS with Touch Connector
13) Support: a/b/g/n/ac 2X2 WIFI,BT5.0
14) Support: 2 x 10/100/1000 Ethernet(RGMII)
15) Support: IR Receiver
16) Support: Optical S/PDIF TX
17) Support: Headphone output,1 x ECM MIC and Speaker out(1.3W@8ohm)
18) Support: Array MIC Connector(Ext Board PDM)
19) Support: Gyroscope+G-sensor
20) Support: Array Key(MENU,VOL+,VOL-,ESC),Reset,Power on/off Key
21) Support: 3 x UART + 2 x UART(Option)
22) Support: 1 x CAN FD
23) Support: 5 x SARADC
24) Support: Debug UART to USB connector and JTAG Connector

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Table of Content

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

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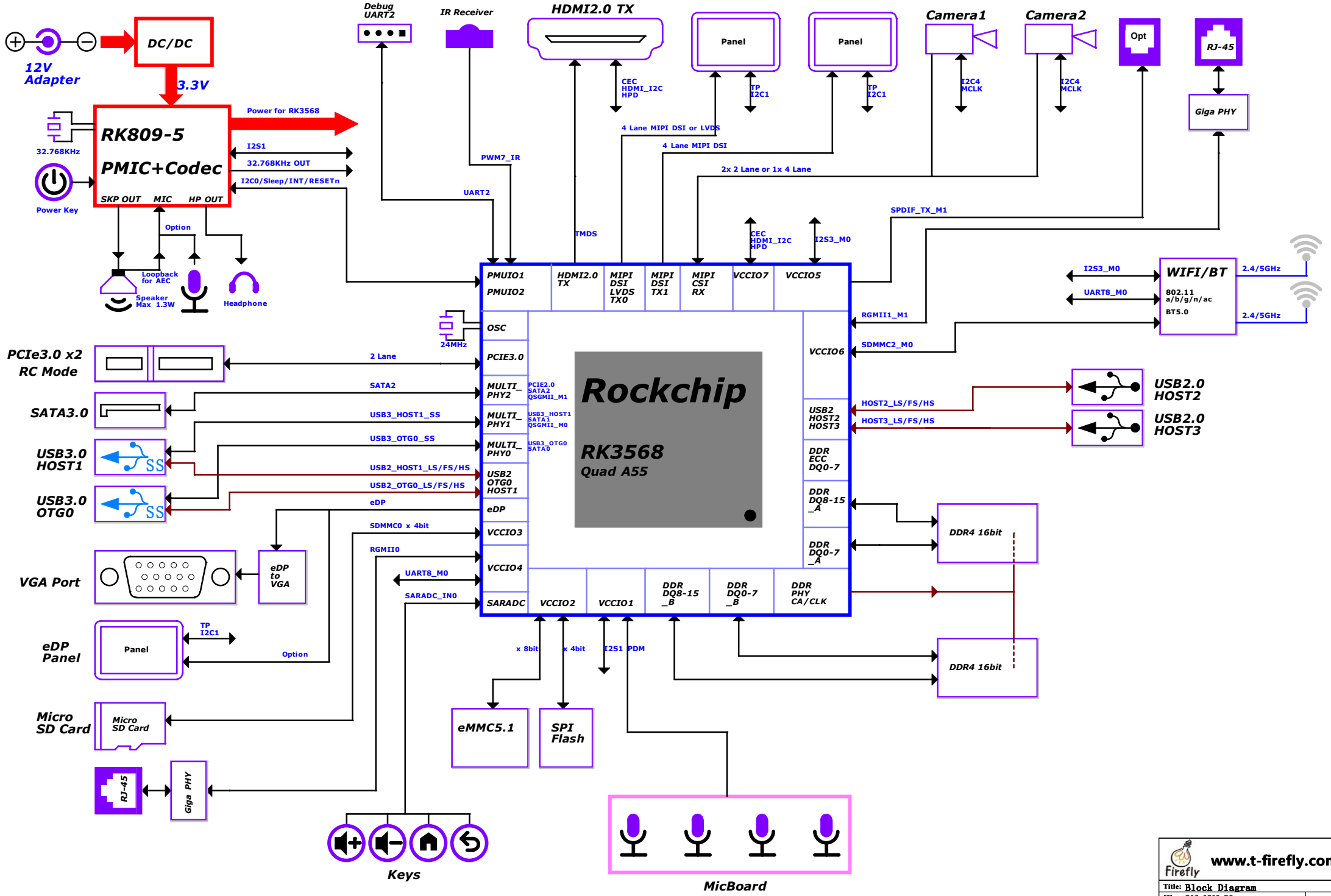
Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2020-09-08	Zhangdz	1:Revision preliminary version	

RK3568 Ref Block Diagram



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Power Diagram

12V Adapter

DC/DC 3000mA Seq:0 Max:

VCC3V3_SYS

RK809-5

Power on Sequence

VCC1	BUCK1 0.5V~2.4V, 2.5A max	Seq:1	VDD_LOGIC Max:	RK3568_Logic
VCC2	BUCK2 0.5V~2.4V, 2.5A max	Seq:2	VDD_GPU Max:	RK3568_GPU
VCC3	BUCK3 0.5V~2.4V, 1.5A max	Seq:3	VCC_DDR Max:	RK3568_DDR_VDDQ
VCC4	BUCK4 0.5V~3.4V, 1.5A max	OFF	VDD_NPU Max:	RK3568_NPU
	LDO1 0.6V~3.4V, 400mA max	OFF	VDDA0V9_IMAGE Max:	
VCC5	LDO2 0.6V~3.4V, 400mA max	Seq:1	VDDA_0V9 Max:	
	LDO3 0.6V~3.4V, 100mA max	Seq:1	VDDA0V9_PMU Max:	
	LDO4(Codec_VDDIO) 0.6V~3.4V, 400mA max	OFF	VCCIO_ACODEC Max:	VCCIO1--I2S1/PDM MIC
VCC6	LDO5 0.6V~3.4V, 400mA max	Seq:4	VCCIO_SD Max:	VCCIO3--SDMMC0
	LDO6 0.6V~3.4V, 400mA max	Seq:2	VCC3V3_PMU Max:	PMUIO1/ PMUIO2
	LDO7 0.6V~3.4V, 400mA max	Seq:2	VCCA_1V8 Max:	
VCC7	LDO8 0.6V~3.4V, 400mA max	Seq:2	VCCA1V8_PMU Max:	PMUPLL_AVDD_1V8
	LDO9 0.6V~3.4V, 400mA max	OFF	VCCA1V8_IMAGE Max:	
VCC8	Switch2 2.1 A max, Rdson=100mΩ	Seq:4	VCC3V3_SD Max:	Micro SD Card
VCC9	Switch1 2.1 A max, Rdson=90mΩ	Seq:4	VCC_3V3 Max:	
	BUCK5: 1.5V~3.6V, 2.5 A max	Seq:2	VCC_1V8 Max:	
VCC_RTC				

VCC5V0_SYS

EXT DC/DC ,5A Seq:2A → VDD_CPU Max: → RK3568_CPU

EXT LDO ,0.3A Seq:2A → VCC2V5_DDR Max: → DDR4 DRAM

VCC3V3_SYS → Mos-->LCD Panel Max:; Mos-->VCC3V3_VGA Max:; RTC IC Max:

MOS OFF → PCIe Slot Max:; SATA Max:

DC/DC 3000mA Seq:0 → VCC5V0_USB Max: → SATA Max:; USB HOST Max:

DC/DC 3000mA Seq:0 → VCC5V0_SYS Max: → VCC5V_HDMI_TX Max:; RK809_SPK_PA Max:; CAN transceiver IC Max:; MIPI-CSI_RX_CON Max:; MIPI/LVDS_Panel_CON0/1 Max:; eDP_Panel_CON/VGA OUT Max:; MIC Expand Board Max:; RGMII/CIF/EBC Expand Board Max:; MOS → VCC5V0_VGA Max:; LDO → VCC3V3_PI6C Max:; LDO → VCC3V3_BU Max:

DC/DC 3000mA → VCC3V3_PCIE Max:

VDDA0V9_IMAGE → MIPI_CSI_RX_AVDD_0V9 Max:; MIPI_DSI_TX0/LVDS_TX0_AVDD_0V9 Max:; MIPI_DSI_TX1_AVDD_0V9 Max:; EDP_TX_AVDD_0V9 Max:; HDMI_TX_AVDD_0V9 Max:

VDDA_0V9 → SYSPLL_AVDD_0V9 Max:; USB2_AVDD_0V9 Max:; USB3_AVDD_0V9 Max:; MULTI_PHY_AVDD_0V9 Max:; PCIE30_AVDD_0V9 Max:

VDDA0V9_PMU → PMU_VDD_LOGIC_0V9 Max:; PMUPLL_AVDD_0V9 Max:

VCCA_1V8 → SYSPLL_AVDD_1V8 Max:; USB2_AVDD_1V8 Max:; USB3_AVDD_1V8 Max:; MULTI_PHY_AVDD_1V8 Max:; PCIE30_AVDD_1V8 Max:; SARADC_AVDD_1V8 Max:

VCCA1V8_IMAGE → MIPI_CSI_RX_AVDD_1V8 Max:; MIPI_DSI_TX0/LVDS_TX0_AVDD_1V8 Max:; MIPI_DSI_TX1_AVDD_1V8 Max:; EDP_TX_AVDD_1V8 Max:; HDMI_TX_AVDD_1V8 Max:

VCC_3V3 → USB3_AVDD_3V3 Max:; USB2_AVDD_3V3 Max:; VCCIO5,VCCIO7 Max:; eMMC_VCC / Nand_VCC Max:; VCC3V3_PHY0/1 Max:; VCC3V3_TP Max:; VCC3V3_SPDIF Max:; VCC3V3_WL_VBAT Max:; Sensor/IR Receiver Max:; UART Device Max:; CAN IC Max:; MIC Expand Board Max:; RGMII/CIF/EBC Expand Board Max:; MIC(Option) Max:; FSUSB30MUX Max:; Max:

VCC_1V8 → OTP_VCC18 Max:; VCCIO2(Default) --eMMC/Nand IO Max:; VCCIO4(Default) --WIFI/BT IO Max:; VCCIO5(Default) Max:; VCCIO6(Default) Max:; GiGa PHY0/1 IO Max:

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Title:	Power Diagram
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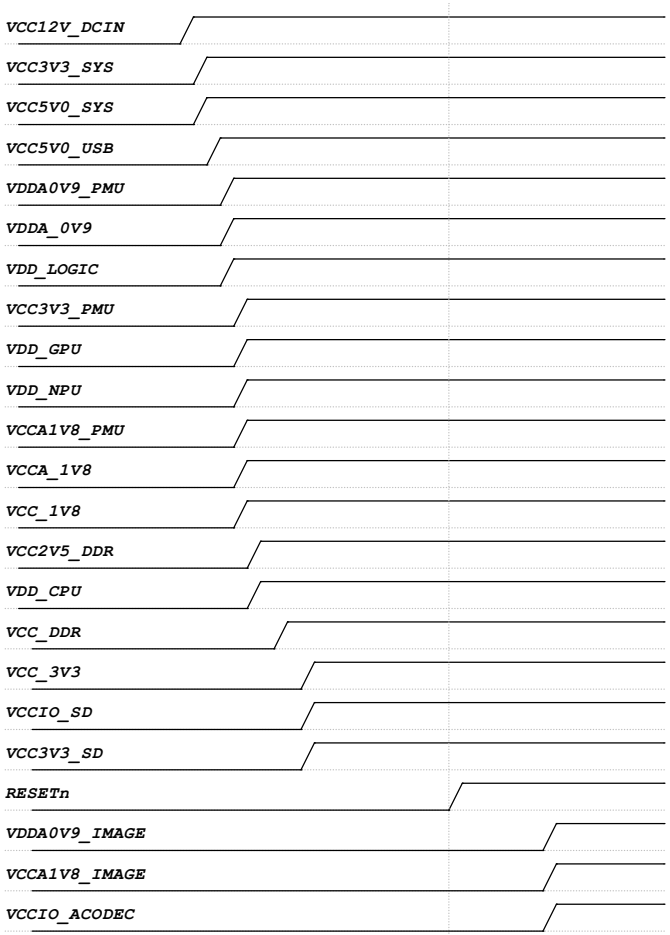
Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC3V3_SYS	RK809_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_BUCK2	2.5A	VDD_GPU	Slot:2	0.9V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_BUCK4	1.5A	VDD_NPU	N/A	0.9V	OFF	OFF	TBD	TBD
VCC3V3_SYS	RK809_LDO1	0.4A	VDDA0V9_IMAGE	N/A	0.9V	OFF	OFF	TBD	TBD
	RK809_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	OFF	TBD	TBD
	RK809_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_LDO4	0.4A	VCCIO_ACODEC	N/A	3.3V	OFF	OFF	TBD	TBD
	RK809_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	OFF	TBD	TBD
	RK809_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_LDO7	0.4A	VCCA_1V8	Slot:2	1.8V	ON	OFF	TBD	TBD
	RK809_LDO8	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	ON	TBD	TBD
	RK809_LDO9	0.4A	VCCA1V8_IMAGE	N/A	1.8V	OFF	OFF	TBD	TBD
VCC3V3_SYS	RK809_SW2 100mohm	2.1A	VCC3V3_SD	Slot:4	3.3V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_SW1 90mohm	2.1A	VCC_3V3	Slot:4	3.3V	ON	OFF	TBD	TBD
	RK809_BUCK5	2.5A	VCC_1V8	Slot:2	1.8V	ON	OFF	TBD	TBD
	RK809_RESETn			Slot:4+5					
VCC12V_DCIN	EXT BUCK	3.0A	VCC3V3_SYS	Slot:0	3.3V	ON	ON	TBD	TBD
VCC12V_DCIN	EXT BUCK	3.0A	VCC5V0_SYS	Slot:0	5.0V	ON	OFF	TBD	TBD
VCC5V0_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	OFF	TBD	TBD
VCC3V3_SYS	EXT LDO	0.3A	VCC2V5_DDR	Slot:2A	2.5V	ON	ON	TBD	TBD

IO Power Domain Map

Updates must be Revision accordingly!

IO Domain	Pin Num	Support IO Voltage		Actual assigned IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	Pin Y20	✓	✗	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	Pin W19	✓	✓	VCC3V3_PMU	VCC3V3_PMU	3.3V	
VCCIO1	Pin H17	✓	✓	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	Pin H18	✓	✓	VCCIO_FLASH	VCC_1V8	1.8V	PIN "FLASH_VOL_SEL" must be logic High if VCCIO_FLASH=3.3V,FLASH_VOL_SEL must be logic low
VCCIO3	Pin L22	✓	✓	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	Pin J21	✓	✓	VCCIO4	VCC_1V8	1.8V	
VCCIO5	Pin V10 Pin V11	✓	✓	VCCIO5	VCC_3V3	3.3V	
VCCIO6	Pin R9 Pin U9	✓	✓	VCCIO6	VCC_1V8	1.8V	
VCCIO7	Pin V12	✓	✓	VCCIO7	VCC_3V3	3.3V	

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UART MAP

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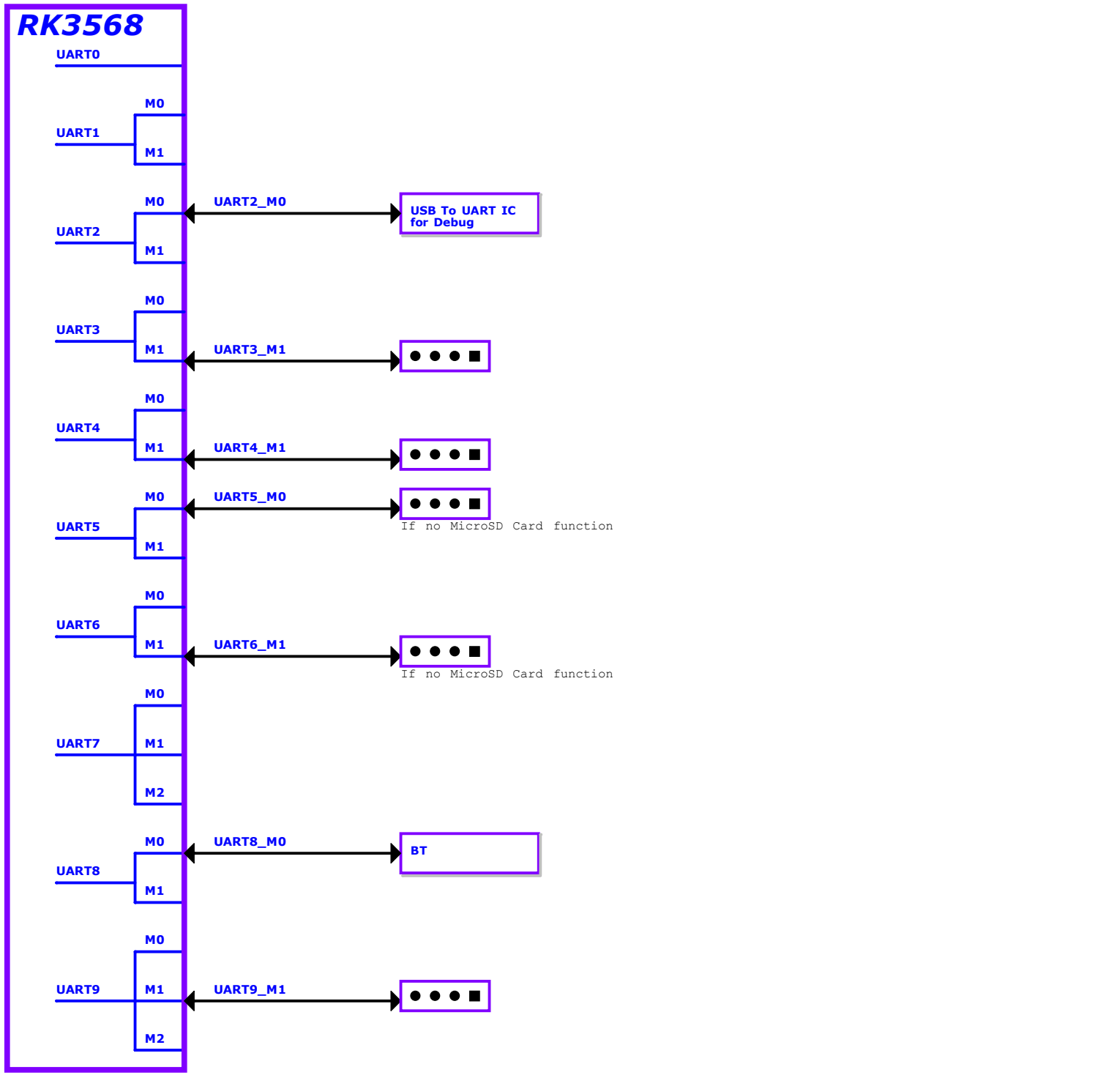

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Title: UART Map	
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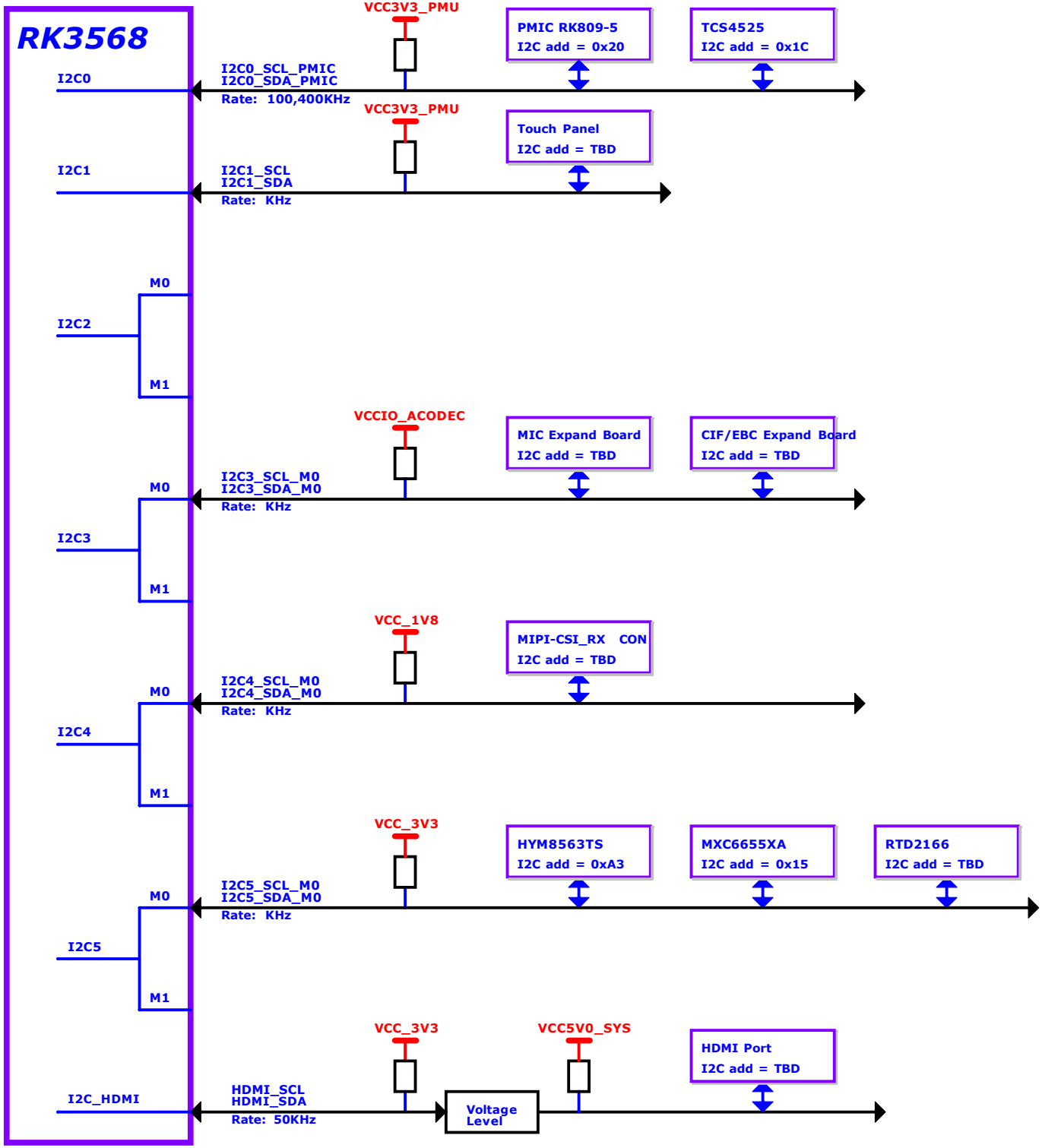
I2C MAP



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Title: I2C Bus Map		
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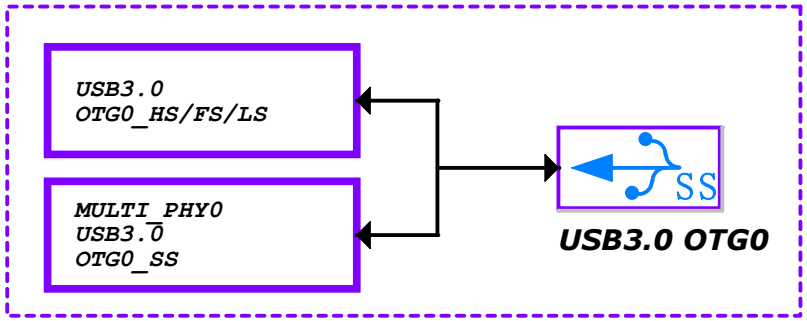
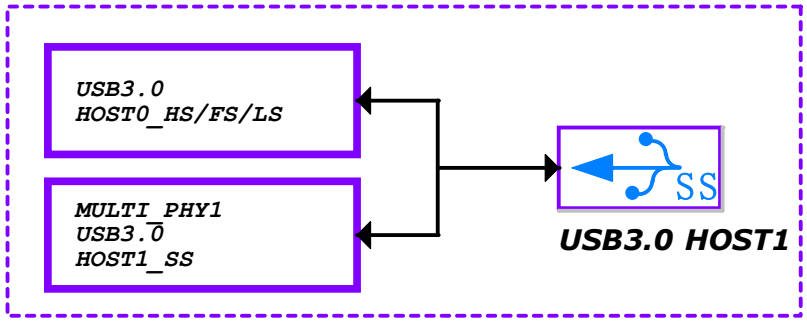
USB3.0 OTG0



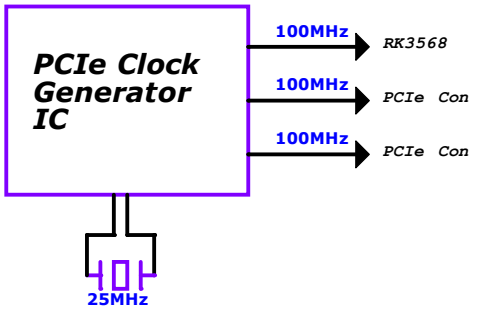
USB3.0 HOST1



PCIe3.0 PHY

Option1	PCIe3.0 x2Lane	PCIE30_REFCLK (RC/EP:input)	PCIE30_TX0 PCIE30_RX0 PCIE30_TX1 PCIE30_RX1	PCIE30X2_CLKREQn PCIE30X2_WAKEn PCIE30X2_PERSTn PCIE30X2_BUTTONRSTn	RC or EP
Option2	PCIe3.0 x1Lane + PCIe3.0 x1Lane	PCIE30_REFCLK (RC:input)	PCIE30_TX0 PCIE30_RX0	PCIE30X2_CLKREQn PCIE30X2_WAKEn PCIE30X2_PERSTn PCIE30X2_BUTTONRSTn	Only RC
			PCIE30_TX1 PCIE30_RX1	PCIE30X1_CLKREQn PCIE30X1_WAKEn PCIE30X1_PERSTn PCIE30X1_BUTTONRSTn	Only RC

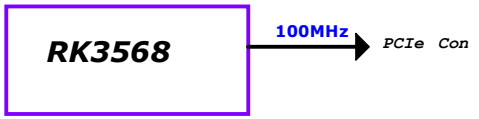
PCIe3.0 REFCLK



PCIe2.0 PHY

MULTI_ PHY2	PCIe2.0 x1Lane	PCIE20_REFCLK (RC:output)	PCIE20_TX PCIE20_RX	PCIE20_CLKREQn PCIE20_WAKEn PCIE20_PERSTn PCIE20_BUTTONRSTn	Only RC

PCIe2.0 REFCLK



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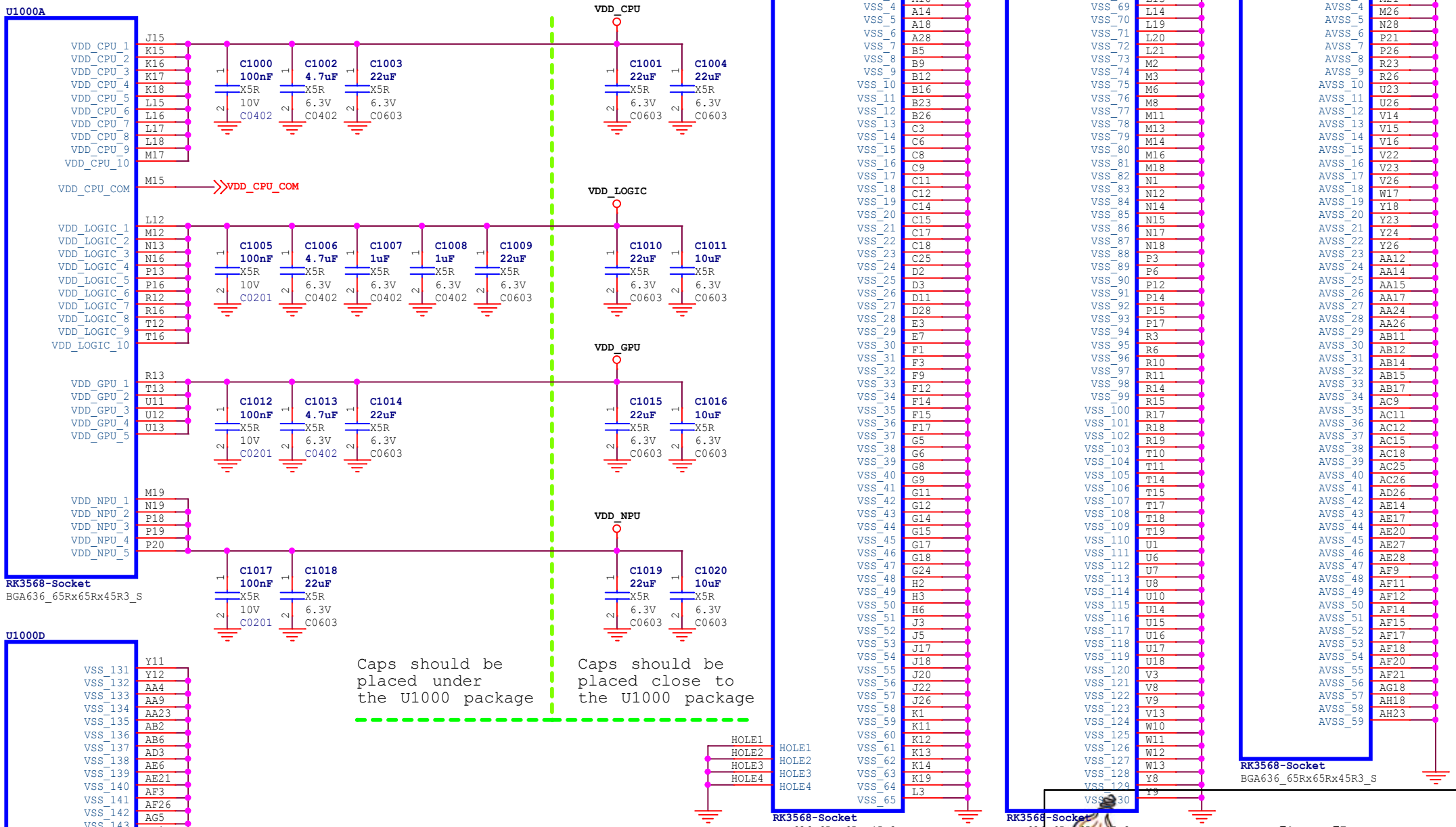
RK3568_ABCDE (Power&Gnd)



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Title: RK3568_Power/GND		
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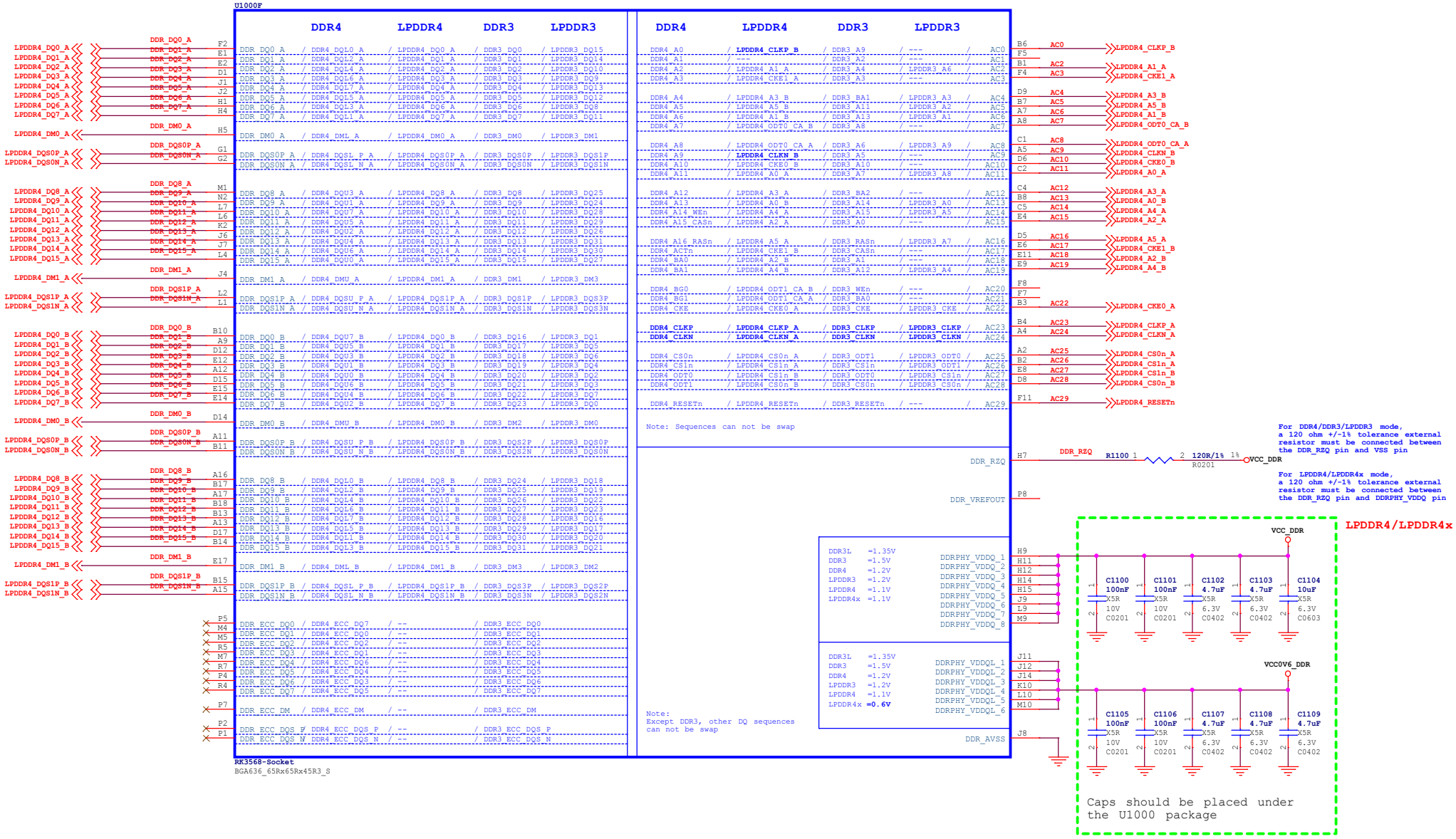
RK3568_F (DDR PHY)



For DDR4/DDR3/LPDDR3 mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_RZQ pin and VSS pin

For LPDDR4/LPDDR4x mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_RZQ pin and DDRPHY_VDDQ pin

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Title:	RK3568_DDR PHY
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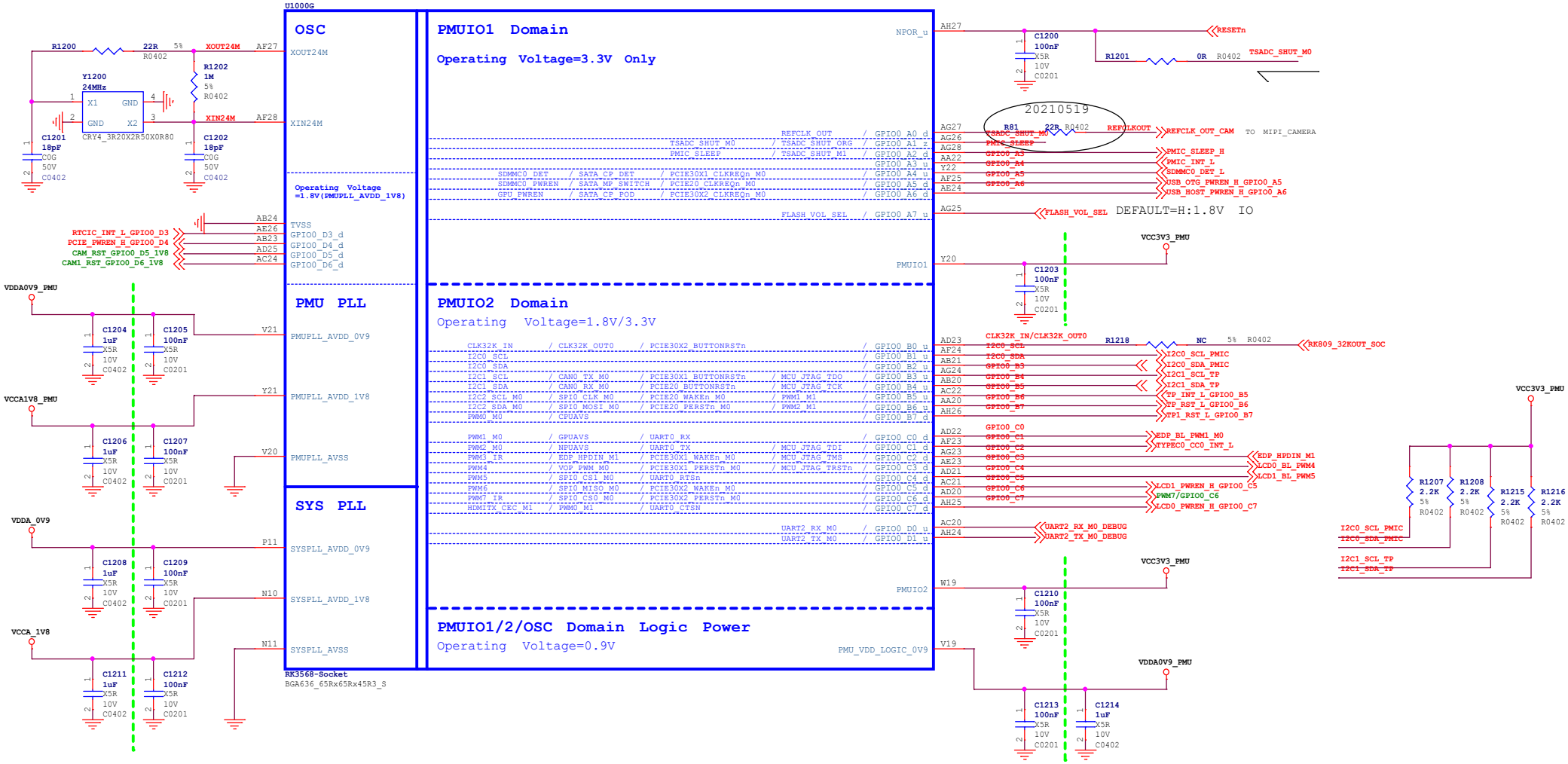
RK3568_G(OSC/PLL/PMUIO1/2)



Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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Title:	RK3568_OSC/PLL/PMUIO
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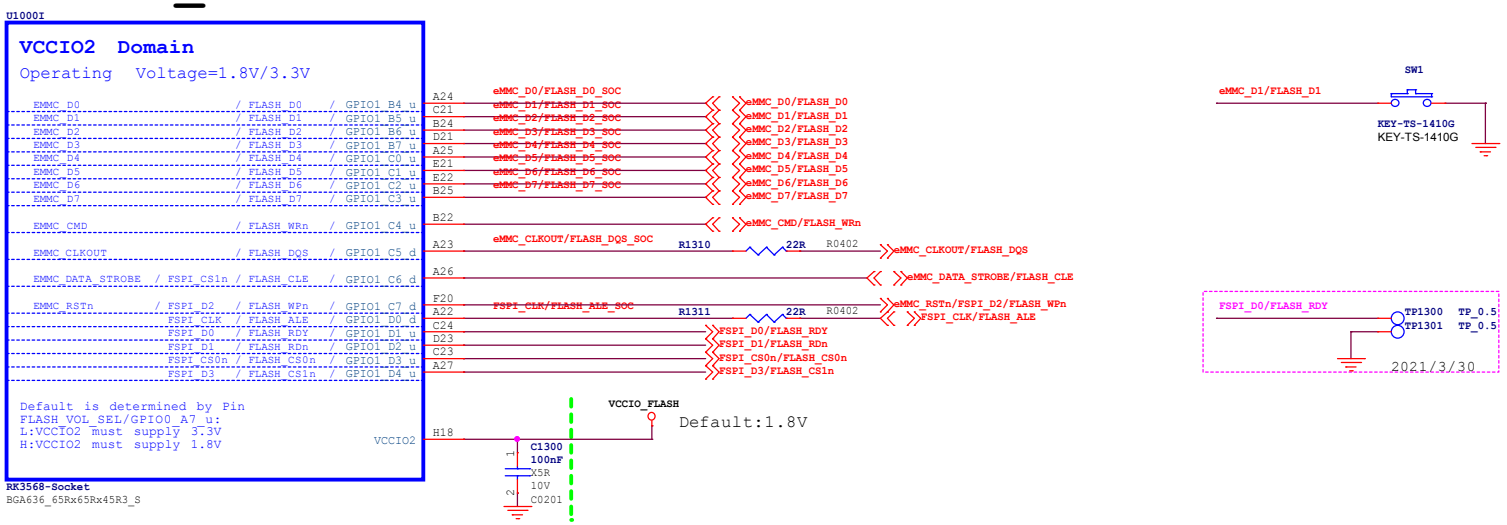
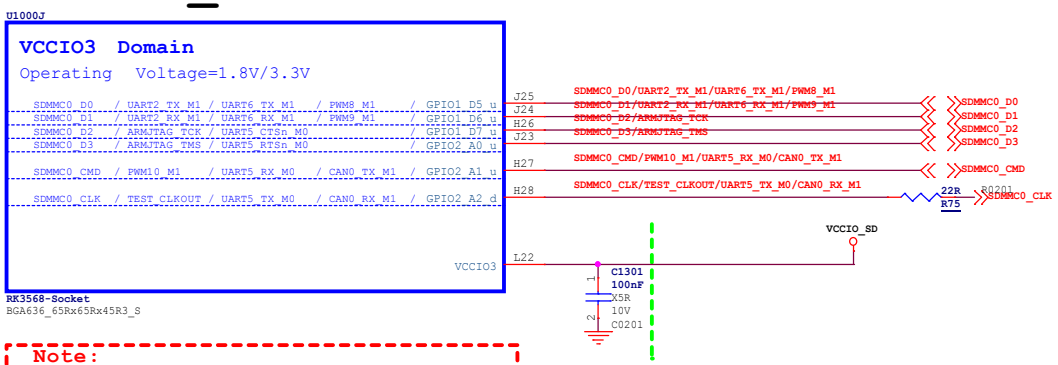
RK3568_I(VCCIO2 Domain)



RK3568_J(VCCIO3 Domain)



Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

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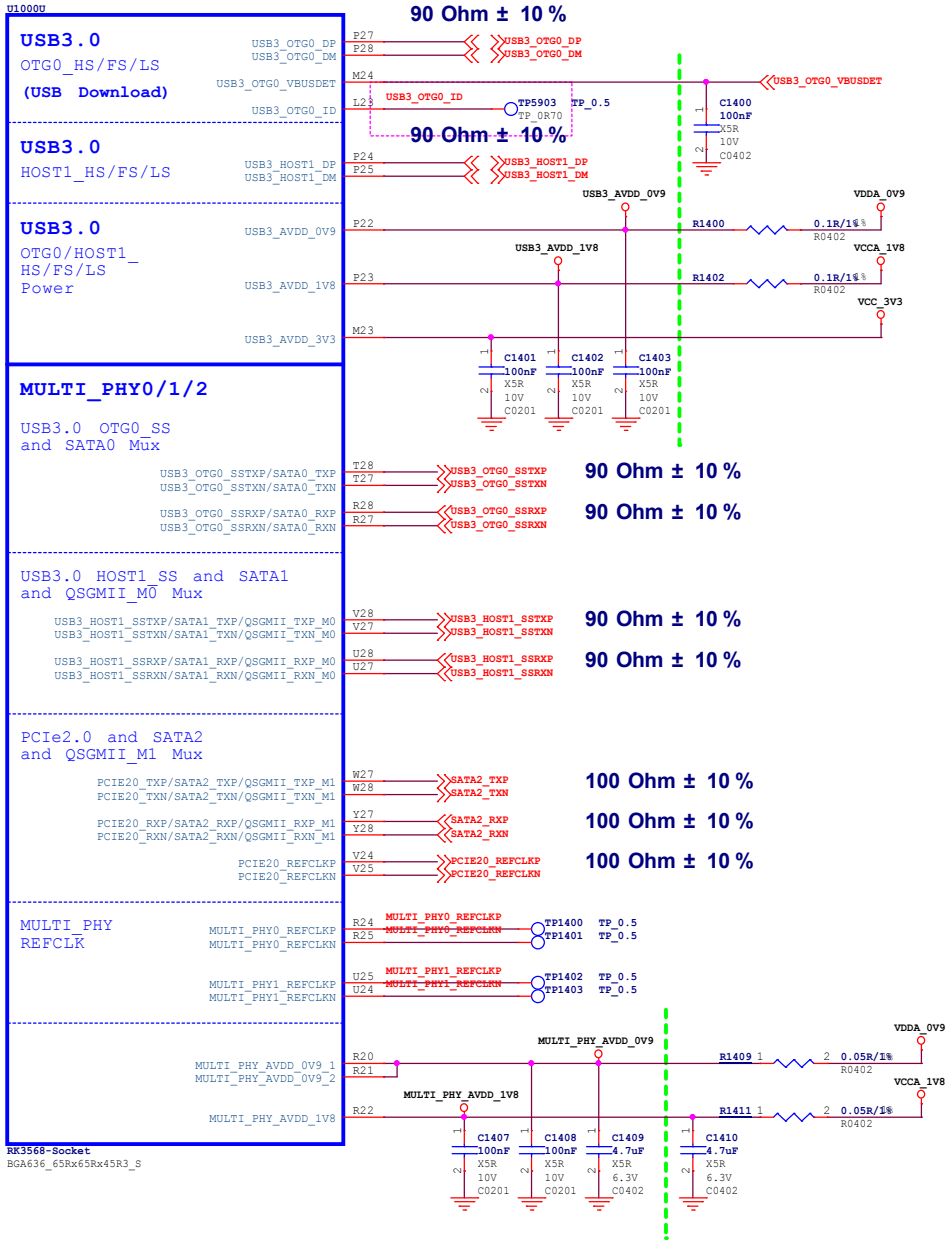
RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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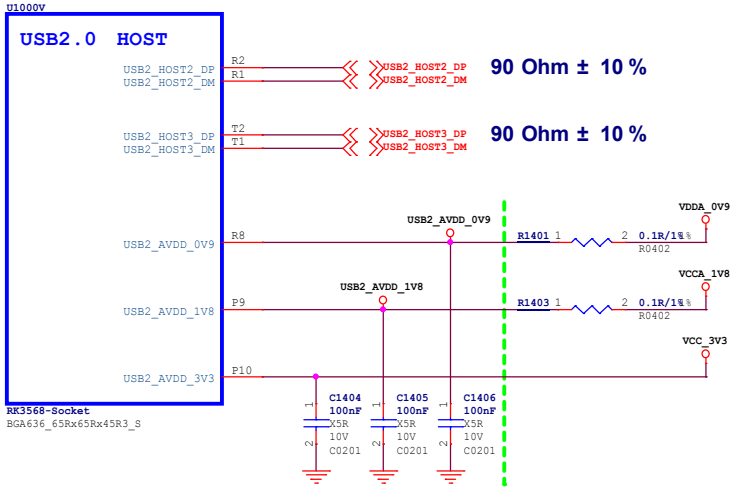
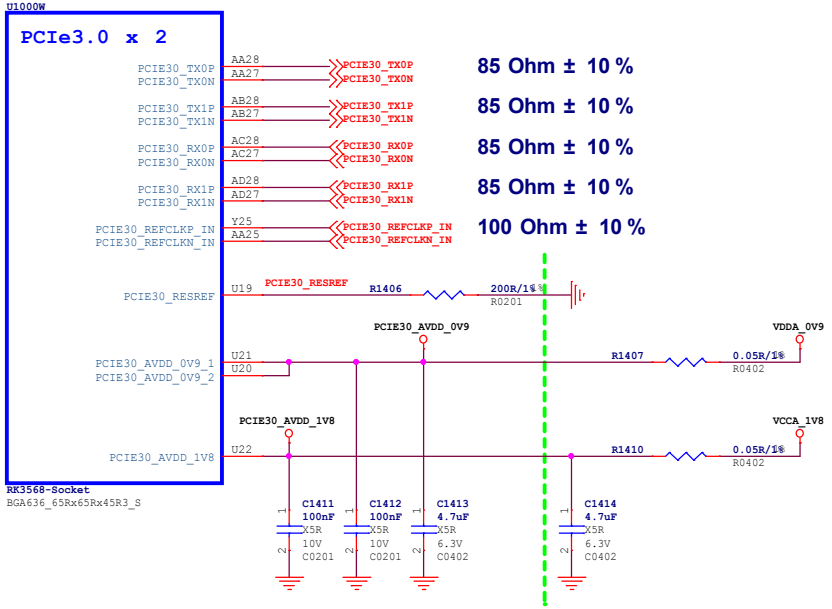
RK3568_V(USB2.0 HOST)



RK3568_W(PCIe3.0 x2)



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Title: RK3568_USB/PCIe/SATA_PHY		
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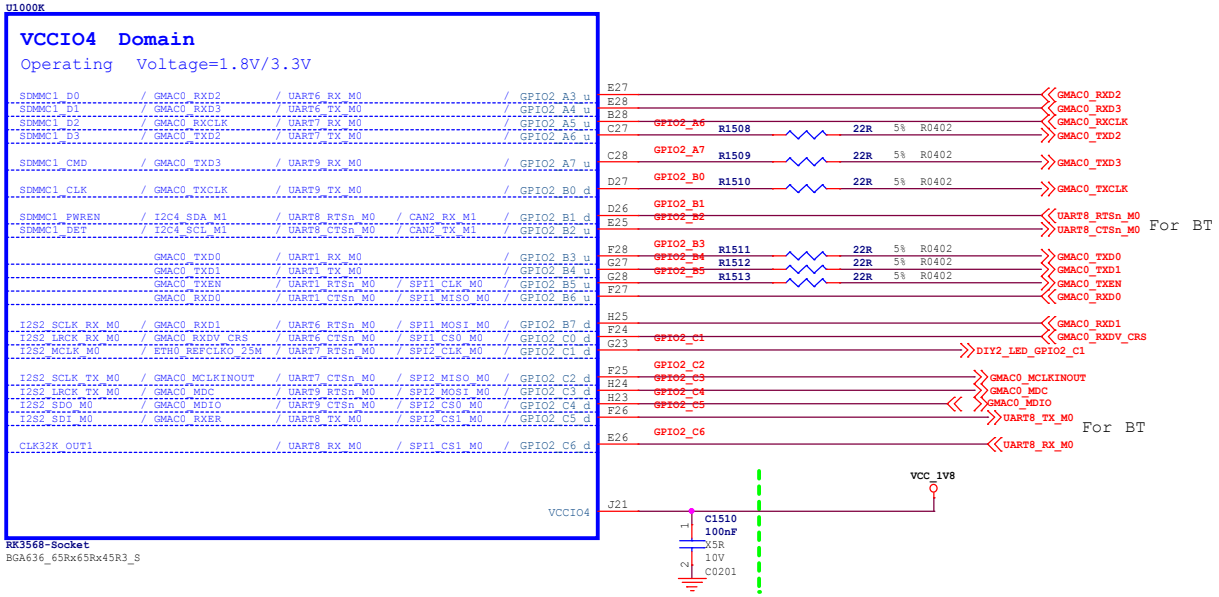
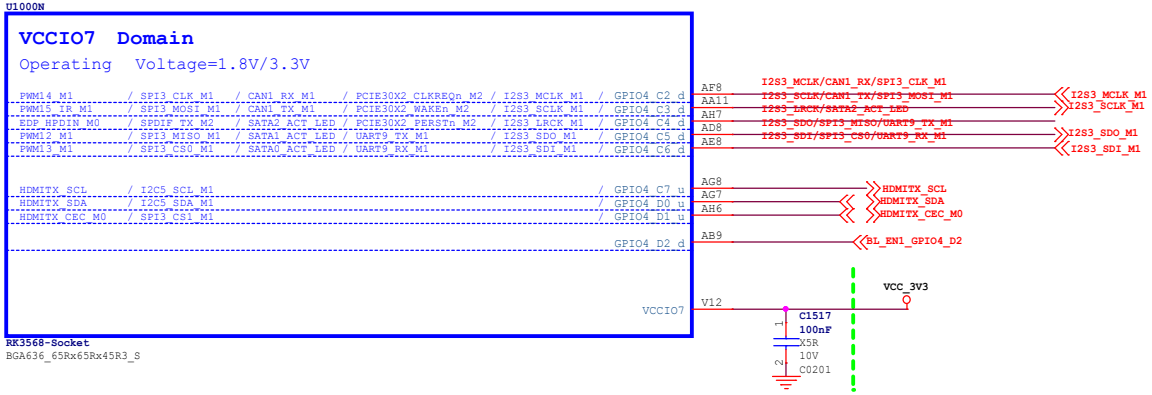
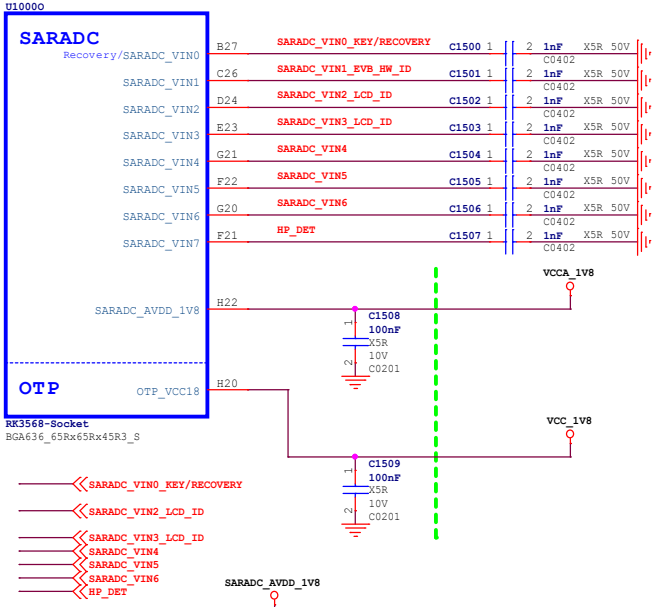
RK3568_K(VCCIO4 Domain)



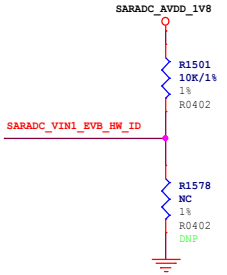
RK3568_N(VCCIO7 Domain)



RK3568_O(SARADC/OTP)



SARADC_VIN1_EVB_HW_ID	Rup	Rdown	ADC	
EVB1	10K	DNP	1023	1.8V
EVB2	20K	100K	852	1.5V
EVB3	18K	36K	681	1.2V
EVB4	51K	51K	512	0.9V
EVB5	36K	18K	340	0.6V
EVB6	100K	20K	170	0.3V
EVB7	DNP	10K	0	0V
EVB8				



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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Title: RK3568_SARADC/GPIO		
File: ROC-3568-PC		REV: V0.1
Create Date: Monday, March 30, 2020	Page Num: 15	
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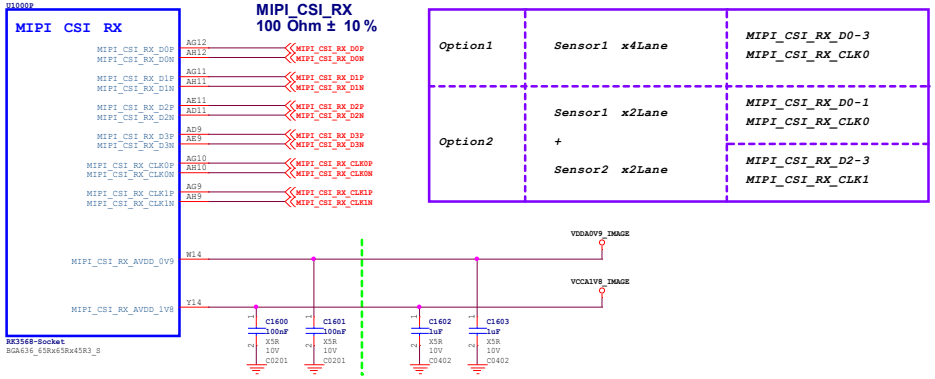
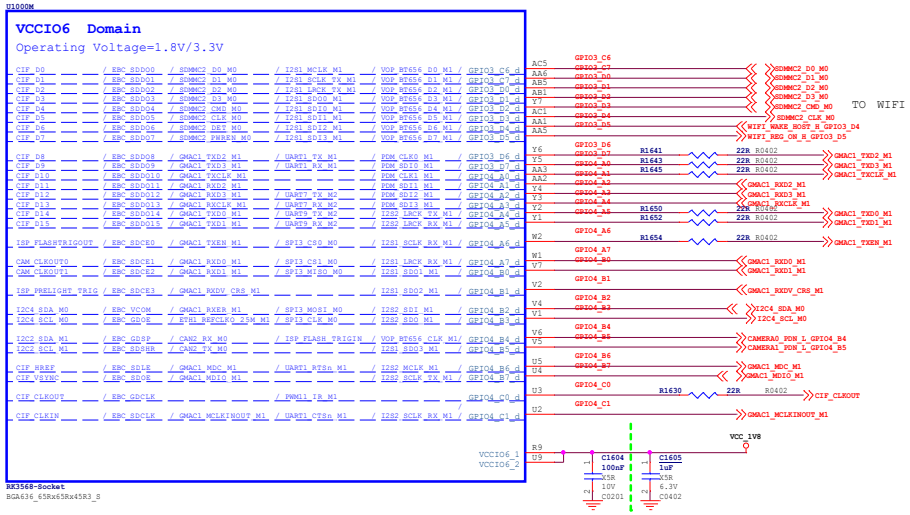
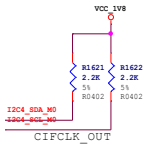
RK3568_P(MIPI_CSI_RX)



Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

RK3568_M(VCCIO6 Domain)





Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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Title:	RK3568 VI Interface	
File:	ROC-3568-PC	REV: V0.1
Create Date:	Monday, March 30, 2020	Page Num: 16
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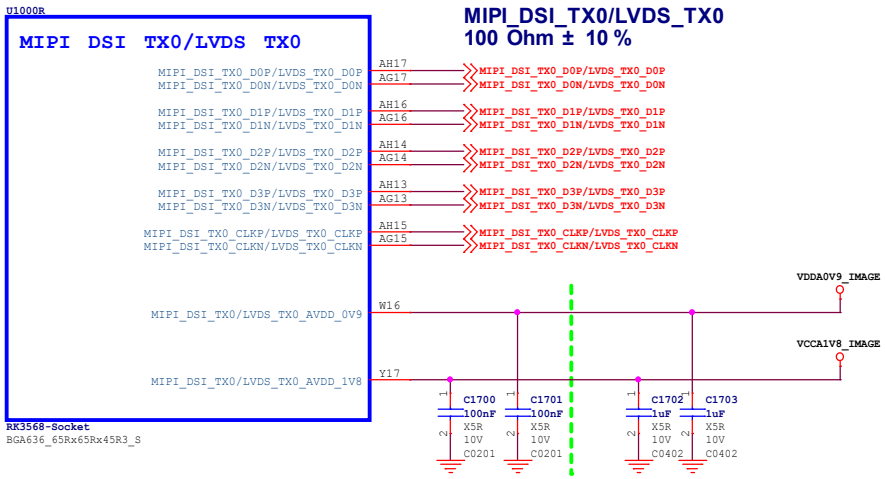
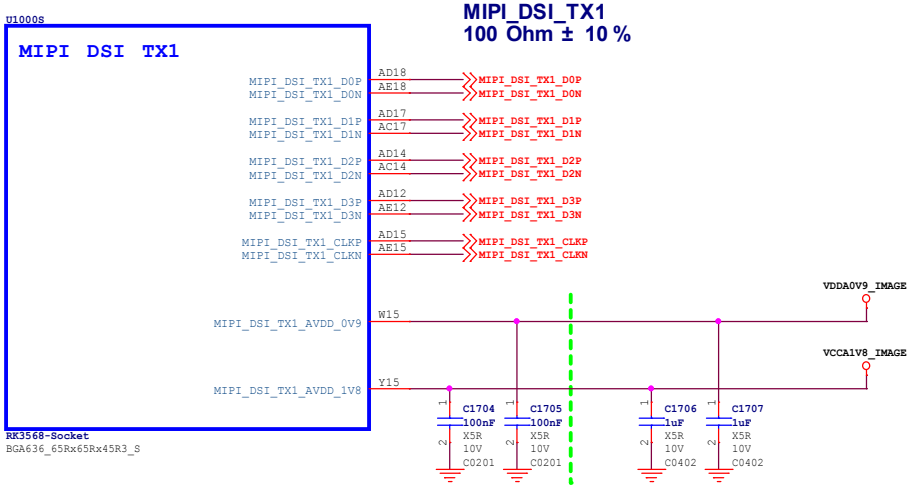
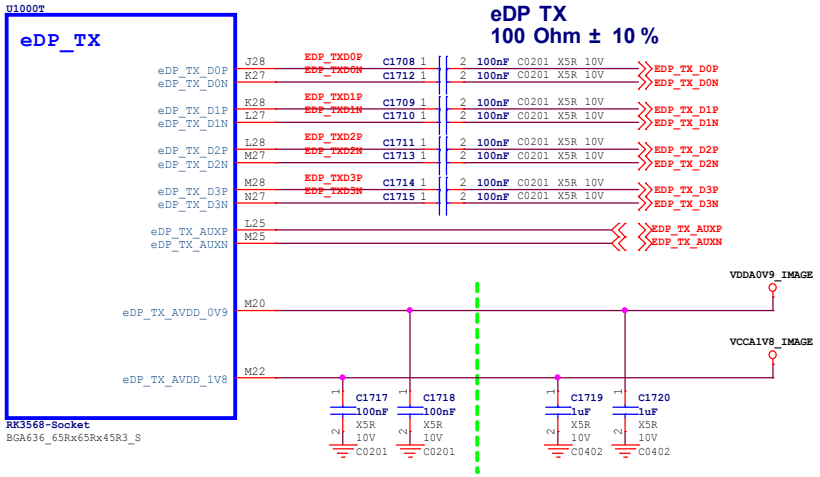
RK3568_R(MIPI_DSI_TX0/LVDS_TX0)



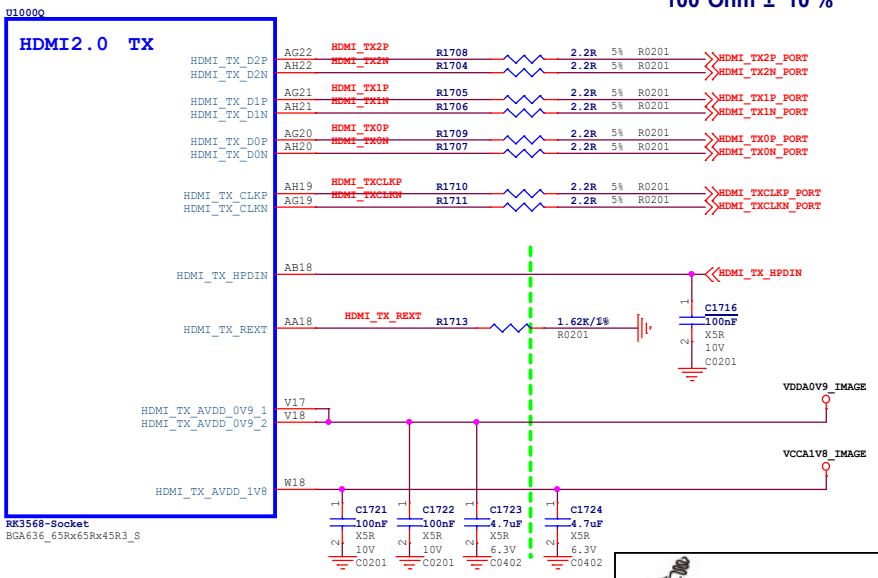
RK3568_S(MIPI_DSI_TX1)



RK3568_T(eDP TX)



RK3568_Q(HDMI2.0 TX)



Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

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Title: RK3568_V0 Interface_1		
File: ROC-3568-PC		REV: V0.1
Create Date: Monday, March 30, 2020	Page:	Num: 17
Modify Date: Wednesday, May 19, 2021	Page:	Total: 45

RK3568_L(VCCIO5 Domain)

U1000L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC_D0	/ VOP_BT656_D0_M0	/ SPI0_MISO_M1	/ PCIE20_CLKREQn_M1	/ I2S1_MCLK_M2	/ GPIO2_D0_d
LCDC_D1	/ VOP_BT656_D1_M0	/ SPI0_MOSI_M1	/ PCIE20_WAKEn_M1	/ I2S1_SCLK_TX_M2	/ GPIO2_D1_d
LCDC_D2	/ VOP_BT656_D2_M0	/ SPI0_CS0_M1	/ PCIE30X1_CLKREQn_M1	/ I2S1_LRCK_TX_M2	/ GPIO2_D2_d
LCDC_D3	/ VOP_BT656_D3_M0	/ SPI0_CLK_M1	/ PCIE30X1_WAKEn_M1	/ I2S1_SDI0_M2	/ GPIO2_D3_d
LCDC_D4	/ VOP_BT656_D4_M0	/ SPI2_CS1_M1	/ PCIE30X2_CLKREQn_M1	/ I2S1_SDI1_M2	/ GPIO2_D4_d
LCDC_D5	/ VOP_BT656_D5_M0	/ SPI2_CS0_M1	/ PCIE30X2_WAKEn_M1	/ I2S1_SDI2_M2	/ GPIO2_D5_d
LCDC_D6	/ VOP_BT656_D6_M0	/ SPI2_MOSI_M1	/ PCIE30X2_PERSTn_M1	/ I2S1_SDI3_M2	/ GPIO2_D6_d
LCDC_D7	/ VOP_BT656_D7_M0	/ SPI2_MISO_M1	/ UART8_TX_M1	/ I2S1_SDO0_M2	/ GPIO2_D7_d
LCDC_CLK	/ VOP_BT656_CLK_M0	/ SPI2_CLK_M1	/ UART8_RX_M1	/ I2S1_SDO1_M2	/ GPIO3_A0_d
LCDC_D8	/ VOP_BT1120_D0	/ SPI1_CS0_M1	/ PCIE30X1_PERSTn_M1	/ SDMMC2_D0_M1	/ GPIO3_A1_d
LCDC_D9	/ VOP_BT1120_D1	/ GMAC1_TXD2_M0	/ I2S3_MCLK_M0	/ SDMMC2_D1_M1	/ GPIO3_A2_d
LCDC_D10	/ VOP_BT1120_D2	/ GMAC1_TXD3_M0	/ I2S3_SCLK_M0	/ SDMMC2_D2_M1	/ GPIO3_A3_d
LCDC_D11	/ VOP_BT1120_D3	/ GMAC1_RXD2_M0	/ I2S3_LRCK_M0	/ SDMMC2_D3_M1	/ GPIO3_A4_d
LCDC_D12	/ VOP_BT1120_D4	/ GMAC1_RXD3_M0	/ I2S3_SDO_M0	/ SDMMC2_CMD_M1	/ GPIO3_A5_d
LCDC_D13	/ VOP_BT1120_CLK	/ GMAC1_TXCLK_M0	/ I2S3_SDI_M0	/ SDMMC2_CLK_M1	/ GPIO3_A6_d
LCDC_D14	/ VOP_BT1120_D5	/ GMAC1_RXCLK_M0		/ SDMMC2_DET_M1	/ GPIO3_A7_d
LCDC_D15	/ VOP_BT1120_D6	/ ETH1_REFCLKO_25M_M0		/ SDMMC2_PWREN_M1	/ GPIO3_B0_d
LCDC_D16	/ VOP_BT1120_D7	/ GMAC1_RXD0_M0	/ UART4_RX_M1	/ PWM8_M0	/ GPIO3_B1_d
LCDC_D17	/ VOP_BT1120_D8	/ GMAC1_RXD1_M0	/ UART4_TX_M1	/ PWM9_M0	/ GPIO3_B2_d
LCDC_D18	/ VOP_BT1120_D9	/ GMAC1_RXDV_CRS_M0	/ I2C5_SCL_M0	/ PDM_SDI0_M2	/ GPIO3_B3_d
LCDC_D19	/ VOP_BT1120_D10	/ GMAC1_RXER_M0	/ I2C5_SDA_M0	/ PDM_SDI1_M2	/ GPIO3_B4_d
LCDC_D20	/ VOP_BT1120_D11	/ GMAC1_TXD0_M0	/ I2C3_SCL_M1	/ PWM10_M0	/ GPIO3_B5_d
LCDC_D21	/ VOP_BT1120_D12	/ GMAC1_TXD1_M0	/ I2C3_SDA_M1	/ PWM11_IR_M0	/ GPIO3_B6_d
LCDC_D22	/ PWM12_M0	/ GMAC1_TXEN_M0	/ UART3_TX_M1	/ PDM_SDI2_M2	/ GPIO3_B7_d
LCDC_D23	/ PWM13_M0	/ GMAC1_MCLKINOUT_M0	/ UART3_RX_M1	/ PDM_SDI3_M2	/ GPIO3_C0_d
LCDC_HSYNC	/ VOP_BT1120_D13	/ SPI1_MOSI_M1	/ PCIE20_PERSTn_M1	/ I2S1_SDO2_M2	/ GPIO3_C1_d
LCDC_VSYNC	/ VOP_BT1120_D14	/ SPI1_MISO_M1	/ UART5_TX_M1	/ I2S1_SDO3_M2	/ GPIO3_C2_d
LCDC_DEN	/ VOP_BT1120_D15	/ SPI1_CLK_M1	/ UART5_RX_M1	/ I2S1_SCLK_RX_M2	/ GPIO3_C3_d
PWM14_M0	/ VOP_PWM_M1	/ GMAC1_MDC_M0	/ UART7_TX_M1	/ PDM_CLK1_M2	/ GPIO3_C4_d
PWM15_IR_M0	/ SPDIF_TX_M1	/ GMAC1_MDIO_M0	/ UART7_RX_M1	/ I2S1_LRCK_RX_M2	/ GPIO3_C5_d

VCCIO5_1
VCCIO5_2

RK3568-Socket
BGA636_65Rx65Rx45R3_S

AG6 GMAC1_INT/PMEB_GPIO2_D0
AD7 GMAC1_RSTn_GPIO2_D1
AC8 GMAC0_INT/PMEB_GPIO2_D2
AC7 GMAC0_RSTn_GPIO2_D3
AF5 PCIE30X2_CLKREQn_M1
AF6 PCIE30X2_WAKEn_M1
AD6 PCIE30X2_PERSTn_M1
AH5 TP1_INT_GPIO2_D7_3V3

AH4 BT_REG_ON_H_GPIO3_A0
AB8 BT_WAKE_HOST_H_GPIO3_A1
AE5 HOST_WAKE_BT_H_GPIO3_A2
AG4 I2S3_SCLK_M0
AF4 I2S3_LRCK_M0
AH3 I2S3_SDO_M0
AG3 I2S3_SDI_M0
for BT

AH2 PCIECLKIC_OE_H_GPIO3_A7
AG2 BL_EN0_GPIO3_B0

AG1 UART4_RX_M1
AF2 UART4_TX_M1
AF1 I2C5_SCL_M0
AE1 I2C5_SDA_M0
AE2 LCD0_RST_GPIO3_B5
AE3 LCD1_RST_GPIO3_B6
AD4 UART3_TX_M1
AD2 UART3_RX_M1

AD1 GSENSOR_INT_L_GPIO3_C1
AA7 USB30_SW_GPIO3_C2
AC4 EDP_BL_EN

AC3 UART7_TX_M1/PWM14_M0
AC2 UART7_RX_M1/SPDIF_TX_M1
PWM14_M0
SPDIF_TX_M1

V10
V11
VCC_3V3
C1800 100nF X5R 10V C0201
C1801 1uF X5R 6.3V C0402 DNP

VCC_3V3
R1800 10K 5% R0402 GMAC1_INT/PMEB_GPIO2_D0
R1801 10K 5% R0402 GMAC0_INT/PMEB_GPIO2_D2
od

VCC_3V3
R1802 2.2K 5% R0402 I2C5_SCL_M0
R1803 2.2K 5% R0402 I2C5_SDA_M0

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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Title: RK3568_V0 Interface_2		
File: ROC-3568-PC		REV: V0.1
Create Date: Wednesday, May 06, 2020	Page Num: 18	
Modify Date: Wednesday, May 19, 2021	Page Total: 45	

RK3568_H(VCCIO1 Domain)

U1000H

VCCIO1 Domain

Operating Voltage=1.8V/3.3V

I2C3_SDA_M0	/ UART3_RX_M0	/ CAN1_RX_M0	/ AUDIOPWM_LOUT_P	/ ACODEC_ADC_DATA	/ GPIO1_A0_u
I2C3_SCL_M0	/ UART3_TX_M0	/ CAN1_TX_M0	/ AUDIOPWM_LOUT_N	/ ACODEC_ADC_CLK	/ GPIO1_A1_u
I2S1_MCLK_M0	/ UART3_RTSn_M0	/ SCR_CLK	/ PCIE30X1_PERSTn_M2		/ GPIO1_A2_d
I2S1_SCLK_TX_M0	/ UART3_CTSn_M0	/ SCR_IO	/ PCIE30X1_WAKEn_M2	/ ACODEC_DAC_CLK	/ GPIO1_A3_d
I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0	/ SPDIF_TX_M0		/ GPIO1_A4_d
I2S1_LRCK_TX_M0	/ UART4_RTSn_M0	/ SCR_RST	/ PCIE30X1_CLKREQn_M2	/ ACODEC_DAC_SYNC	/ GPIO1_A5_d
I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0	/ AUDIOPWM_ROUT_P		/ GPIO1_A6_d
I2S1_SDO0_M0	/ UART4_CTSn_M0	/ SCR_DET	/ AUDIOPWM_ROUT_N	/ ACODEC_DAC_DATAL	/ GPIO1_A7_d
I2S1_SDO1_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0	/ PCIE20_CLKREQn_M2	/ ACODEC_DAC_DATAR	/ GPIO1_B0_d
I2S1_SDO2_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0	/ PCIE20_WAKEn_M2	/ ACODEC_ADC_SYNC	/ GPIO1_B1_d
I2S1_SDO3_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0	/ PCIE20_PERSTn_M2		/ GPIO1_B2_d
	I2S1_SDI0_M0	/ PDM_SDI0_M0			/ GPIO1_B3_d

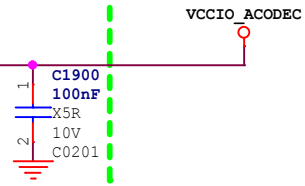
VCCIO1

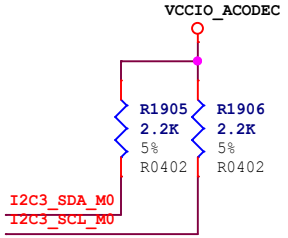
RK3568-Socket

BGA636_65Rx65Rx45R3_S

Default:RK809+PDM MIC

D18	I2C3_SDA	I2C3_SDA_M0
E18	I2C3_SCL	I2C3_SCL_M0
A19	I2S1_MCLK_M0	I2S1_MCLK_M0_RK809
B19	I2S1_SCLK_TX_M0	I2S1_SCLK_TX_M0_RK809
F18	I2S1_SCLK_RX_M0/PDM_CLK1_M0/GPIO1_A4	HUB_RST_GPIO1_A4_d
A20	I2S1_LRCK_TX_M0	I2S1_LRCK_TX_M0_RK809
C20	I2S1_LRCK_RX_M0/PDM_CLK0_M0	PDM_CLK0_M0_RK809
B20	I2S1_SDO0_M0	I2S1_SDO0_M0_RK809
D20	GPIO1_B0	DIY1_LED_GPIO1_B0
E20	GPIO1_B1	WORK_LED_GPIO1_B1
A21	GPIO1_B2	DIY_LED_GPIO1_B2
B21	I2S1_SDI0_M0/PDM_SDI0_M0	I2S1_SDI0_M0/PDM_SDI0_M0_RK809





Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

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Title: RK3568 Audio Interface		
File: ROC-3568-PC		REV: V0.1
Create Date: Monday, March 30, 2020	Page Num: 19	
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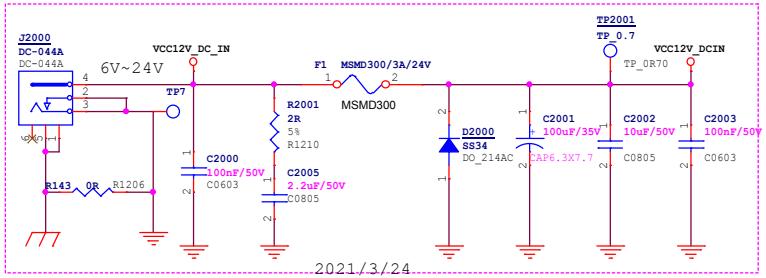
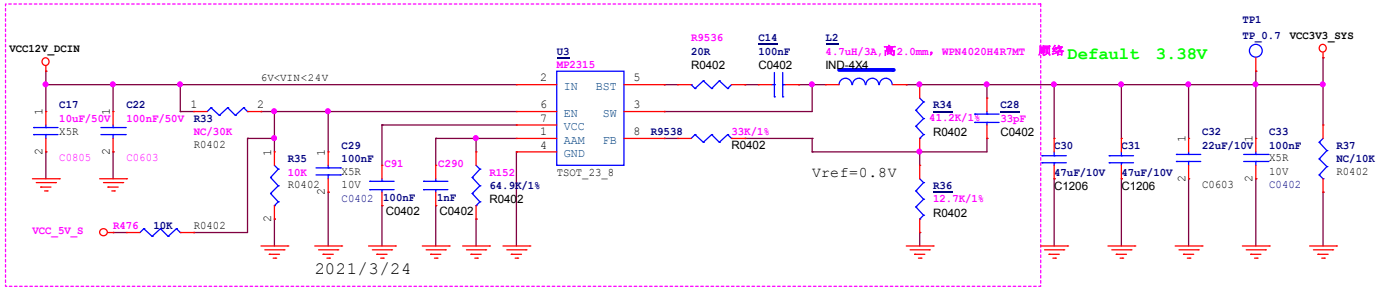
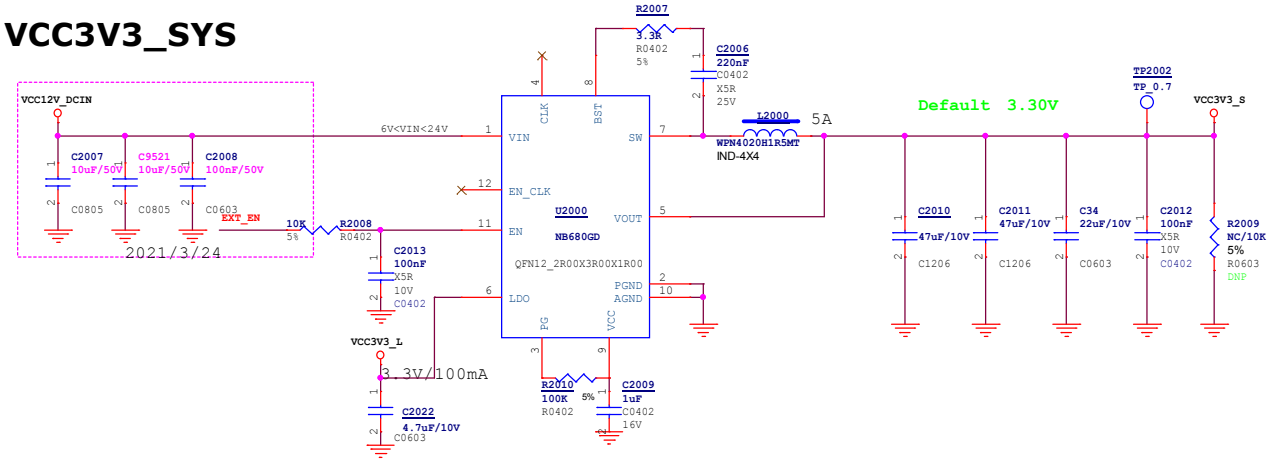
12V/3A DCIN

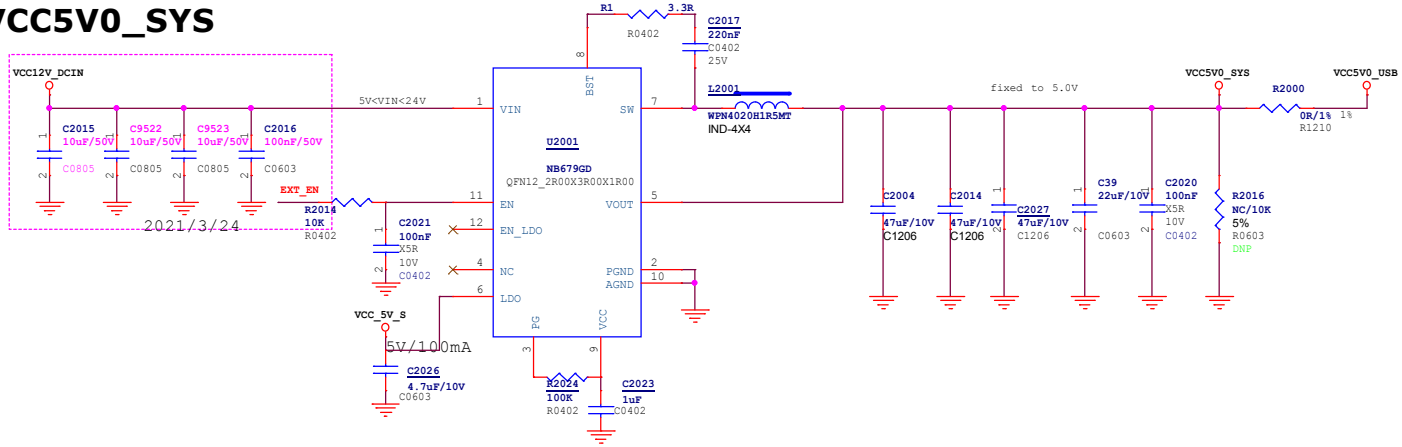




VCC3V3_SYS



VCC5V0_SYS



EXT_EN

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Title: Power_DC IN		
File: ROC-3568-PC		REV: V0.1
Create Date: Monday, May 18, 2020	Page	Num: 20
Modify Date: Wednesday, May 19, 2021	Page	Total: 45

I2C0_SCL_PMIC
I2C0_SDA_PMIC
PMIC_INT_L
PMIC_SLEEP_H
RK809_32KOUT_WIFI
RK809_32KOUT_SOC
RESETn
VDD_CPU_COM
I2S1_MCLK_M0_RK809
I2S1_SCLK_TX_M0_RK809
I2S1_LRCK_TX_M0_RK809
I2S1_SDO0_M0_RK809
I2S1_SDI0_M0/PDM_SDI0_M0_RK809
PDM_CLK0_M0_RK809
EXT_EN
HPL_OUT
HP_SNS
HPR_OUT
SPKN_OUT
SPKP_OUT
MIC1_INP
MIC1_INN
PWRON_KEY
RESET_KEY

OUT
VDD
FB
100R
BUCK4
RK3568

PMIC RK809 DCDC

VDD_LOGIC
VDD_GPU
VDD_NPU
VCC_DDR
VCC3V3_SYS
U2100A
RK809-5
QFN68_7R00X7R00X0R80_T
L2100 470nH SW1 IND_252010 DCR<50mohm
L2102 470nH SW2 IND_252010 DCR<50mohm
L2101 470nH IND_252010 DCR<50mohm
L2103 470nH IND_252010 DCR<50mohm
R79 560R
R80 9.1K/1%
Feedback from RK3568
2021.5.19
DDR4
R2118 51K/1%
R2121 120K/1%
2021/3/24

DDR4	1.21V	62K 1%
LPDDR4/4x	1.11V	47K 1%
DDR3	1.53V	110K 1%
DDR3L	1.35V	82K 1%
LPDDR3	1.25V	68K 1%

VDD
Pin
OUT
FB
100R
RK3568
BUCK1/BUCK2

PMIC RK809 LDO

U2100B
400mA LDO: 400mA@Vin>3V 200mA@Vin>2V
VCC3V3_SYS
LDO1 400mA
LDO2 400mA
Low noise LDO3 100mA
Codec vddio LDO4 400mA
LDO5 400mA
LDO6 400mA
LDO7 400mA
LDO8 400mA
LDO9 400mA
2.1A SWOUT2
2.1A SWOUT1
BUCK5 1.5V-3.6V 2.5A
VCC8\9: 2.7V-5.5V
VDDA0V9_IMAGE
VDDA_0V9
VDDA0V9_PMU
VCCIO_ACODEC
VCCIO_SD
VCC3V3_PMU
VCCA_1V8
VCCA1V8_PMU
VCCA1V8_IMAGE
VCC3V3_SD
VCC_3V3
VCC_1V8
RK809-5
QFN68_7R00X7R00X0R80_T
L2104 470nH IND_252010 DCR<50mohm
R2122 0R
R2123 DNP
<Tolerance>

PMIC RK809 Management

U2100C
VCC3V3_PMU
VCCIO_WL
Y2100 32.768KHz CRY2_6R90X1R40X1R30
I2C0_SDA_PMIC
I2C0_SCL_PMIC
SDA_809
SCL_809
PMIC_INT_L
PMIC_SLEEP_H
RK809_CLK32KOUT
RESETn
RK809_VREF
Gas Gauge
2021/3/24
VCC_5V_S
1.2V
RK809_PWRON
EXT_EN
RESET_KEY
PWRON_KEY
SW2100
KEY-TS-1410G
KEY_4PIN
D2100 ESD5451N
D2101 ESD5451N
ESD0402
RK809-5
QFN68_7R00X7R00X0R80_T

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PMIC RK809 CODEC

VCC5V0_SYS
FB2100 120R-100MHz
U2100D
VCC_SPK_HP
CPn
CPp
VCC_CPVDD
VCC_CPVSS
VCC_1P8D
VCC_1P8A
MCLK
BCLK
LRCLK
SDI
SDO/PDMDATA
PDMCLK
HPL_OUT
HP_SNS
HPR_OUT
SPK_OUTn
SPK_OUTp
MIC1p MIC_L
MIC1n MIC_R
SPKN FB2101 180R-100M
SPKP FB2102 180R-100M
RK809-5
QFN68_7R00X7R00X0R80_T

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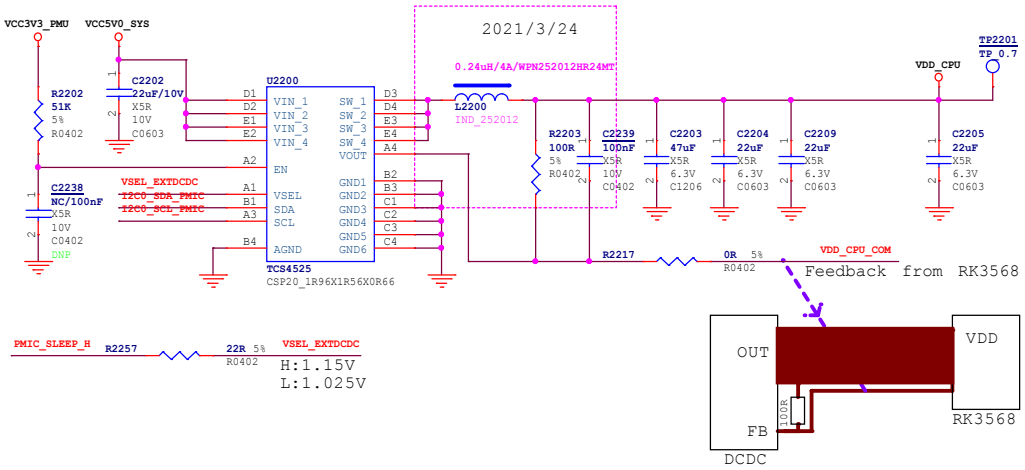
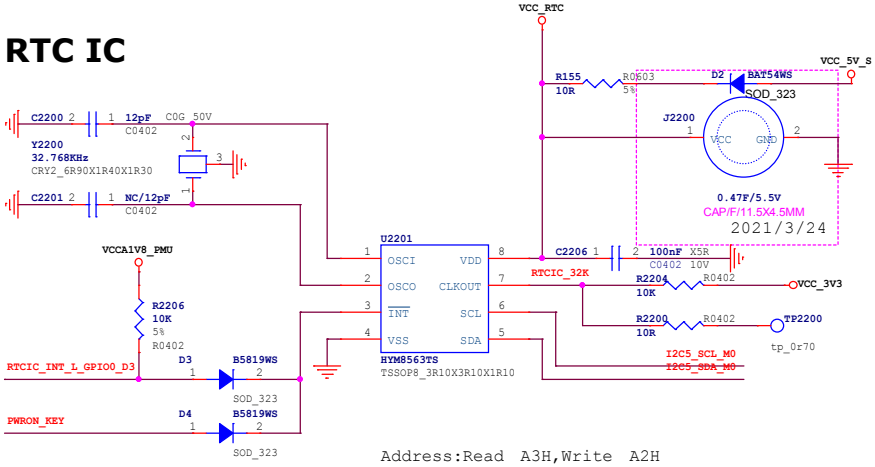
Title:	Power_PMIC
File:	ROC-3568-PC
REV:	V0.1
Create Date:	Monday, May 18, 2020
Page:	Num: 21
Modify Date:	Wednesday, May 19, 2021
Page:	Total: 45

PMIC_SLEEP_H
VDD_CPU_COM
PWRON_KEY
I2C0_SCL_PMIC
I2C0_SDA_PMIC
RTCIC_INT_L_GPIO0_D3
I2C5_SCL_M0
I2C5_SDA_M0

VDD_CPU



RTC IC



Address:Read A3H,Write A2H

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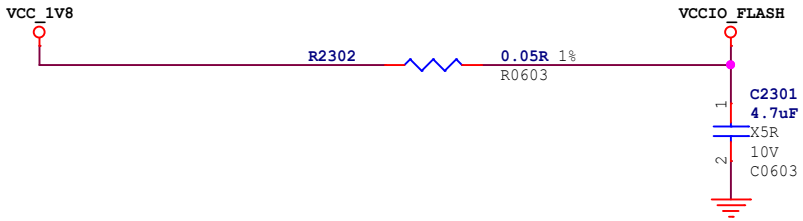
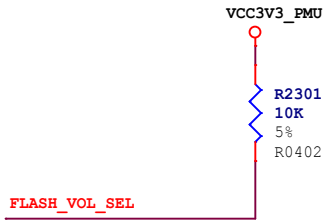
Title: Power_other		
File: ROC-3568-PC		REV: V0.1
Create Date: Monday, May 18, 2020	Page:	Num: 22
Modify Date: Wednesday, May 19, 2021	Page:	Total: 45

FLASH_VOL_SEL

Flash Power Manage

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)





Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L:3.3V IO driven
Logic=H:1.8V IO driven

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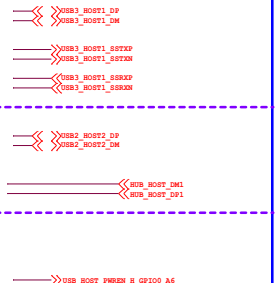
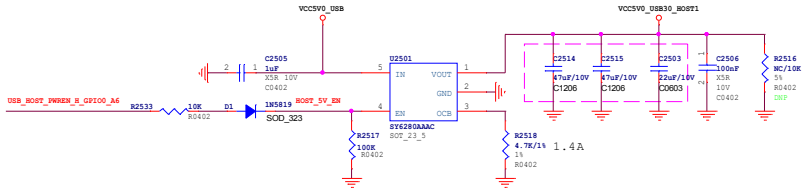
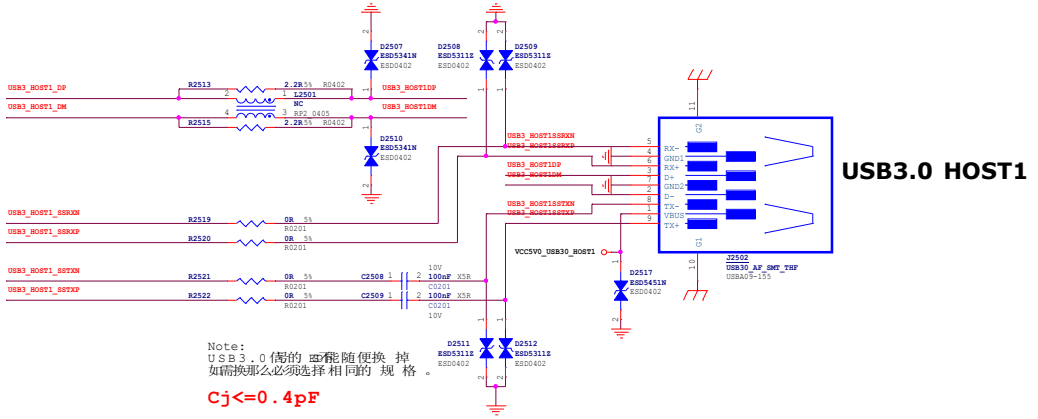
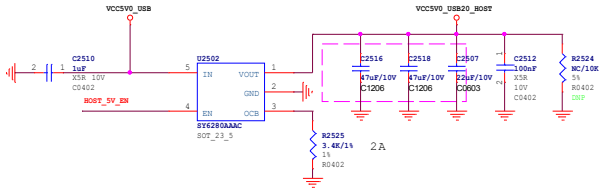
Title: Power_Flash Power Manage	
File: ROC-3568-PC	REV: V0.1
Create Date: Tuesday, May 19, 2020	Page Num: 23
Modify Date: Wednesday, May 19, 2021	Page Total: 45



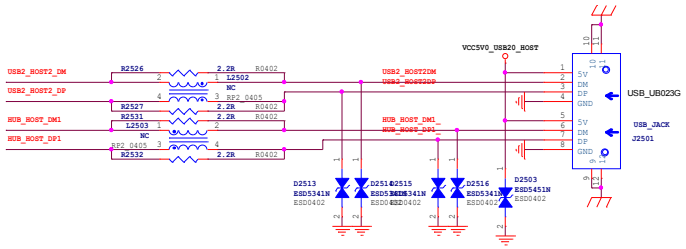




USB3.0 HOST1



USB2.0 HOST2
USB2.0 HOST3



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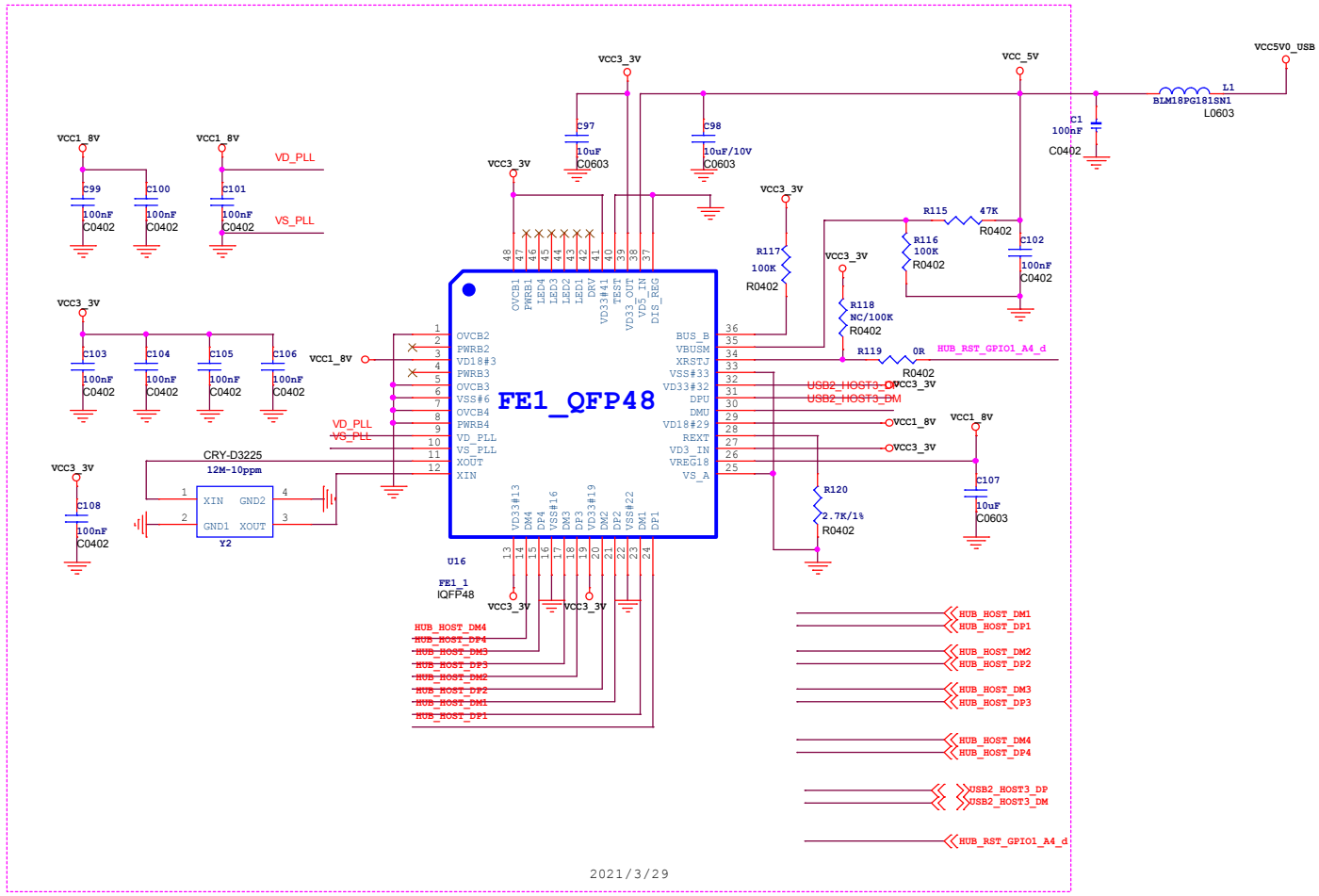
Title:	USB2/USB3 Port	
File:	ROC-3568-PC	REV: V0.1
Create Date:	Tuesday, March 31, 2020	Page Num: 24
Modify Date:	Wednesday, May 19, 2021	Page Total: 45

USB2.0 HUB



Title:	USB2.0 HUB GL850G
File:	ROC-3568-PC
REV:	V0.1
Create Date:	Wednesday, November 04, 2020
Page Num:	25
Modify Date:	Wednesday, May 19, 2021
Page Total:	45

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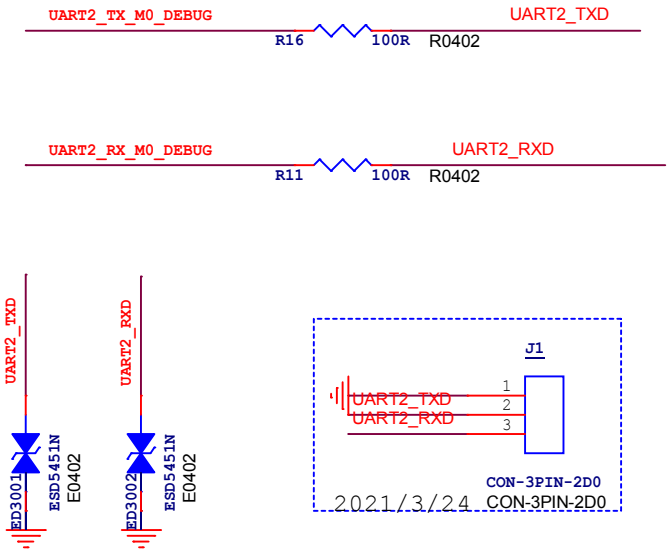
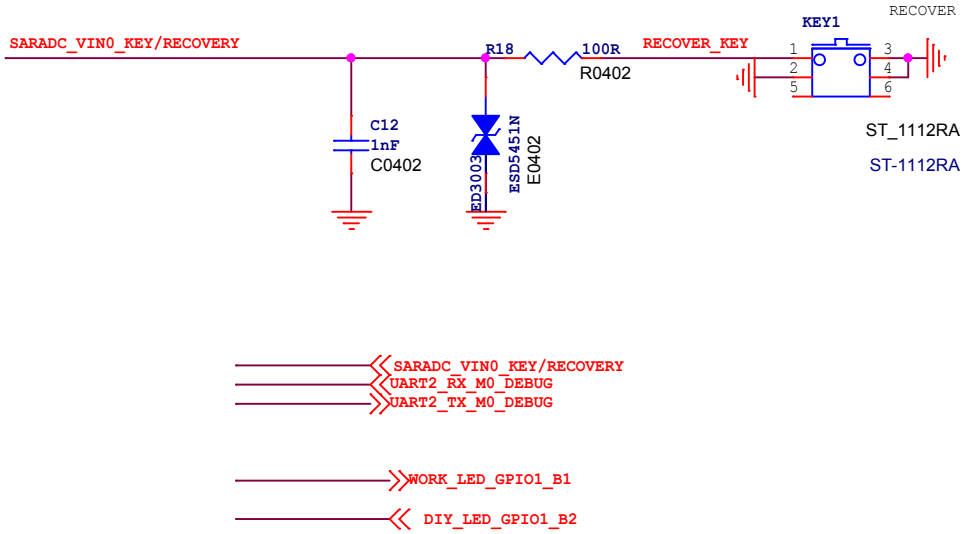
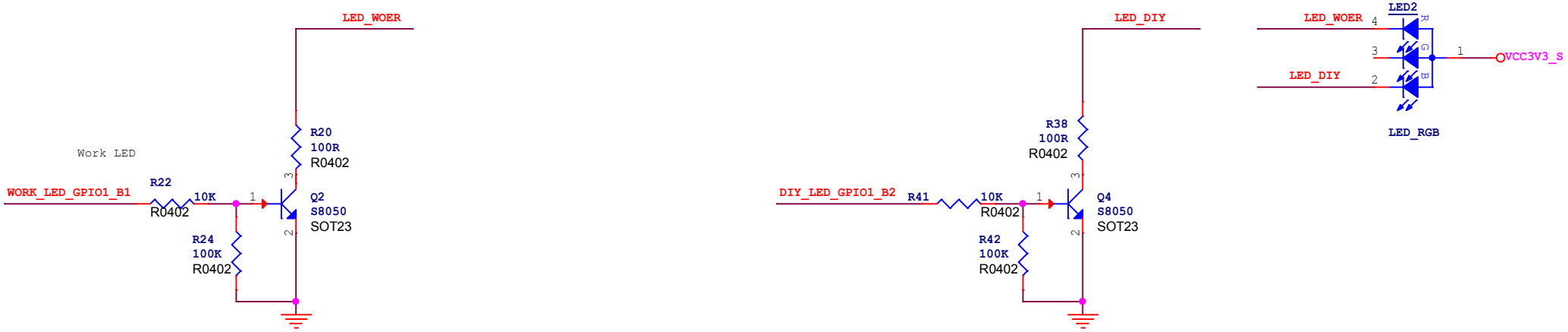
DEBUG



KEY



LED



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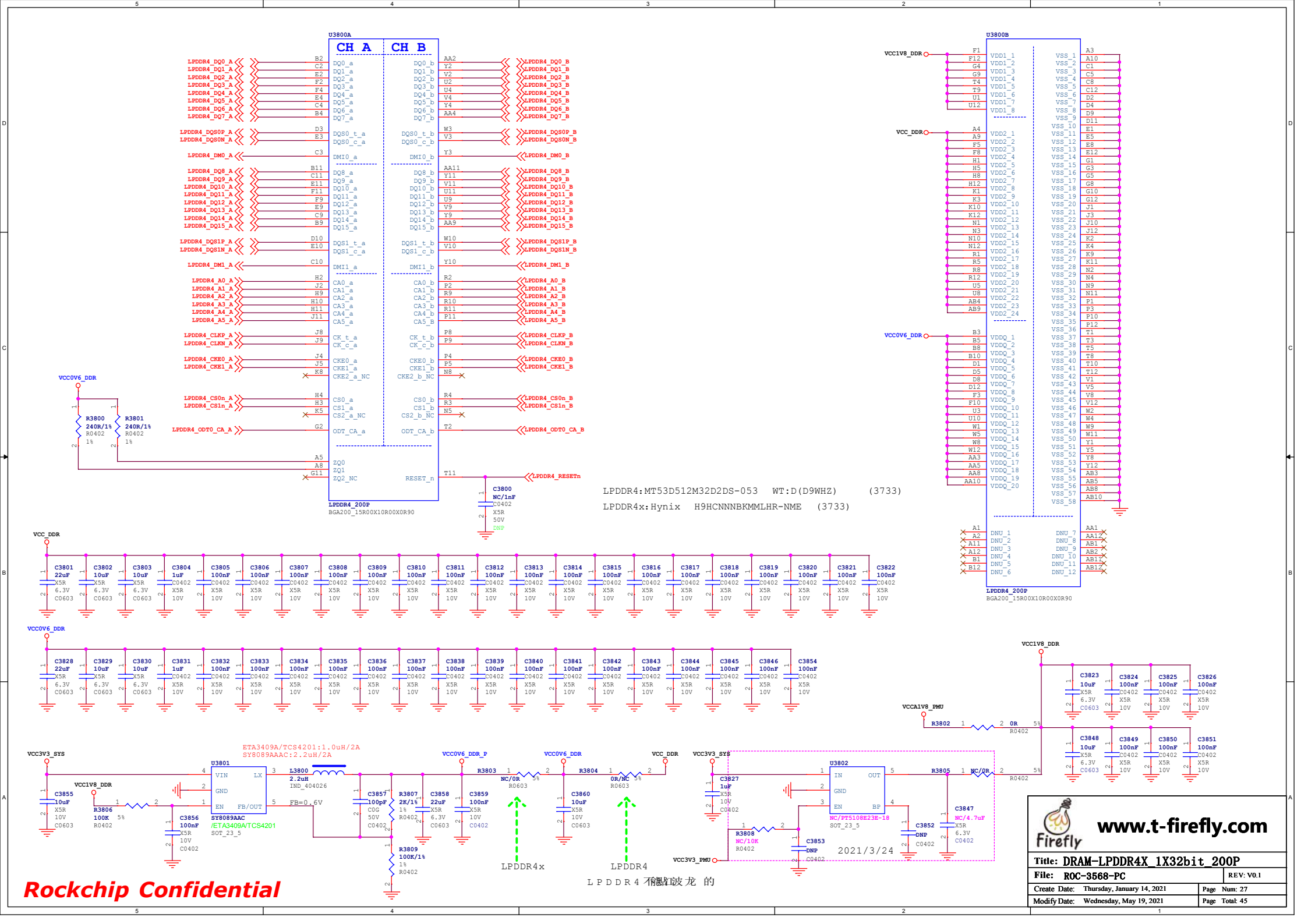
Title: KEY/LED/DEBUG		
File: ROC-3568-PC		REV: V0.1
Create Date: Wednesday, November 04, 2020	Page Num: 26	
Modify Date: Wednesday, May 19, 2021	Page Total: 45	


U3800A
CH A
CH B
LPDDR4_200P
BGA200_15R00X10R00X0R90
U3800B
LPDDR4_200P
BGA200_15R00X10R00X0R90
LPDDR4:MT53D512M32D2DS-053 WT:D(D9WHZ) (3733)
LPDDR4x:Hynix H9HCNNNBKMMLHR-NME (3733)
VCC_DDR
VCC0V6_DDR
VCC1V8_DDR
VCCA1V8_PMU
VCC3V3_SYS
VCC3V3_PMU
VCC0V6_DDR_P
ETA3409A/TCS4201:1.0uH/2A
SY8089AAAC:2.2uH/2A
SY8089AAC
/ETA3409/TCS4201
SOT_23_5
NC/PT5108E23E-18
2021/3/24
LPDDR4x
LPDDR4
LPDDR4 不贴时 的
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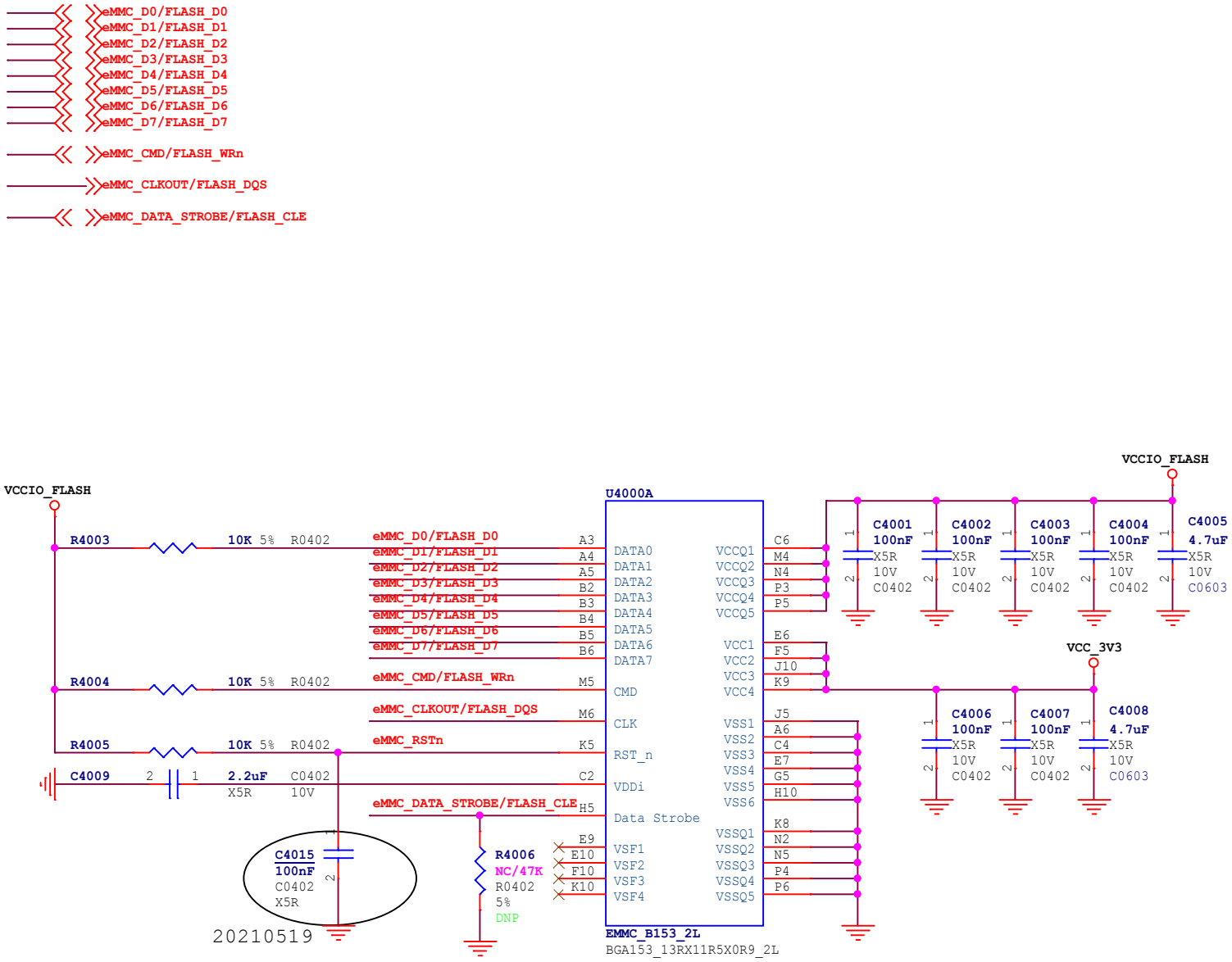
Title: DRAM-LPDDR4X_1X32bit_200P
File: ROC-3568-PC
REV: V0.1
Create Date: Thursday, January 14, 2021
Page Num: 27
Modify Date: Wednesday, May 19, 2021
Page Total: 45



KLMBG2JETD-B041

SDINBDA6-32G-XI1

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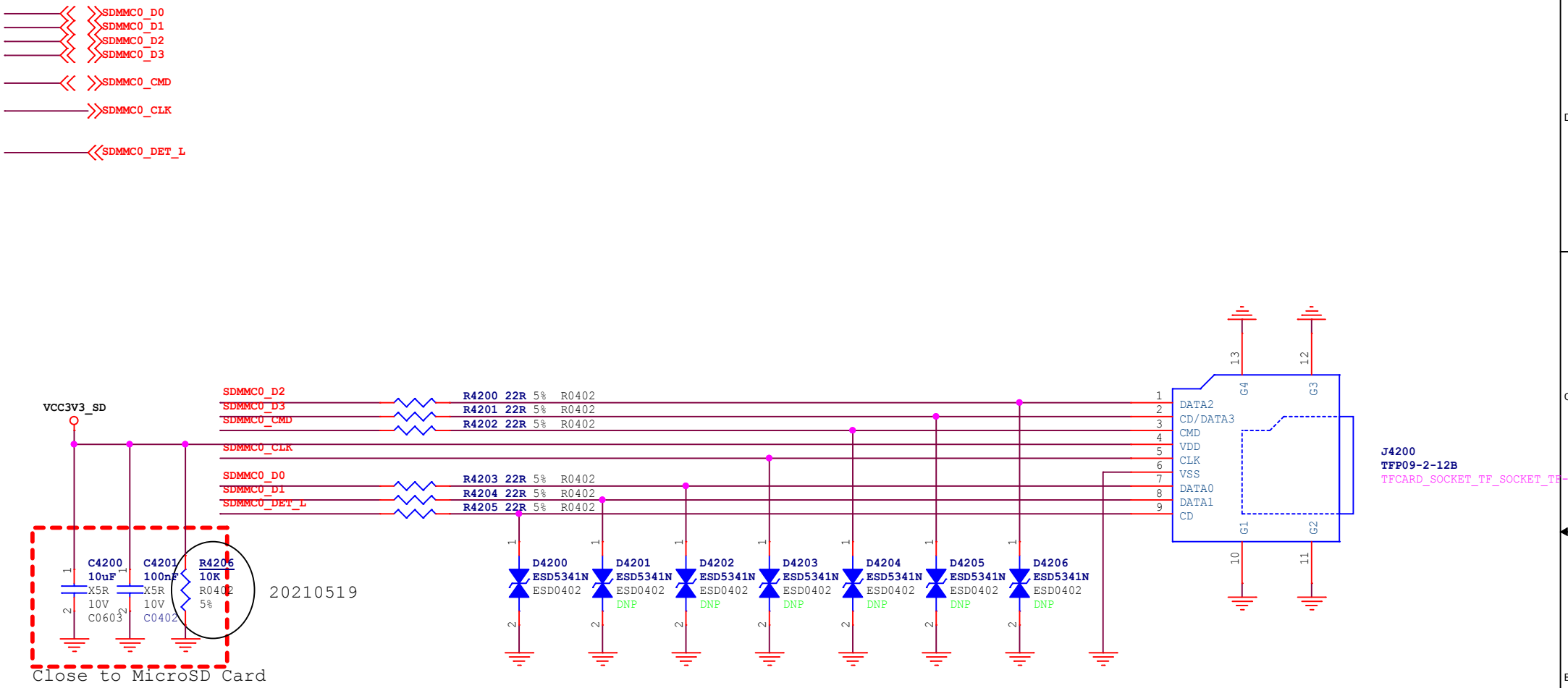
Title: Flash-eMMC Flash		
File: ROC-3568-PC		REV: V0.1
Create Date: Thursday, May 07, 2020		Page Num: 28
Modify Date: Wednesday, May 19, 2021		Page Total: 45



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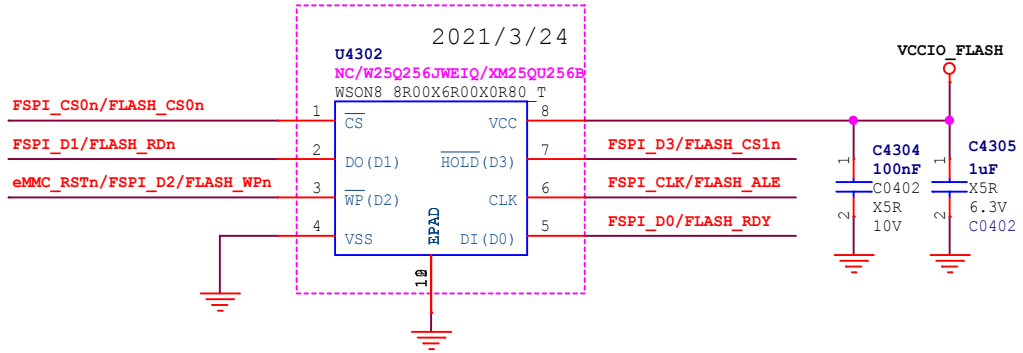
Title: Flash-MicroSD Card		
File: ROC-3568-PC		REV: V0.1
Create Date: Thursday, May 07, 2020	Page Num: 29	
Modify Date: Wednesday, May 19, 2021	Page Total: 45	

FSPI_CLK/FLASH_ALE

FSPI_D0/FLASH_RDY
FSPI_D1/FLASH_RDn
eMMC_RSTn/FSPI_D2/FLASH_WPn
FSPI_D3/FLASH_CS1n

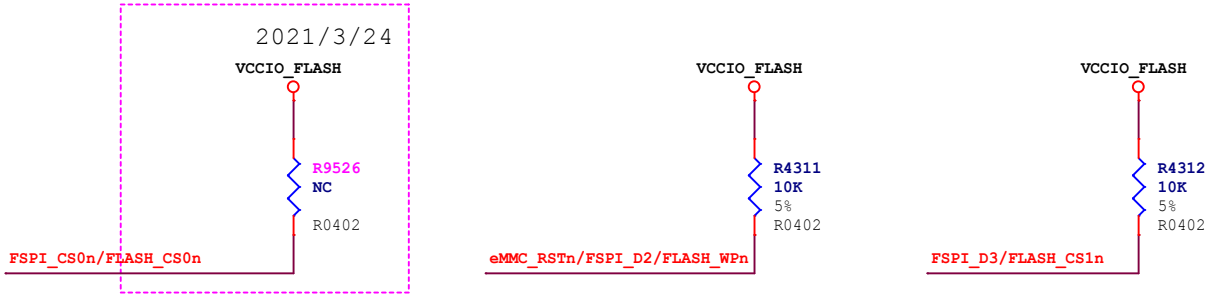
FSPI_CS0n/FLASH_CS0n



Default: 1.8V

SPI Nor: W25Q256JWEIQ 1.8V--DEFAULT

W25Q256FV,GD25Q256D 3.3V



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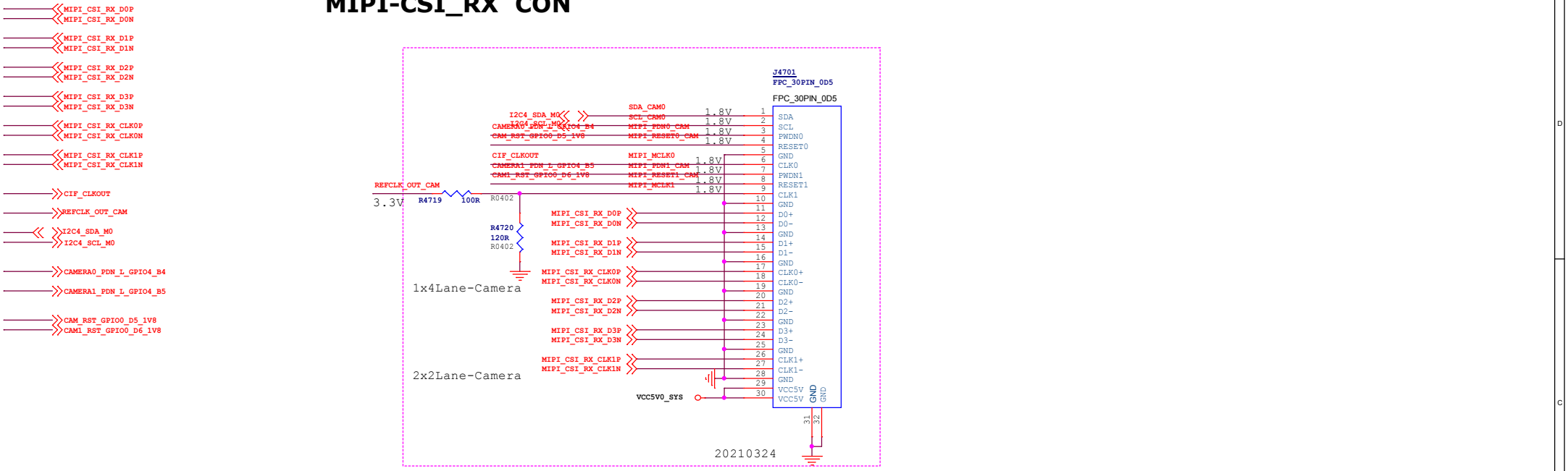
Title: Flash-SPI FLASH		
File: ROC-3568-PC		REV: V0.1
Create Date: Thursday, May 07, 2020		Page Num: 30
Modify Date: Wednesday, May 19, 2021		Page Total: 45

MIPI-CSI_RX CON



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Title: VI-Camera_MIPI-CSI	
File: ROC-3568-PC	REV: V0.1
Create Date: Thursday, May 07, 2020	Page Num: 31
Modify Date: Wednesday, May 19, 2021	Page Total: 45

HDMI_TX2P_PORT
HDMI_TX2N_PORT
HDMI_TX1P_PORT
HDMI_TX1N_PORT
HDMI_TX0P_PORT
HDMI_TX0N_PORT
HDMI_TXCLKP_PORT
HDMI_TXCLKN_PORT
HDMITX_SCL
HDMITX_SDA
HDMITX_CEC_M0
HDMI_TX_HPDIN

VCC5V0_SYS
C5001
1uF
C0402
X5R
10V

VCC5V_HDMI
C5000
1uF
X5R
10V
C0402

Cj<=0.4pF

HDMI TX DDC

VCC5V0_SYS
D5000
B5819WS
SOD_323
VCC_3V3
VCC5V_HDMI
R5000
10K
5%
R0402
Q5000
2SK3018
SOT_323
R5001
1.8K
5%
R0402
HDMITX_SCL
HDMI_TXDDC_SCL_PORT
VCC_3V3
R5002
10K
5%
R0402
Q5001
2SK3018
SOT_323
R5003
1.8K
5%
R0402
HDMITX_SDA
HDMI_TXDDC_SDA_PORT

U5000 ESD5304D
U5001 ESD5304D
U5002 ESD5304D
SON10_2R50X1R00X0R50
IO4 IO3 IO2 IO1 GND NC_6 NC_7 NC_9 NC_10

HDMI_TX2P_PORT
HDMI_TX2N_PORT
HDMI_TX1P_PORT
HDMI_TX1N_PORT
HDMI_TX0P_PORT
HDMI_TX0N_PORT
HDMI_TXCLKP_PORT
HDMI_TXCLKN_PORT
HDMI_TX_CEC_PORT
HDMI_TXDDC_SCL_PORT
HDMI_TXDDC_SDA_PORT
HDMI_TX_HPD_PORT

VCC5V_HDMI
ED5005
ESD5341N
ESD0402

J5000
HDMI_TYPE_A
hdmi_a_phd
Type A
D2P D2_G D2N D1P D1_G D1N D0P D0_G D0N CLKP CLK_G CLKN CEC Utility SCL SDA GND +5V HPD
G1 G2 G3 G4 20 21 22 23

HDMI TX CEC

VCC_3V3
VCC5V_HDMI
R5006
27K
5%
R0402
Q5002
2SK3018
SOT_323
HDMITX_CEC_M0
HDMI_TX_CEC_PORT

HDMI TX HPD

HDMI_TX_HPDIN
R5005
1K
5%
R0402
HDMI_TX_HPD_PORT
R5008
100K
5%
R0402

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Title: VO-HDMI2.0 TX		
File: ROC-3568-PC		REV: V0.1
Create Date: Thursday, May 07, 2020	Page Num: 32	
Modify Date: Wednesday, May 19, 2021	Page Total: 45	

MIPI_DSI_TX0_D0P/LVDS_TX0_D0P
MIPI_DSI_TX0_D0N/LVDS_TX0_D0N

MIPI_DSI_TX0_D1P/LVDS_TX0_D1P
MIPI_DSI_TX0_D1N/LVDS_TX0_D1N

MIPI_DSI_TX0_D2P/LVDS_TX0_D2P
MIPI_DSI_TX0_D2N/LVDS_TX0_D2N

MIPI_DSI_TX0_D3P/LVDS_TX0_D3P
MIPI_DSI_TX0_D3N/LVDS_TX0_D3N

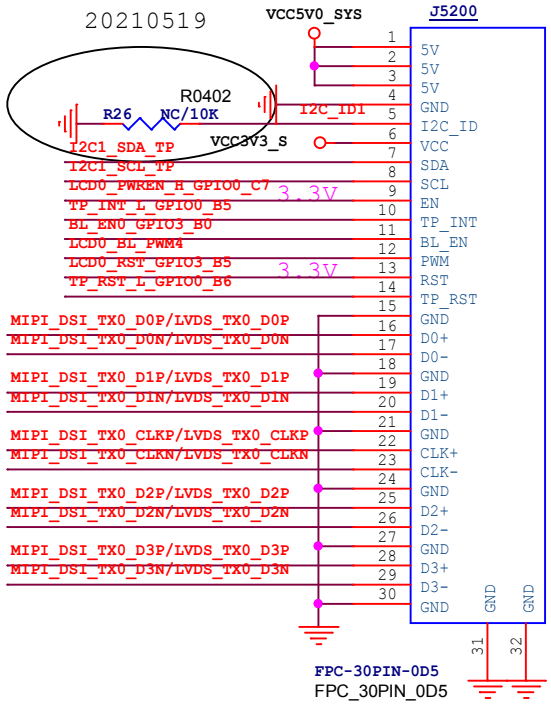
MIPI_DSI_TX0_CLKP/LVDS_TX0_CLKP
MIPI_DSI_TX0_CLKN/LVDS_TX0_CLKN

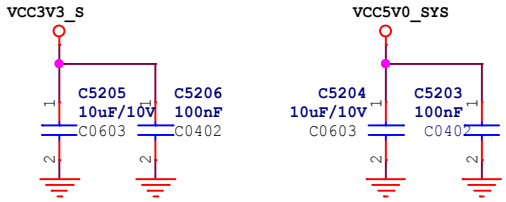
I2C1_SCL_TP
I2C1_SDA_TP
TP_INT_L_GPIO0_B5
TP_RST_L_GPIO0_B6

LCD0_BL_PWM4
LCD0_PWREN_H_GPIO0_C7

BL_EN0_GPIO3_B0
LCD0_RST_GPIO3_B5

SARADC_VIN2_LCD_ID
SARADC_VIN2_LCD_ID R5202 0R R0402 I2C_ID1





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Title: VO-LCM_MIPI-DSI_TX0/LVDS_TX0		
File: ROC-3568-PC		REV: V0.1
Create Date: Tuesday, May 19, 2020	Page Num: 33	
Modify Date: Wednesday, May 19, 2021	Page Total: 45	

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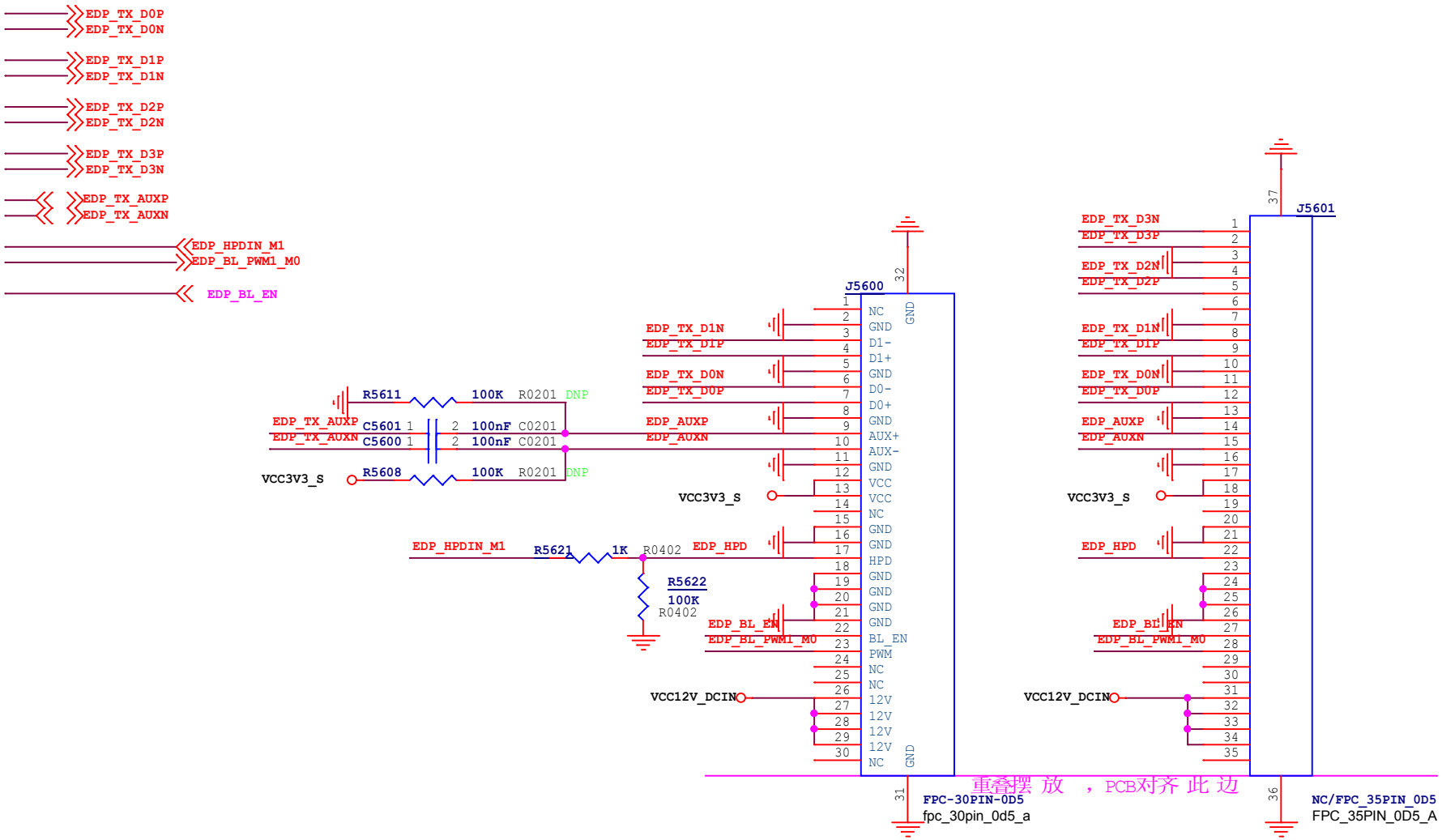
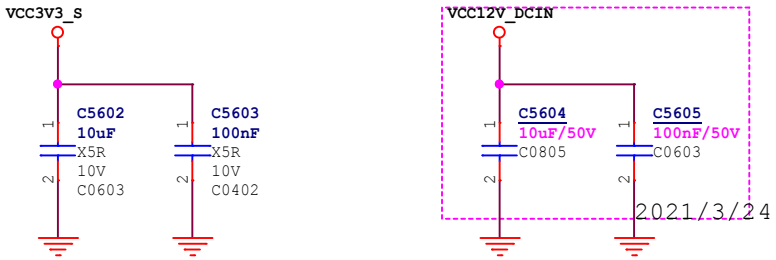
Title: VO-LCM_MIPI-DSI_TX1		
File: ROC-3568-PC		REV: V0.1
Create Date: Tuesday, May 19, 2020	Page Num: 34	
Modify Date: Wednesday, May 19, 2021	Page Total: 45	



Default no place,Support 4K eDP Panel



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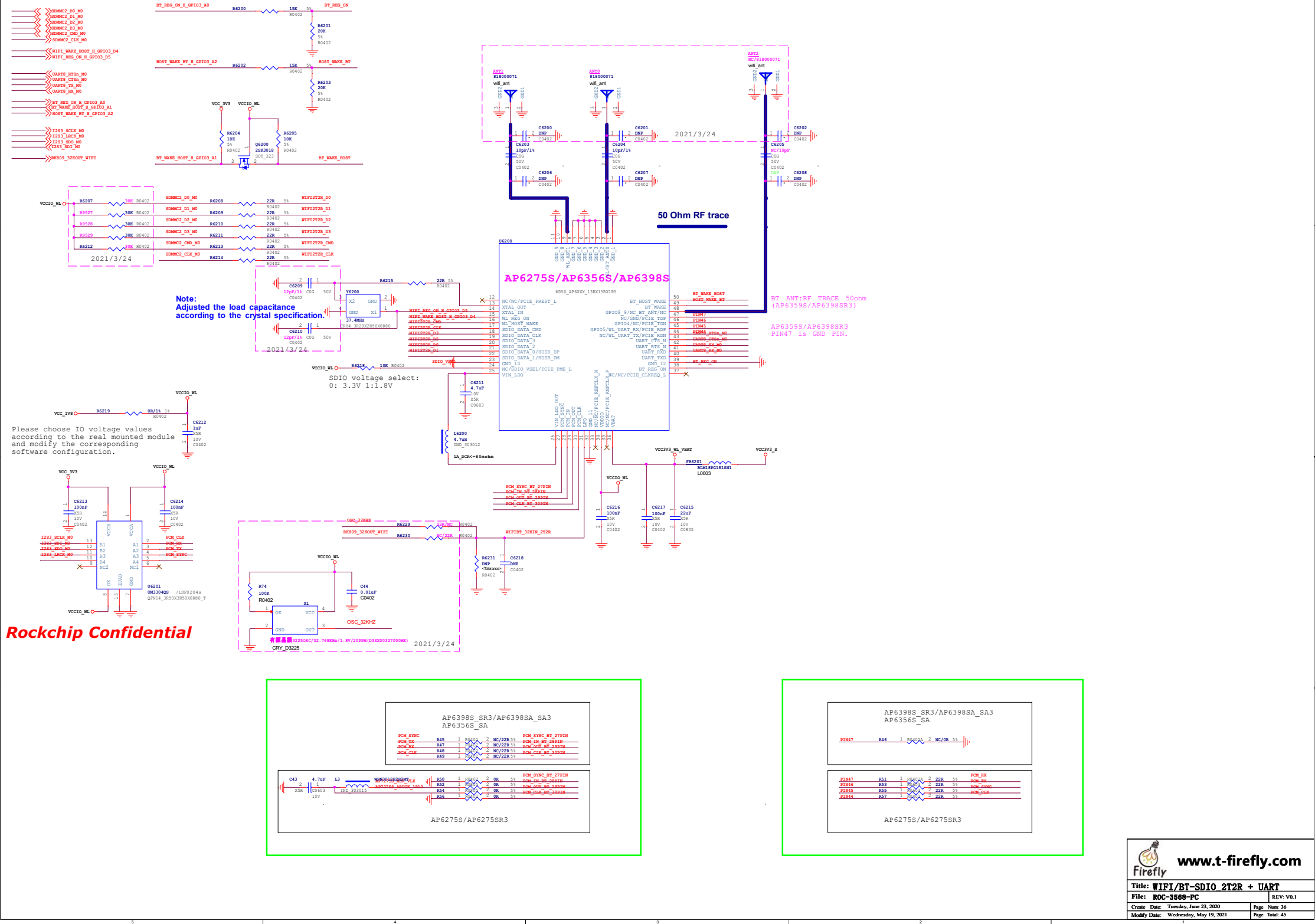
Title: VO-LCM_eDP		
File: ROC-3568-PC		REV: V0.1
Create Date: Saturday, July 18, 2020	Page Num: 35	
Modify Date: Wednesday, May 19, 2021	Page Total: 45	


AP6275S/AP6356S/AP6398S
50 Ohm RF trace
BT ANT:RF TRACE 50ohm
(AP6359S/AP6398SR3)
AP6359S/AP6398SR3
PIN47 is GND PIN.
Note:
Adjusted the load capacitance
according to the crystal specification.
SDIO voltage select:
0: 3.3V 1:1.8V
Please choose IO voltage values
according to the real mounted module
and modify the corresponding
software configuration.
2021/3/24
AP6398S_SR3/AP6398SA_SA3
AP6356S_SA
AP6275S/AP6275SR3
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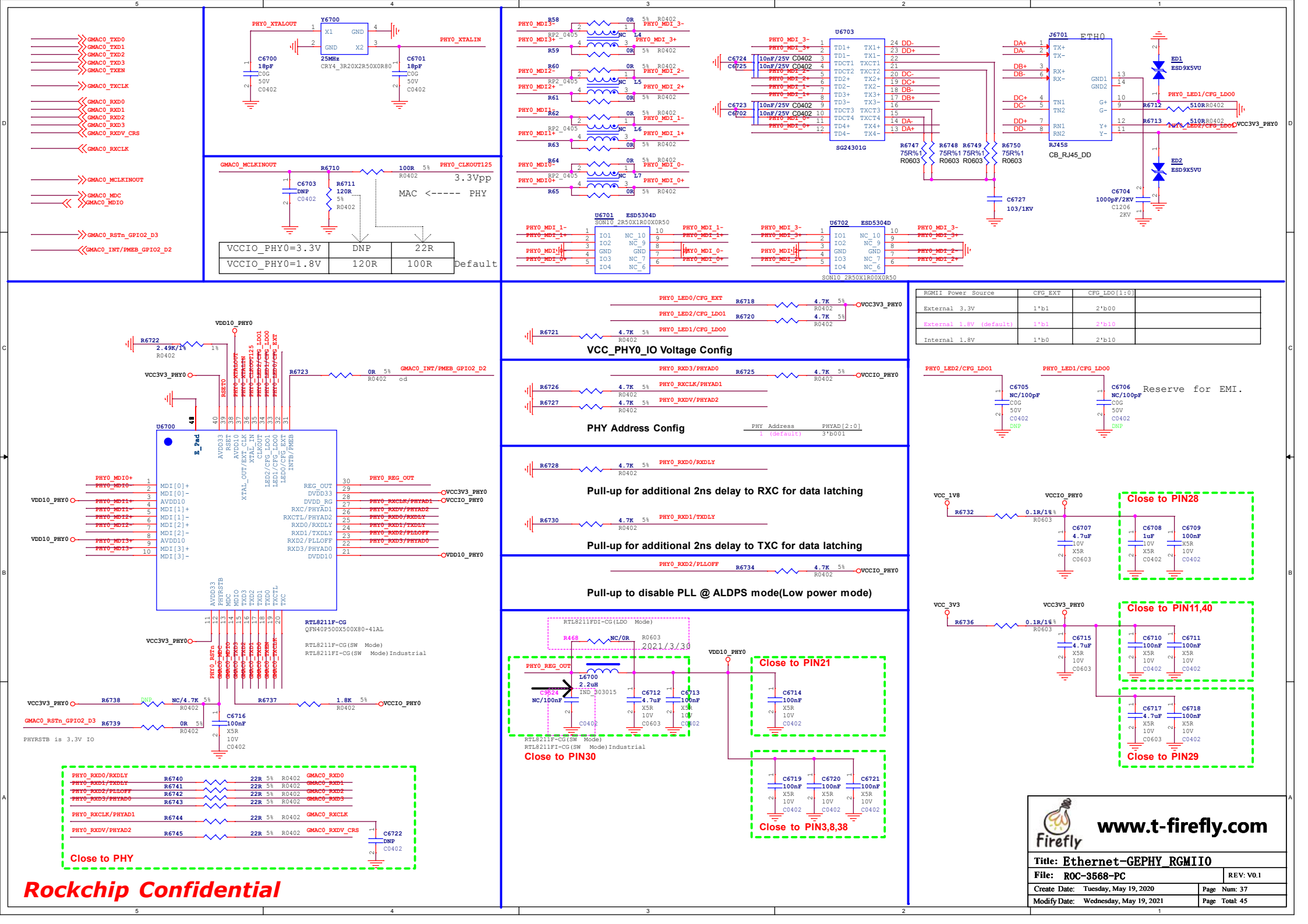
Title: WIFI/BT-SDIO 2T2R + UART
File: ROC-3568-PC
REV: V0.1
Create Date: Tuesday, June 23, 2020
Modify Date: Wednesday, May 19, 2021
Num: 36
Total: 45


GMAC0_TXD0
GMAC0_TXD1
GMAC0_TXD2
GMAC0_TXD3
GMAC0_TXEN
GMAC0_TXCLK
GMAC0_RXD0
GMAC0_RXD1
GMAC0_RXD2
GMAC0_RXD3
GMAC0_RXDV_CRS
GMAC0_RXCLK
GMAC0_MCLKINOUT
GMAC0_MDC
GMAC0_MDIO
GMAC0_RSTn_GPIO2_D3
GMAC0_INT/PMEB_GPIO2_D2
PHY0_XTALOUT
Y6700
X1
GND
X2
25MHz
CRY4_3R20X2R50X0R80
PHY0_XTALIN
C6700
18pF
C0G
50V
C0402
C6701
18pF
C0G
50V
C0402
GMAC0_MCLKINOUT
R6710
100R 5%
R0402
PHY0_CLKOUT125
3.3Vpp
MAC <----- PHY
C6703
DNP
C0402
R6711
120R
5%
R0402
VCCIO_PHY0=3.3V
DNP
22R
VCCIO_PHY0=1.8V
120R
100R
Default
PHY0_MDI3-
PHY0_MDI3+
PHY0_MDI2-
PHY0_MDI2+
PHY0_MDI1-
PHY0_MDI1+
PHY0_MDI0-
PHY0_MDI0+
R58
R59
R60
R61
R62
R63
R64
R65
0R 5% R0402
RP2_0405
NC
L4
L5
L6
L7
U6703
SG24301G
TD1+
TD1-
TD2+
TD2-
TD3+
TD3-
TD4+
TD4-
TX1+
TX1-
TX2+
TX2-
TX3+
TX3-
TX4+
TX4-
C6724
C6725
C6723
C6702
10nF/25V C0402
R6747
R6748
R6749
R6750
75R%1
R0603
C6727
103/1KV
J6701
ETH0
RJ45S
CB_RJ45_DD
DA+
DA-
DB+
DB-
DC+
DC-
DD+
DD-
ED1
ESD9X5VU
ED2
ESD9X5VU
PHY0_LED1/CFG_LDO0
PHY0_LED2/CFG_LDO1
R6712
R6713
510R R0402
C6704
1000pF/2KV
C1206
2KV
VCC3V3_PHY0
U6701
ESD5304D
SON10_2R50X1R00X0R50
U6702
ESD5304D
SON10_2R50X1R00X0R50
IO1
IO2
GND
IO3
IO4
NC_10
NC_9
NC_7
NC_6
VDD10_PHY0
R6722
2.49K/1%
R0402
VCC3V3_PHY0
R6723
0R 5%
R0402
od
GMAC0_INT/PMEB_GPIO2_D2
U6700
E_Pad
49
RSET0
PHY0_XTALOUT
PHY0_XTALIN
PHY0_CLKOUT125
PHY0_LED2/CFG_LDO1
PHY0_LED1/CFG_LDO0
PHY0_LED0/CFG_EXT
AVDD33
RSET
AVDD10
XTAL_OUT/EXT_CLK
XTAL_IN
CLKOUT
LED2/CFG_LDO1
LED1/CFG_LDO0
LED0/CFG_EXT
INTB/PMEB
MDI[0]+
MDI[0]-
AVDD10
MDI[1]+
MDI[1]-
MDI[2]+
MDI[2]-
AVDD10
MDI[3]+
MDI[3]-
REG_OUT
DVDD33
DVDD_RG
RXC/PHYAD1
RXCTL/PHYAD2
RXD0/RXDLY
RXD1/TXDLY
RXD2/PLLOFF
RXD3/PHYAD0
DVDD10
PHY0_REG_OUT
VCC3V3_PHY0
VCCIO_PHY0
VDD10_PHY0
AVDD33
PHYRSTB
MDC
MDIO
TXD3
TXD2
TXD1
TXD0
TXCTL
TXC
RTL8211F-CG
QFN40P500X500X80-41AL
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
PHY0_RSTn
GMAC0_MDC
GMAC0_MDIO
GMAC0_TXD3
GMAC0_TXD2
GMAC0_TXD1
GMAC0_TXD0
GMAC0_TXEN
GMAC0_TXCLK
R6738
DNP
NC/4.7K 5%
R0402
R6737
1.8K 5%
R0402
VCCIO_PHY0
GMAC0_RSTn_GPIO2_D3
R6739
0R 5%
R0402
C6716
100nF
X5R
10V
C0402
PHYRSTB is 3.3V IO
PHY0_RXD0/RXDLY
PHY0_RXD1/TXDLY
PHY0_RXD2/PLLOFF
PHY0_RXD3/PHYAD0
PHY0_RXCLK/PHYAD1
PHY0_RXDV/PHYAD2
R6740
R6741
R6742
R6743
R6744
R6745
22R 5% R0402
GMAC0_RXD0
GMAC0_RXD1
GMAC0_RXD2
GMAC0_RXD3
GMAC0_RXCLK
GMAC0_RXDV_CRS
C6722
DNP
C0402
Close to PHY
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PHY0_LED0/CFG_EXT
PHY0_LED2/CFG_LDO1
PHY0_LED1/CFG_LDO0
R6718
R6720
R6721
4.7K 5%
R0402
VCC3V3_PHY0
VCC_PHY0_IO Voltage Config
PHY0_RXD3/PHYAD0
PHY0_RXCLK/PHYAD1
PHY0_RXDV/PHYAD2
R6725
R6726
R6727
VCCIO_PHY0
PHY Address Configuration
PHY Address
PHYAD[2:0]
1 (default)
3'b001
PHY0_RXD0/RXDLY
R6728
Pull-up for additional 2ns delay to RXC for data latching
PHY0_RXD1/TXDLY
R6730
Pull-up for additional 2ns delay to TXC for data latching
PHY0_RXD2/PLLOFF
R6734
Pull-up to disable PLL @ ALDPS mode(Low power mode)
RTL8211FDI-CG(LDO Mode)
R468
NC/0R
R0603
2021/3/30
PHY0_REG_OUT
L6700
2.2uH
IND_B03015
C5624
NC/100nF
C6712
4.7uF
X5R
10V
C0603
C6713
100nF
X5R
10V
C0402
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
Close to PIN30
VDD10_PHY0
Close to PIN21
C6714
100nF
X5R
10V
C0402
C6719
100nF
C6720
100nF
C6721
100nF
Close to PIN3,8,38
RGMII Power Source
CFG_EXT
CFG_LDO[1:0]
External 3.3V
1'b1
2'b00
External 1.8V (default)
1'b1
2'b10
Internal 1.8V
1'b0
2'b10
PHY0_LED2/CFG_LDO1
C6705
NC/100pF
C0G
50V
C0402
DNP
PHY0_LED1/CFG_LDO0
C6706
NC/100pF
C0G
50V
C0402
DNP
Reserve for EMI.
VCC_1V8
R6732
0.1R/1%
R0603
VCCIO_PHY0
C6707
4.7uF
10V
X5R
C0603
C6708
1uF
10V
X5R
C0402
C6709
100nF
X5R
10V
C0402
Close to PIN28
VCC_3V3
R6736
0.1R/1%
R0603
VCC3V3_PHY0
C6715
4.7uF
X5R
10V
C0603
C6710
100nF
C6711
100nF
Close to PIN11,40
C6717
4.7uF
C6718
100nF
Close to PIN29
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Firefly
Title: Ethernet-GEPHY_RGMII0
File: ROC-3568-PC
REV: V0.1
Create Date: Tuesday, May 19, 2020
Page Num: 37
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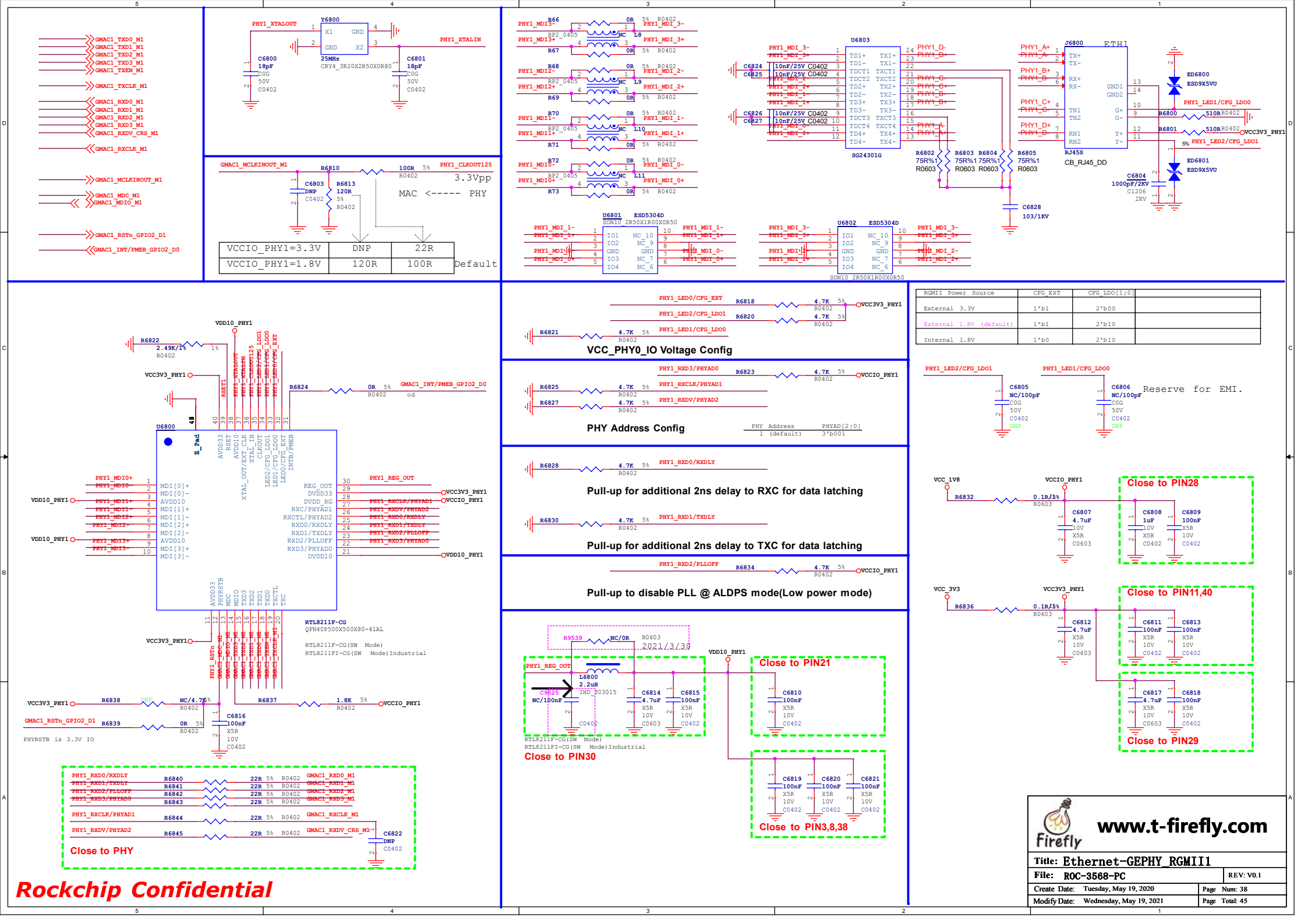
Page Total: 45


GMAC1_TXD0_M1
GMAC1_TXD1_M1
GMAC1_TXD2_M1
GMAC1_TXD3_M1
GMAC1_TXEN_M1
GMAC1_TXCLK_M1
GMAC1_RXD0_M1
GMAC1_RXD1_M1
GMAC1_RXD2_M1
GMAC1_RXD3_M1
GMAC1_RXDV_CRS_M1
GMAC1_RXCLK_M1
GMAC1_MCLKINOUT_M1
GMAC1_MDC_M1
GMAC1_MDIO_M1
GMAC1_RSTn_GPIO2_D1
GMAC1_INT/PMEB_GPIO2_D0
PHY1_XTALOUT
Y6800
25MHz
CRY4_3R20X2R50X0R80
PHY1_XTALIN
C6800 18pF C0G 50V C0402
C6801 18pF C0G 50V C0402
GMAC1_MCLKINOUT_M1
R6810 100R 5% R0402
PHY1_CLKOUT125
3.3Vpp
C6803 DNP C0402
R6813 120R 5% R0402
MAC <----- PHY
VCCIO_PHY1=3.3V DNP 22R
VCCIO_PHY1=1.8V 120R 100R Default
PHY1_MDI3+ PHY1_MDI3-
PHY1_MDI2+ PHY1_MDI2-
PHY1_MDI1+ PHY1_MDI1-
PHY1_MDI0+ PHY1_MDI0-
R66 R67 R68 R69 R70 R71 R72 R73 0R 5% R0402
RP2_0405
L8 L9 L10 L11
U6803
SG24301G
C6824 C6825 C6826 C6827 10nF/25V C0402
R6802 75R%1 R0603
R6803 R6804 75R%1 R0603
R6805 75R%1 R0603
C6828 103/1KV
J6800 ETH1
RJ45S
CB_RJ45_DD
ED6800 ESD9X5VU
ED6801 ESD9X5VU
PHY1_LED1/CFG_LDO0
PHY1_LED2/CFG_LDO1
R6800 510R R0402
R6801 510R R0402
VCC3V3_PHY1
C6804 1000pF/2KV C1206 2KV
U6801 ESD5304D SON10_2R50X1R00X0R50
U6802 ESD5304D SON10_2R50X1R00X0R50
VDD10_PHY1
R6822 2.49K/1% R0402
VCC3V3_PHY1
R6824 0R 5% R0402 od
GMAC1_INT/PMEB_GPIO2_D0
U6800
E_Pad
MDI[0]+ MDI[0]- MDI[1]+ MDI[1]- MDI[2]+ MDI[2]- MDI[3]+ MDI[3]-
AVDD10
REG_OUT DVDD33 DVDD_RG RXC/PHYAD1 RXCTL/PHYAD2 RXD0/RXDLY RXD1/TXDLY RXD2/PLLOFF RXD3/PHYAD0 DVDD10
PHY1_REG_OUT
VCC3V3_PHY1
VCCIO_PHY1
VDD10_PHY1
RTL8211F-CG
QFN40P500X500X80-41AL
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
R6838 DNP NC/4.7K 5% R0402
R6837 1.8K 5% R0402
R6839 0R 5% R0402
GMAC1_RSTn_GPIO2_D1
C6816 100nF X5R 10V C0402
PHYRSTB is 3.3V IO
R6840 R6841 R6842 R6843 R6844 R6845 22R 5% R0402
PHY1_RXD0/RXDLY
PHY1_RXD1/TXDLY
PHY1_RXD2/PLLOFF
PHY1_RXD3/PHYAD0
PHY1_RXCLK/PHYAD1
PHY1_RXDV/PHYAD2
GMAC1_RXD0_M1
GMAC1_RXD1_M1
GMAC1_RXD2_M1
GMAC1_RXD3_M1
GMAC1_RXCLK_M1
GMAC1_RXDV_CRS_M1
C6822 DNP C0402
Close to PHY
Rockchip Confidential
PHY1_LED0/CFG_EXT
PHY1_LED2/CFG_LDO1
PHY1_LED1/CFG_LDO0
R6818 R6820 R6821 4.7K 5% R0402
VCC_PHY0_IO Voltage Config
PHY1_RXD3/PHYAD0
PHY1_RXCLK/PHYAD1
PHY1_RXDV/PHYAD2
R6823 R6825 R6827 4.7K 5% R0402
VCCIO_PHY1
PHY Address Configuration
PHY Address PHYAD[2:0]
1 (default) 3'b001
R6828 4.7K 5% R0402
PHY1_RXD0/RXDLY
Pull-up for additional 2ns delay to RXC for data latching
R6830 4.7K 5% R0402
PHY1_RXD1/TXDLY
Pull-up for additional 2ns delay to TXC for data latching
PHY1_RXD2/PLLOFF
R6834 4.7K 5% R0402
VCCIO_PHY1
Pull-up to disable PLL @ ALDPS mode(Low power mode)
R9539 NC/0R R0603
2021/3/30
VDD10_PHY1
PHY1_REG_OUT
L6800 2.2uH IND_B03015
C6825 NC/100nF
C6814 4.7uF X5R 10V C0603
C6815 100nF X5R 10V C0402
C6810 100nF X5R 10V C0402
Close to PIN21
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
Close to PIN30
C6819 C6820 C6821 100nF X5R 10V C0402
Close to PIN3,8,38
RGMII Power Source | CFG_EXT | CFG_LDO[1:0]
External 3.3V | 1'b1 | 2'b00
External 1.8V (default) | 1'b1 | 2'b10
Internal 1.8V | 1'b0 | 2'b10
PHY1_LED2/CFG_LDO1
PHY1_LED1/CFG_LDO0
C6805 NC/100pF C0G 50V C0402 DNP
C6806 NC/100pF C0G 50V C0402 DNP
Reserve for EMI.
VCC_1V8
VCCIO_PHY1
R6832 0.1R/1% R0603
C6807 4.7uF 10V X5R C0603
C6808 1uF 10V X5R C0402
C6809 100nF X5R 10V C0402
Close to PIN28
VCC_3V3
VCC3V3_PHY1
R6836 0.1R/1% R0603
C6812 4.7uF 10V X5R C0603
C6811 100nF X5R 10V C0402
C6813 100nF X5R 10V C0402
Close to PIN11,40
C6817 4.7uF X5R 10V C0603
C6818 100nF X5R 10V C0402
Close to PIN29
Firefly
www.t-firefly.com
Title: Ethernet-GEPHY_RGMII1
File: ROC-3568-PC
REV: V0.1
Create Date: Tuesday, May 19, 2020
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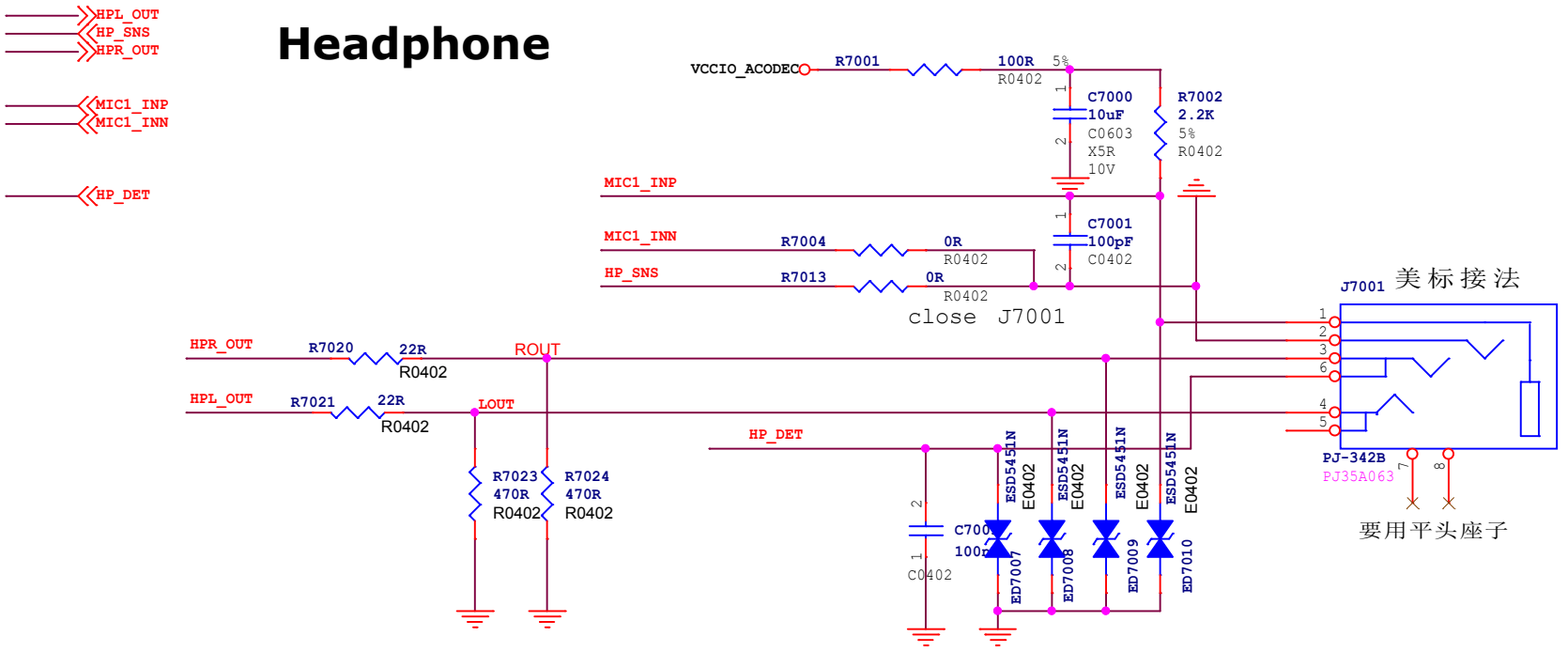
Headphone



www.t-firefly.com

Title: Audio Port		
File: ROC-3568-PC		REV: V0.1
Create Date: Tuesday, May 19, 2020		Page Num: 39
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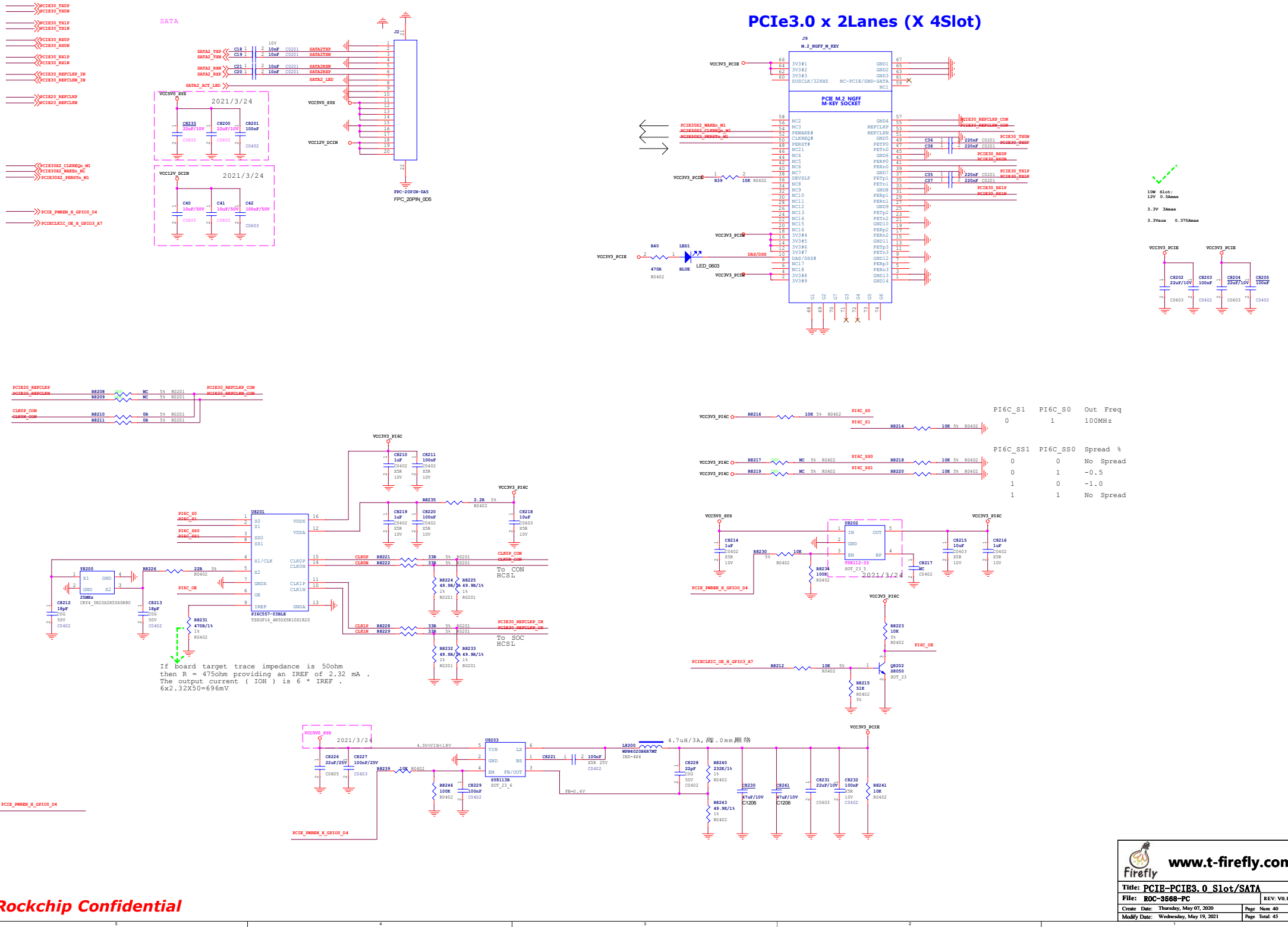
PCIe3.0 x 2Lanes (X 4Slot)



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Title:	PCIE-PCIE3.0 Slot/SATA
File:	ROC-3568-PC
REV:	V0.1
Create Date:	Thursday, May 07, 2020
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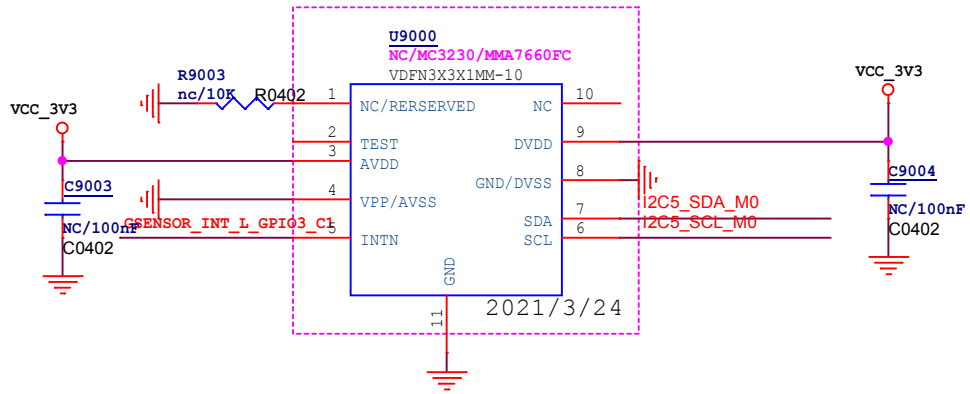
I2C5_SCL_M0
I2C5_SDA_M0
GSENSOR_INT_L_GPIO3_C1

Gyroscope+G-sensor



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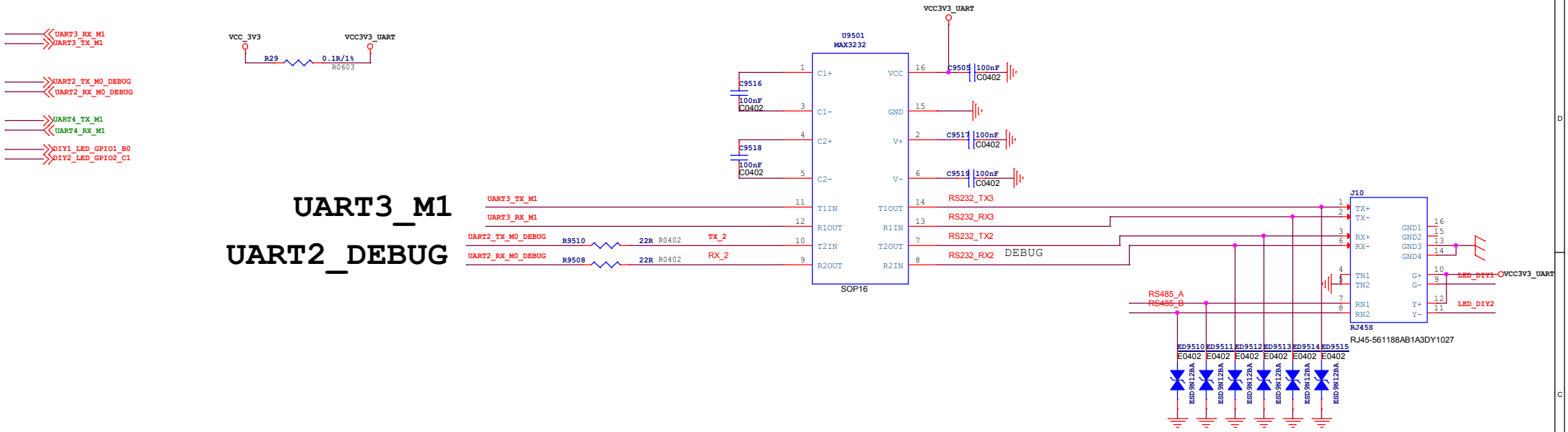
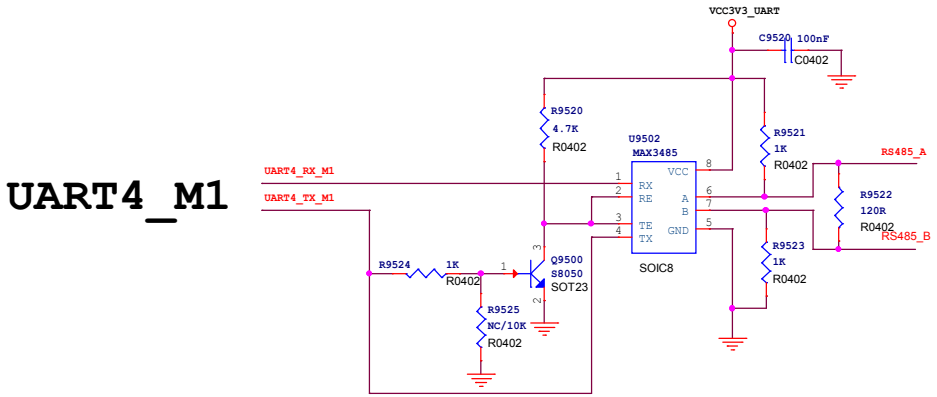
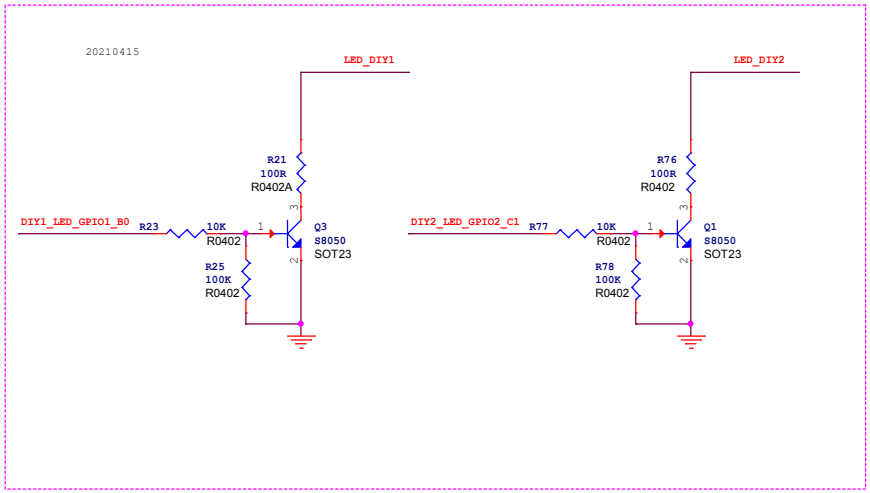
Title: Sensor		
File: ROC-3568-PC		REV: V0.1
Create Date: Tuesday, May 19, 2020		Page Num: 41
Modify Date: Wednesday, May 19, 2021		Page Total: 45



RS485





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Title: RS232/RS485		
File: ROC-3568-PC		REV: V0.1
Create Date: Friday, July 10, 2020	Page	Num: 42
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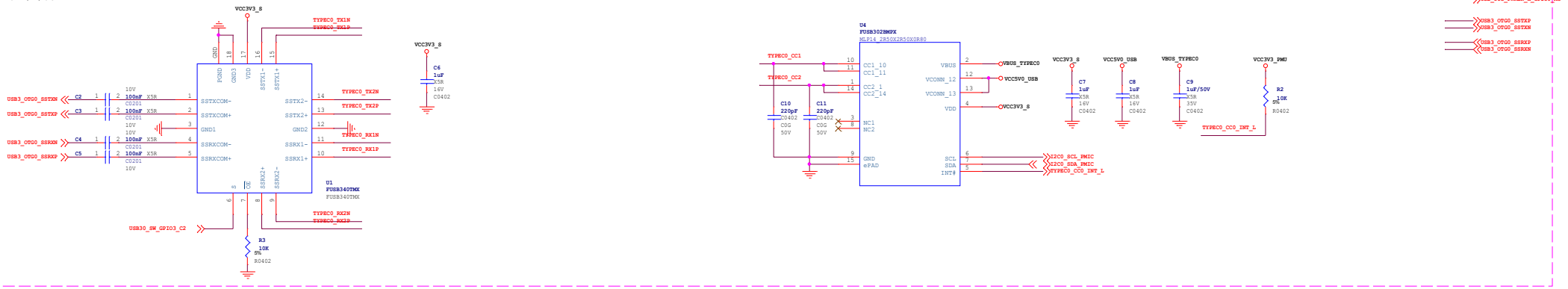
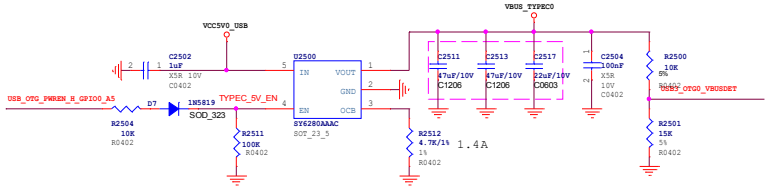
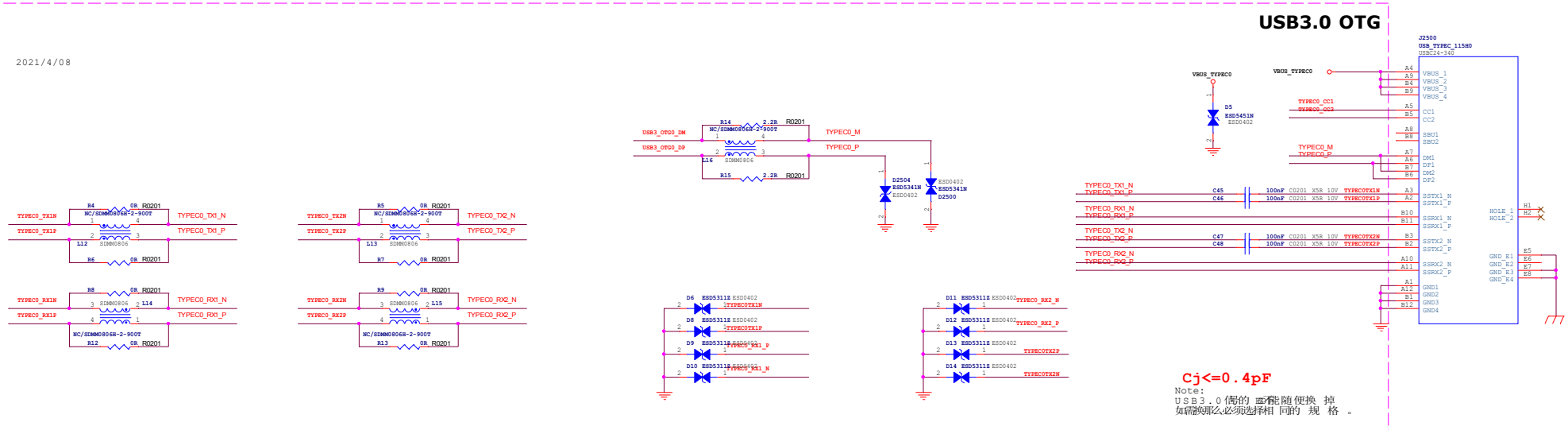
2021/4/08


VCC3V3_S
TYPEC0_TX1N
TYPEC0_TX1P
TYPEC0_TX2N
TYPEC0_TX2P
TYPEC0_RX1N
TYPEC0_RX1P
TYPEC0_RX2N
TYPEC0_RX2P
USB3_OTG0_SSTXN
USB3_OTG0_SSTXP
USB3_OTG0_SSRXN
USB3_OTG0_SSRXP
USB30_SW_GPIO3_C2
U1
FUSB340TMX
U4
FUSB302BMPX
TYPEC0_CC1
TYPEC0_CC2
VBUS_TYPEC0
VCC5V0_USB
I2C0_SCL_PMIC
I2C0_SDA_PMIC
TYPEC0_CC0_INT_L
VCC3V3_PMU
USB3_OTG0_DP
USB3_OTG0_DM
USB3_OTG0_VBUSDET
USB_OTG_PWREN_H_GPIO0_A5


VCC5V0_USB
VBUS_TYPEC0
U2500
SY6280AAAC
TYPEC_5V_EN
USB_OTG_PWREN_H_GPIO0_A5
USB3_OTG0_VBUSDET
1.4A


2021/4/08
USB3.0 OTG
J2500
USB_TYPEC_115H0
TYPEC0_TX1_N
TYPEC0_TX1_P
TYPEC0_RX1_N
TYPEC0_RX1_P
TYPEC0_TX2_N
TYPEC0_TX2_P
TYPEC0_RX2_N
TYPEC0_RX2_P
Cj<=0.4pF
Note:
USB3.0信号的共模随便换 掉
如需换那么必须选择相 同的 规 格 。

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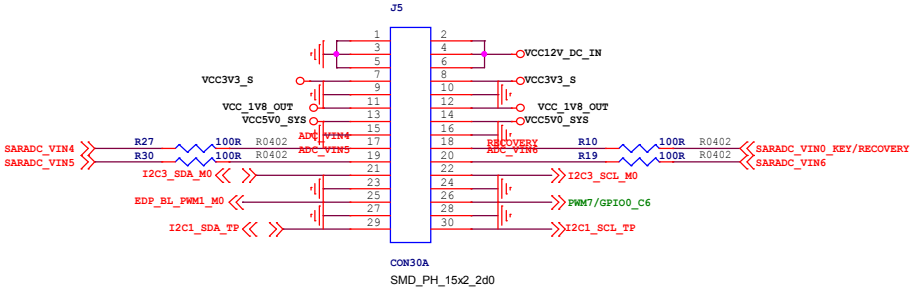
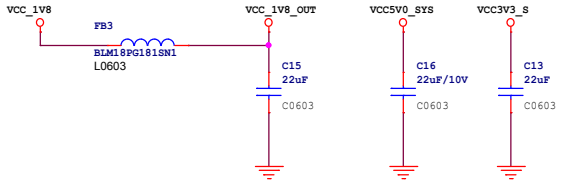
Title: TYPE-C
File: ROC-3568-PC
REV: V0.1
Create Date: Thursday, April 08, 2021
Modify Date: Wednesday, May 19, 2021
Page Num: 43
Page Total: 45

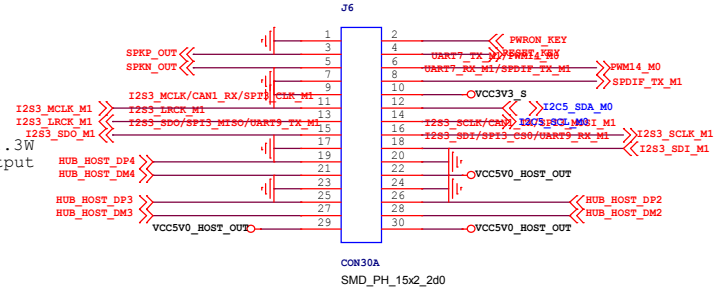


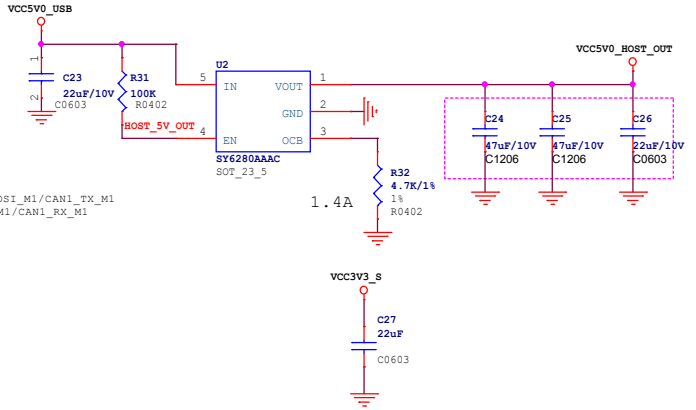


3.3V
3.3V

SPK

Note:8ohm/1.3W
Speaker Output





CAN1_M1

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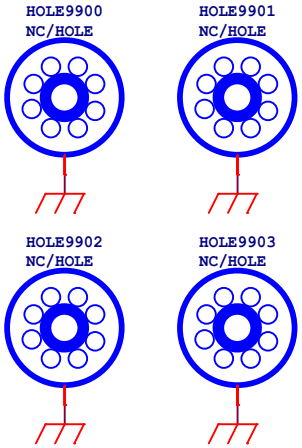
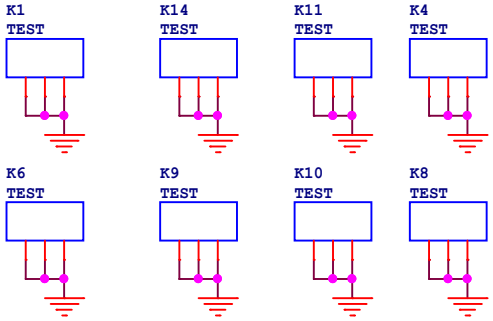
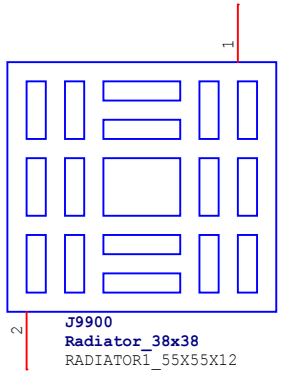
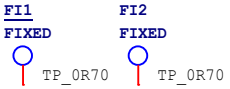
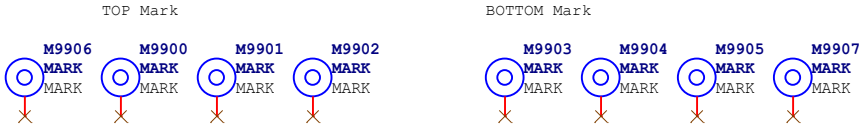
Title: Extension Interface		
File: ROC-3399-PC+		REV: V0.1
Create Date: Thursday, November 05, 2020	Page:	Num: 44
Modify Date: Wednesday, May 19, 2021	Page:	Total: 45











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File: ROC-3568-PC		REV: V0.1
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