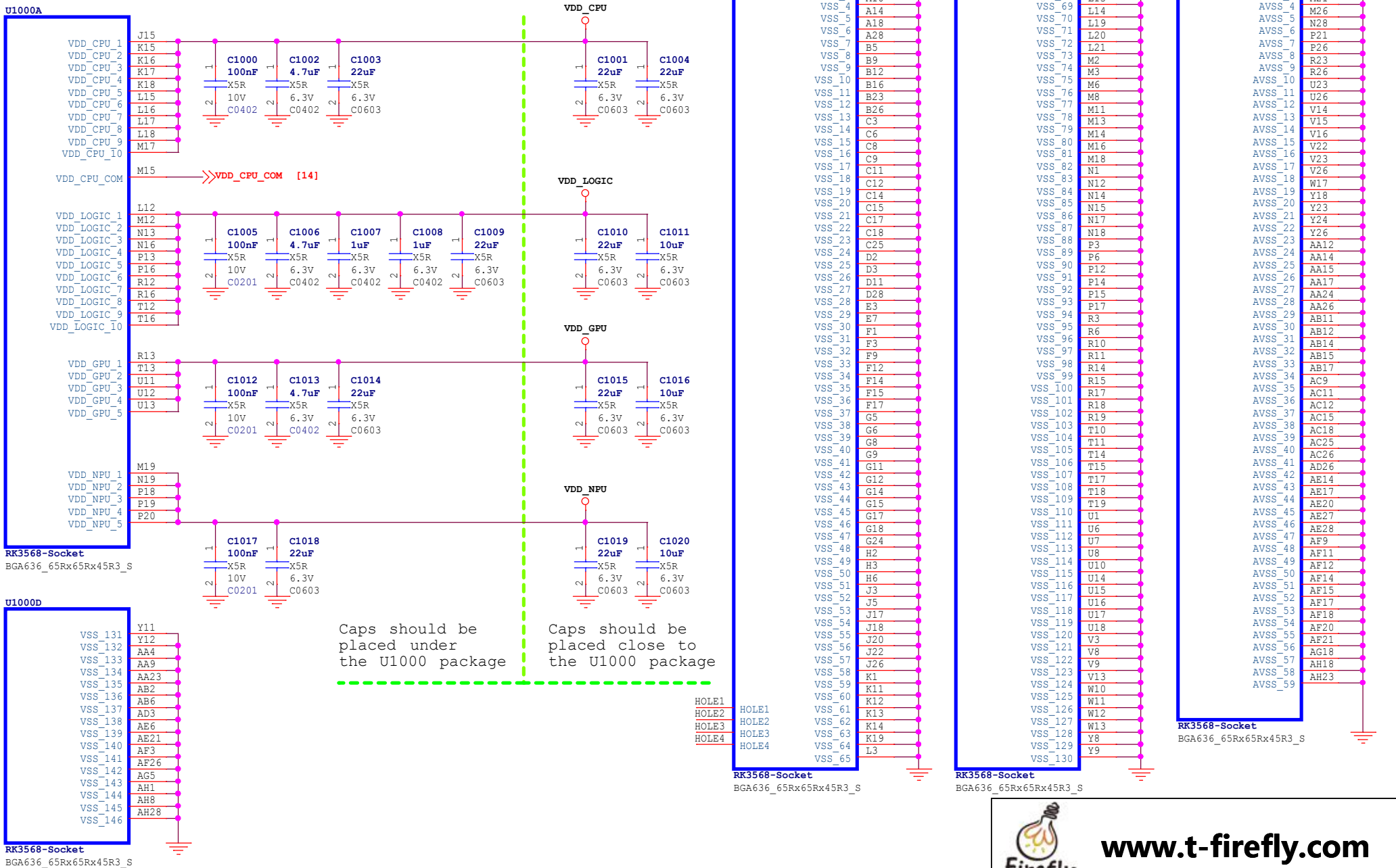




# RK3568\_ABCDE (Power&Gnd)



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Title: RK3568 Power/GND		REV: V1.1
File: ROC-3568-PC		
Create Date: Monday, March 30, 2020	Page Num: 2	
Modify Date: Tuesday, August 09, 2022	Page Total: 36	

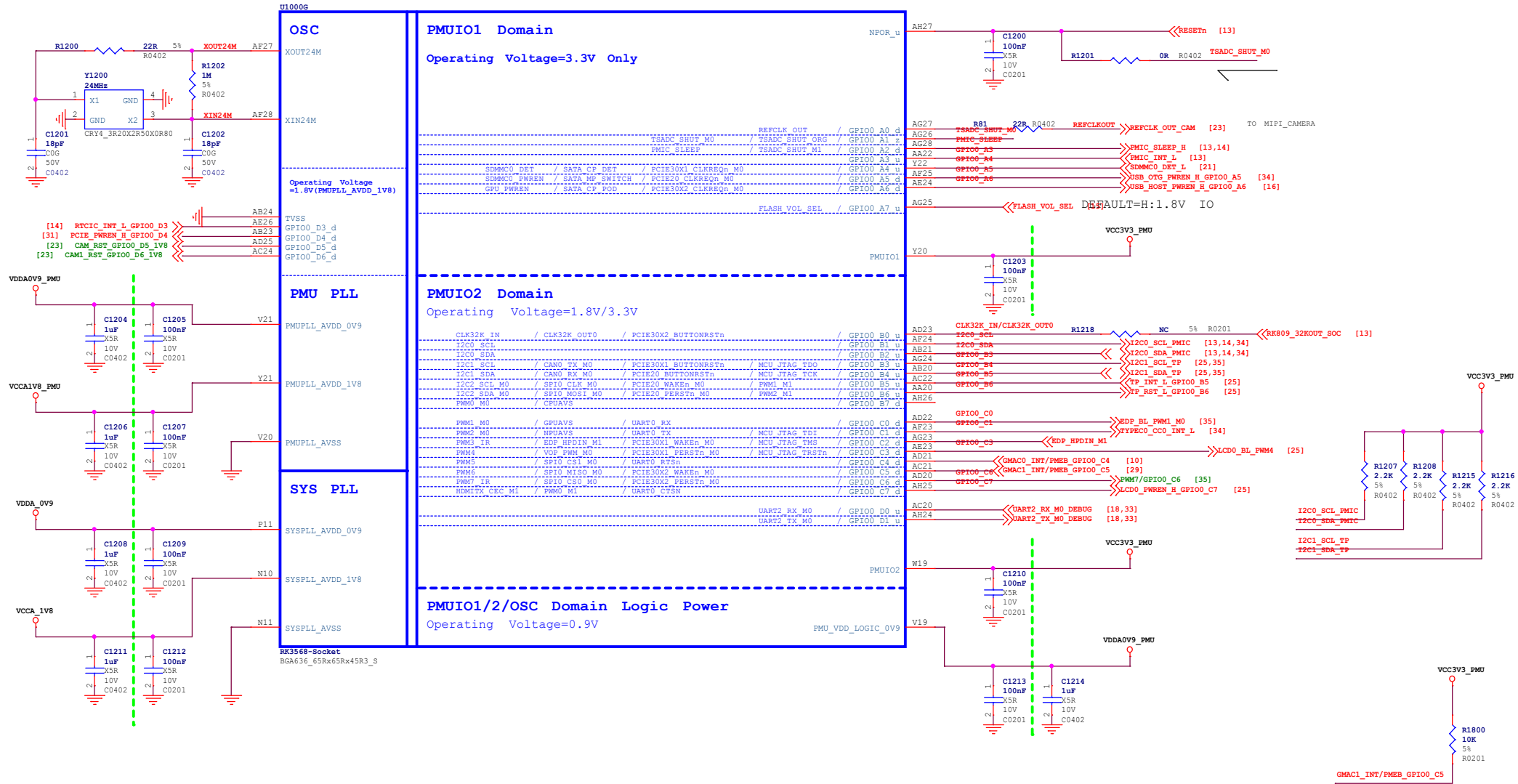
# RK3568\_F (DDR PHY)

U1000F


	DDR4	LPDDR4	DDR3	LPDDR3
[19] LPDDR4_DQ0_A	DDR_DQ0_A	F2	DDR_DQ0_A / DDR4_DQ10_A / LPDDR4_DQ0_A	DDR3_DQ0 / LPDDR3_DQ15
[19] LPDDR4_DQ1_A	DDR_DQ1_A	E1	DDR_DQ1_A / DDR4_DQ11_A / LPDDR4_DQ1_A	DDR3_DQ1 / LPDDR3_DQ14
[19] LPDDR4_DQ2_A	DDR_DQ2_A	E2	DDR_DQ2_A / DDR4_DQ12_A / LPDDR4_DQ2_A	DDR3_DQ2 / LPDDR3_DQ13
[19] LPDDR4_DQ3_A	DDR_DQ3_A	D1	DDR_DQ3_A / DDR4_DQ13_A / LPDDR4_DQ3_A	DDR3_DQ3 / LPDDR3_DQ12
[19] LPDDR4_DQ4_A	DDR_DQ4_A	F1	DDR_DQ4_A / DDR4_DQ14_A / LPDDR4_DQ4_A	DDR3_DQ4 / LPDDR3_DQ11
[19] LPDDR4_DQ5_A	DDR_DQ5_A	J2	DDR_DQ5_A / DDR4_DQ15_A / LPDDR4_DQ5_A	DDR3_DQ5 / LPDDR3_DQ10
[19] LPDDR4_DQ6_A	DDR_DQ6_A	H1	DDR_DQ6_A / DDR4_DQ16_A / LPDDR4_DQ6_A	DDR3_DQ6 / LPDDR3_DQ9
[19] LPDDR4_DQ7_A	DDR_DQ7_A	H4	DDR_DQ7_A / DDR4_DQ17_A / LPDDR4_DQ7_A	DDR3_DQ7 / LPDDR3_DQ8
[19] LPDDR4_DQ8_A	DDR_DQ8_A	M1	DDR_DQ8_A / DDR4_DQ18_A / LPDDR4_DQ8_A	DDR3_DQ8 / LPDDR3_DQ7
[19] LPDDR4_DQ9_A	DDR_DQ9_A	M2	DDR_DQ9_A / DDR4_DQ19_A / LPDDR4_DQ9_A	DDR3_DQ9 / LPDDR3_DQ6
[19] LPDDR4_DQ10_A	DDR_DQ10_A	L7	DDR_DQ10_A / DDR4_DQ20_A / LPDDR4_DQ10_A	DDR3_DQ10 / LPDDR3_DQ5
[19] LPDDR4_DQ11_A	DDR_DQ11_A	L6	DDR_DQ11_A / DDR4_DQ21_A / LPDDR4_DQ11_A	DDR3_DQ11 / LPDDR3_DQ4
[19] LPDDR4_DQ12_A	DDR_DQ12_A	K2	DDR_DQ12_A / DDR4_DQ22_A / LPDDR4_DQ12_A	DDR3_DQ12 / LPDDR3_DQ3
[19] LPDDR4_DQ13_A	DDR_DQ13_A	J6	DDR_DQ13_A / DDR4_DQ23_A / LPDDR4_DQ13_A	DDR3_DQ13 / LPDDR3_DQ2
[19] LPDDR4_DQ14_A	DDR_DQ14_A	J7	DDR_DQ14_A / DDR4_DQ24_A / LPDDR4_DQ14_A	DDR3_DQ14 / LPDDR3_DQ1
[19] LPDDR4_DQ15_A	DDR_DQ15_A	L4	DDR_DQ15_A / DDR4_DQ25_A / LPDDR4_DQ15_A	DDR3_DQ15 / LPDDR3_DQ0
[19] LPDDR4_DM1_A	DDR_DM1_A	J4	DDR_DM1_A / DDR4_DM0_A / LPDDR4_DM1_A	DDR3_DM1 / LPDDR3_DM3
[19] LPDDR4_DQS1P_A	DDR_DQS1P_A	L2	DDR_DQS1P_A / DDR4_DQS1_P_A / LPDDR4_DQS1P_A	DDR3_DQS1P / LPDDR3_DQS3P
[19] LPDDR4_DQS1N_A	DDR_DQS1N_A	L1	DDR_DQS1N_A / DDR4_DQS1_N_A / LPDDR4_DQS1N_A	DDR3_DQS1N / LPDDR3_DQS3N
[19] LPDDR4_DQ0_B	DDR_DQ0_B	B10	DDR_DQ0_B / DDR4_DQ07_B / LPDDR4_DQ0_B	DDR3_DQ16 / LPDDR3_DQ1
[19] LPDDR4_DQ1_B	DDR_DQ1_B	A9	DDR_DQ1_B / DDR4_DQ08_B / LPDDR4_DQ1_B	DDR3_DQ17 / LPDDR3_DQ0
[19] LPDDR4_DQ2_B	DDR_DQ2_B	D12	DDR_DQ2_B / DDR4_DQ09_B / LPDDR4_DQ2_B	DDR3_DQ18 / LPDDR3_DQ0
[19] LPDDR4_DQ3_B	DDR_DQ3_B	A12	DDR_DQ3_B / DDR4_DQ10_B / LPDDR4_DQ3_B	DDR3_DQ19 / LPDDR3_DQ0
[19] LPDDR4_DQ4_B	DDR_DQ4_B	E12	DDR_DQ4_B / DDR4_DQ11_B / LPDDR4_DQ4_B	DDR3_DQ20 / LPDDR3_DQ0
[19] LPDDR4_DQ5_B	DDR_DQ5_B	A12	DDR_DQ5_B / DDR4_DQ12_B / LPDDR4_DQ5_B	DDR3_DQ21 / LPDDR3_DQ0
[19] LPDDR4_DQ6_B	DDR_DQ6_B	D15	DDR_DQ6_B / DDR4_DQ13_B / LPDDR4_DQ6_B	DDR3_DQ22 / LPDDR3_DQ0
[19] LPDDR4_DQ7_B	DDR_DQ7_B	E15	DDR_DQ7_B / DDR4_DQ14_B / LPDDR4_DQ7_B	DDR3_DQ23 / LPDDR3_DQ0
[19] LPDDR4_DQ8_B	DDR_DQ8_B	E14	DDR_DQ8_B / DDR4_DQ15_B / LPDDR4_DQ8_B	DDR3_DQ24 / LPDDR3_DQ0
[19] LPDDR4_DQ9_B	DDR_DQ9_B	D14	DDR_DQ9_B / DDR4_DQ16_B / LPDDR4_DQ9_B	DDR3_DQ25 / LPDDR3_DQ0
[19] LPDDR4_DQ10_B	DDR_DQ10_B	A16	DDR_DQ10_B / DDR4_DQ17_B / LPDDR4_DQ10_B	DDR3_DQ26 / LPDDR3_DQ0
[19] LPDDR4_DQ11_B	DDR_DQ11_B	B17	DDR_DQ11_B / DDR4_DQ18_B / LPDDR4_DQ11_B	DDR3_DQ27 / LPDDR3_DQ0
[19] LPDDR4_DQ12_B	DDR_DQ12_B	B18	DDR_DQ12_B / DDR4_DQ19_B / LPDDR4_DQ12_B	DDR3_DQ28 / LPDDR3_DQ0
[19] LPDDR4_DQ13_B	DDR_DQ13_B	B13	DDR_DQ13_B / DDR4_DQ20_B / LPDDR4_DQ13_B	DDR3_DQ29 / LPDDR3_DQ0
[19] LPDDR4_DQ14_B	DDR_DQ14_B	D17	DDR_DQ14_B / DDR4_DQ21_B / LPDDR4_DQ14_B	DDR3_DQ30 / LPDDR3_DQ0
[19] LPDDR4_DQ15_B	DDR_DQ15_B	B14	DDR_DQ15_B / DDR4_DQ22_B / LPDDR4_DQ15_B	DDR3_DQ31 / LPDDR3_DQ0
[19] LPDDR4_DM1_B	DDR_DM1_B	E17	DDR_DM1_B / DDR4_DM1_B / LPDDR4_DM1_B	DDR3_DM3 / LPDDR3_DM2
[19] LPDDR4_DQS1P_B	DDR_DQS1P_B	B15	DDR_DQS1P_B / DDR4_DQS1_P_B / LPDDR4_DQS1P_B	DDR3_DQS3P / LPDDR3_DQS2P
[19] LPDDR4_DQS1N_B	DDR_DQS1N_B	A15	DDR_DQS1N_B / DDR4_DQS1_N_B / LPDDR4_DQS1N_B	DDR3_DQS3N / LPDDR3_DQS2N
X P5	DDR_ECC_DQ0		DDR4_ECC_DQ0 / --- / ---	DDR3_ECC_DQ0
X M4	DDR_ECC_DQ1		DDR4_ECC_DQ1 / --- / ---	DDR3_ECC_DQ1
X H5	DDR_ECC_DQ2		DDR4_ECC_DQ2 / --- / ---	DDR3_ECC_DQ2
X R5	DDR_ECC_DQ3		DDR4_ECC_DQ3 / --- / ---	DDR3_ECC_DQ3
X M7	DDR_ECC_DQ4		DDR4_ECC_DQ4 / --- / ---	DDR3_ECC_DQ4
X R7	DDR_ECC_DQ5		DDR4_ECC_DQ5 / --- / ---	DDR3_ECC_DQ5
X P4	DDR_ECC_DQ6		DDR4_ECC_DQ6 / --- / ---	DDR3_ECC_DQ6
X R4	DDR_ECC_DQ7		DDR4_ECC_DQ7 / --- / ---	DDR3_ECC_DQ7
X P7	DDR_ECC_DM		DDR4_ECC_DM / --- / ---	DDR3_ECC_DM
X P2	DDR_ECC_DQS_P		DDR4_ECC_DQS_P / --- / ---	DDR3_ECC_DQS_P
X P1	DDR_ECC_DQS_N		DDR4_ECC_DQS_N / --- / ---	DDR3_ECC_DQS_N

DDR4	LPDDR4	DDR3	LPDDR3
DDR4_A0	LPDDR4_CLKP_B	DDR3_A9	---
DDR4_A1	LPDDR4_A1_A	DDR3_A4	LPDDR3_A5
DDR4_A2	LPDDR4_A2_A	DDR3_A5	LPDDR3_A6
DDR4_A3	LPDDR4_CKE1_A	DDR3_A3	---
DDR4_A4	LPDDR4_A3_B	DDR3_BA1	LPDDR3_A3
DDR4_A5	LPDDR4_A3_B	DDR3_A11	LPDDR3_A2
DDR4_A6	LPDDR4_A1_B	DDR3_A11	LPDDR3_A1
DDR4_A7	LPDDR4_ODT0_CA_B	DDR3_A5	---
DDR4_A8	LPDDR4_ODT0_CA_A	DDR3_A6	LPDDR3_A9
DDR4_A9	LPDDR4_CLKN_B	DDR3_A5	---
DDR4_A10	LPDDR4_CKE0_B	DDR3_A10	---
DDR4_A11	LPDDR4_A0_A	---	LPDDR3_A8
DDR4_A12	LPDDR4_A3_A	DDR3_BA2	---
DDR4_A13	LPDDR4_A0_B	DDR3_A14	LPDDR3_A0
DDR4_A14	LPDDR4_A4_A	DDR3_A15	LPDDR3_A5
DDR4_A15	LPDDR4_A2_A	DDR3_A0	---
DDR4_A16	RASn	DDR3_RASn	LPDDR3_A7
DDR4_BA0	LPDDR4_CKE1_B	DDR3_CASn	---
DDR4_BA1	LPDDR4_A4_B	DDR3_A12	LPDDR3_A4
DDR4_BG0	LPDDR4_ODT1_CA_B	DDR3_Wen	---
DDR4_BG1	LPDDR4_ODT1_CA_A	---	---
DDR4_CKE	LPDDR4_CKE0_A	DDR3_CKE	LPDDR3_CKE
DDR4_CLKP	LPDDR4_CLKP_A	DDR3_CLKP	LPDDR3_CLKP
DDR4_CLKN	LPDDR4_CLKN_A	DDR3_CLKN	LPDDR3_CLKN
DDR4_CSn0	LPDDR4_CSn0_A	DDR3_ODT1	LPDDR3_ODT0
DDR4_CSn1	LPDDR4_CSn1_B	DDR3_CSn0	---
DDR4_CSn2	LPDDR4_CSn2_B	DDR3_CSn1	---
DDR4_CSn3	LPDDR4_CSn3_B	DDR3_CSn2	---
DDR4_CSn4	LPDDR4_CSn4_B	DDR3_CSn3	---
DDR4_CSn5	LPDDR4_CSn5_B	DDR3_CSn4	---
DDR4_CSn6	LPDDR4_CSn6_B	DDR3_CSn5	---
DDR4_CSn7	LPDDR4_CSn7_B	DDR3_CSn6	---
DDR4_CSn8	LPDDR4_CSn8_B	DDR3_CSn7	---
DDR4_CSn9	LPDDR4_CSn9_B	DDR3_CSn8	---
DDR4_CSn10	LPDDR4_CSn10_B	DDR3_CSn9	---
DDR4_CSn11	LPDDR4_CSn11_B	DDR3_CSn10	---
DDR4_CSn12	LPDDR4_CSn12_B	DDR3_CSn11	---
DDR4_CSn13	LPDDR4_CSn13_B	DDR3_CSn12	---
DDR4_CSn14	LPDDR4_CSn14_B	DDR3_CSn13	---
DDR4_CSn15	LPDDR4_CSn15_B	DDR3_CSn14	---
DDR4_CSn16	LPDDR4_CSn16_B	DDR3_CSn15	---
DDR4_CSn17	LPDDR4_CSn17_B	DDR3_CSn16	---
DDR4_CSn18	LPDDR4_CSn18_B	DDR3_CSn17	---
DDR4_CSn19	LPDDR4_CSn19_B	DDR3_CSn18	---
DDR4_CSn20	LPDDR4_CSn20_B	DDR3_CSn19	---
DDR4_CSn21	LPDDR4_CSn21_B	DDR3_CSn20	---
DDR4_CSn22	LPDDR4_CSn22_B	DDR3_CSn21	---
DDR4_CSn23	LPDDR4_CSn23_B	DDR3_CSn22	---
DDR4_CSn24	LPDDR4_CSn24_B	DDR3_CSn23	---
DDR4_CSn25	LPDDR4_CSn25_B	DDR3_CSn24	---
DDR4_CSn26	LPDDR4_CSn26_B	DDR3_CSn25	---
DDR4_CSn27	LPDDR4_CSn27_B	DDR3_CSn26	---
DDR4_CSn28	LPDDR4_CSn28_B	DDR3_CSn27	---
DDR4_CSn29	LPDDR4_CSn29_B	DDR3_CSn28	---
DDR4_CSn30	LPDDR4_CSn30_B	DDR3_CSn29	---
DDR4_CSn31	LPDDR4_CSn31_B	DDR3_CSn30	---
DDR4_CSn32	LPDDR4_CSn32_B	DDR3_CSn31	---
DDR4_CSn33	LPDDR4_CSn33_B	DDR3_CSn32	---
DDR4_CSn34	LPDDR4_CSn34_B	DDR3_CSn33	---
DDR4_CSn35	LPDDR4_CSn35_B	DDR3_CSn34	---
DDR4_CSn36	LPDDR4_CSn36_B	DDR3_CSn35	---
DDR4_CSn37	LPDDR4_CSn37_B	DDR3_CSn36	---
DDR4_CSn38	LPDDR4_CSn38_B	DDR3_CSn37	---
DDR4_CSn39	LPDDR4_CSn39_B	DDR3_CSn38	---
DDR4_CSn40	LPDDR4_CSn40_B	DDR3_CSn39	---
DDR4_CSn41	LPDDR4_CSn41_B	DDR3_CSn40	---
DDR4_CSn42	LPDDR4_CSn42_B	DDR3_CSn41	---
DDR4_CSn43	LPDDR4_CSn43_B	DDR3_CSn42	---
DDR4_CSn44	LPDDR4_CSn44_B	DDR3_CSn43	---
DDR4_CSn45	LPDDR4_CSn45_B	DDR3_CSn44	---
DDR4_CSn46	LPDDR4_CSn46_B	DDR3_CSn45	---
DDR4_CSn47	LPDDR4_CSn47_B	DDR3_CSn46	---
DDR4_CSn48	LPDDR4_CSn48_B	DDR3_CSn47	---
DDR4_CSn49	LPDDR4_CSn49_B	DDR3_CSn48	---
DDR4_CSn50	LPDDR4_CSn50_B	DDR3_CSn49	---
DDR4_CSn51	LPDDR4_CSn51_B	DDR3_CSn50	---
DDR4_CSn52	LPDDR4_CSn52_B	DDR3_CSn51	---
DDR4_CSn53	LPDDR4_CSn53_B	DDR3_CSn52	---
DDR4_CSn54	LPDDR4_CSn54_B	DDR3_CSn53	---
DDR4_CSn55	LPDDR4_CSn55_B	DDR3_CSn54	---
DDR4_CSn56	LPDDR4_CSn56_B	DDR3_CSn55	---
DDR4_CSn57	LPDDR4_CSn57_B	DDR3_CSn56	---
DDR4_CSn58	LPDDR4_CSn58_B	DDR3_CSn57	---
DDR4_CSn59	LPDDR4_CSn59_B	DDR3_CSn58	---
DDR4_CSn60	LPDDR4_CSn60_B	DDR3_CSn59	---
DDR4_CSn61	LPDDR4_CSn61_B	DDR3_CSn60	---
DDR4_CSn62	LPDDR4_CSn62_B	DDR3_CSn61	---
DDR4_CSn63	LPDDR4_CSn63_B	DDR3_CSn62	---
DDR4_CSn64	LPDDR4_CSn64_B	DDR3_CSn63	---
DDR4_CSn65	LPDDR4_CSn65_B	DDR3_CSn64	---
DDR4_CSn66	LPDDR4_CSn66_B	DDR3_CSn65	---
DDR4_CSn67	LPDDR4_CSn67_B	DDR3_CSn66	---
DDR4_CSn68	LPDDR4_CSn68_B	DDR3_CSn67	---
DDR4_CSn69	LPDDR4_CSn69_B	DDR3_CSn68	---
DDR4_CSn70	LPDDR4_CSn70_B	DDR3_CSn69	---
DDR4_CSn71	LPDDR4_CSn71_B	DDR3_CSn70	---
DDR4_CSn72	LPDDR4_CSn72_B	DDR3_CSn71	---
DDR4_CSn73	LPDDR4_CSn73_B	DDR3_CSn72	---
DDR4_CSn74	LPDDR4_CSn74_B	DDR3_CSn73	---
DDR4_CSn75	LPDDR4_CSn75_B	DDR3_CSn74	---
DDR4_CSn76	LPDDR4_CSn76_B	DDR3_CSn75	---
DDR4_CSn77	LPDDR4_CSn77_B	DDR3_CSn76	---
DDR4_CSn78	LPDDR4_CSn78_B	DDR3_CSn77	---
DDR4_CSn79	LPDDR4_CSn79_B	DDR3_CSn78	---
DDR4_CSn80	LPDDR4_CSn80_B	DDR3_CSn79	---
DDR4_CSn81	LPDDR4_CSn81_B	DDR3_CSn80	---
DDR4_CSn82	LPDDR4_CSn82_B	DDR3_CSn81	---
DDR4_CSn83	LPDDR4_CSn83_B	DDR3_CSn82	---
DDR4_CSn84	LPDDR4_CSn84_B	DDR3_CSn83	---
DDR4_CSn85	LPDDR4_CSn85_B	DDR3_CSn84	---
DDR4_CSn86	LPDDR4_CSn86_B	DDR3_CSn85	---
DDR4_CSn87	LPDDR4_CSn87_B	DDR3_CSn86	---
DDR4_CSn88	LPDDR4_CSn88_B	DDR3_CSn87	---
DDR4_CSn89	LPDDR4_CSn89_B	DDR3_CSn88	---
DDR4_CSn90	LPDDR4_CSn90_B	DDR3_CSn89	---
DDR4_CSn91	LPDDR4_CSn91_B	DDR3_CSn90	---
DDR4_CSn92	LPDDR4_CSn92_B	DDR3_CSn91	---
DDR4_CSn93	LPDDR4_CSn93_B	DDR3_CSn92	---
DDR4_CSn94	LPDDR4_CSn94_B	DDR3_CSn93	---
DDR4_CSn95	LPDDR4_CSn95_B	DDR3_CSn94	---
DDR4_CSn96	LPDDR4_CSn96_B	DDR3_CSn95	---
DDR4_CSn97	LPDDR4_CSn97_B	DDR3_CSn96	---
DDR4_CSn98	LPDDR4_CSn98_B	DDR3_CSn97	---
DDR4_CSn99	LPDDR4_CSn99_B	DDR3_CSn98	---
DDR4_CSn100	LPDDR4_CSn100_B	DDR3_CSn99	---
DDR4_CSn101	LPDDR4_CSn101_B	DDR3_CSn100	---
DDR4_CSn102	LPDDR4_CSn102_B	DDR3_CSn101	---
DDR4_CSn103	LPDDR4_CSn103_B	DDR3_CSn102	---
DDR4_CSn104	LPDDR4_CSn104_B	DDR3_CSn103	---
DDR4_CSn105	LPDDR4_CSn105_B	DDR3_CSn104	---
DDR4_CSn106	LPDDR4_CSn106_B	DDR3_CSn105	---
DDR4_CSn107	LPDDR4_CSn107_B	DDR3_CSn106	---
DDR4_CSn108	LPDDR4_CSn108_B	DDR3_CSn107	---
DDR4_CSn109	LPDDR4_CSn109_B	DDR3_CSn108	---
DDR4_CSn110	LPDDR4_CSn110_B	DDR3_CSn109	---
DDR4_CSn111	LPDDR4_CSn111_B	DDR3_CSn110	---
DDR4_CSn112	LPDDR4_CSn112_B	DDR3_CSn111	---
DDR4_CSn113	LPDDR4_CSn113_B	DDR3_CSn112	---
DDR4_CSn114	LPDDR4_CSn114_B	DDR3_CSn113	---
DDR4_CSn115	LPDDR4_CSn115_B	DDR3_CSn114	---
DDR4_CSn116	LPDDR4_CSn116_B	DDR3_CSn115	---
DDR4_CSn117	LPDDR4_CSn117_B	DDR3_CSn116	---
DDR4_CSn118	LPDDR4_CSn118_B	DDR3_CSn117	---
DDR4_CSn119	LPDDR4_CSn119_B	DDR3_CSn118	---
DDR4_CSn120	LPDDR4_CSn120_B	DDR3_CSn119	---
DDR4_CSn121	LPDDR4_CSn121_B	DDR3_CSn120	---
DDR4_CSn122	LPDDR4_CSn122_B	DDR3_CSn121	---
DDR4_CSn123	LPDDR4_CSn123_B	DDR3_CSn122	---
DDR4_CSn124	LPDDR4_CSn124_B	DDR3_CSn123	---
DDR4_CSn125	LPDDR4_CSn125_B	DDR3_CSn124	---
DDR4_CSn126	LPDDR4_CSn126_B	DDR3_CSn125	---
DDR4_CSn127	LPDDR4_CSn127_B	DDR3_CSn126	---
DDR4_CSn128	LPDDR4_CSn128_B	DDR3_CSn127	---
DDR4_CSn129	LPDDR4_CSn129_B	DDR3_CSn128	---
DDR4_CSn130	LPDDR4_CSn130_B	DDR3_CSn129	---
DDR4_CSn131	LPDDR4_CSn131_B	DDR3_CSn130	---
DDR4_CSn132	LPDDR4_CSn132_B	DDR3_CSn131	---
DDR4_CSn133	LPDDR4_CSn133_B	DDR3_C	

# RK3568\_G (OSC/PLL/PMUIO1/2)



**Note:**  
Caps between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

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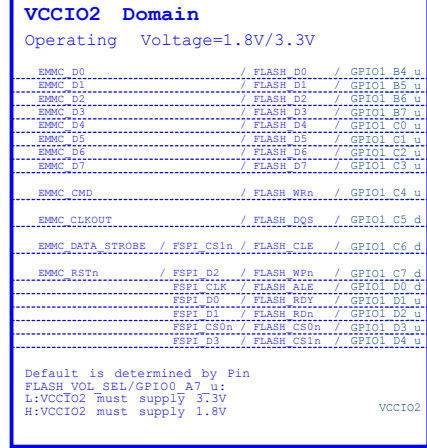
**Title:** RK3568\_OSC/PLL/PMUIO  
**File:** ROC-3568-PC  
**REV:** V1.1

**Create Date:** Monday, March 30, 2020  
**Modify Date:** Tuesday, August 09, 2022

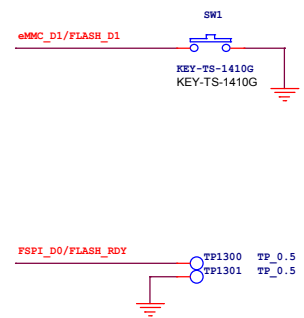
**Page Num:** 4  
**Page Total:** 36

# RK3568\_I (VCCIO2 Domain)

U1000I

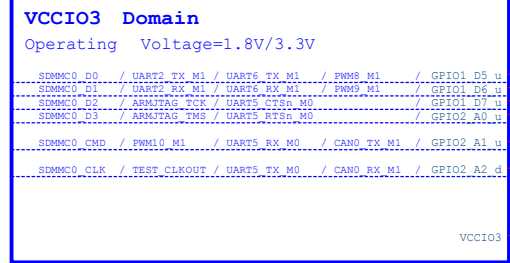


RK3568-Socket  
BGA636\_65Rx65Rx45R3\_S



# RK3568\_J (VCCIO3 Domain)

U1000J



RK3568-Socket  
BGA636\_65Rx65Rx45R3\_S

**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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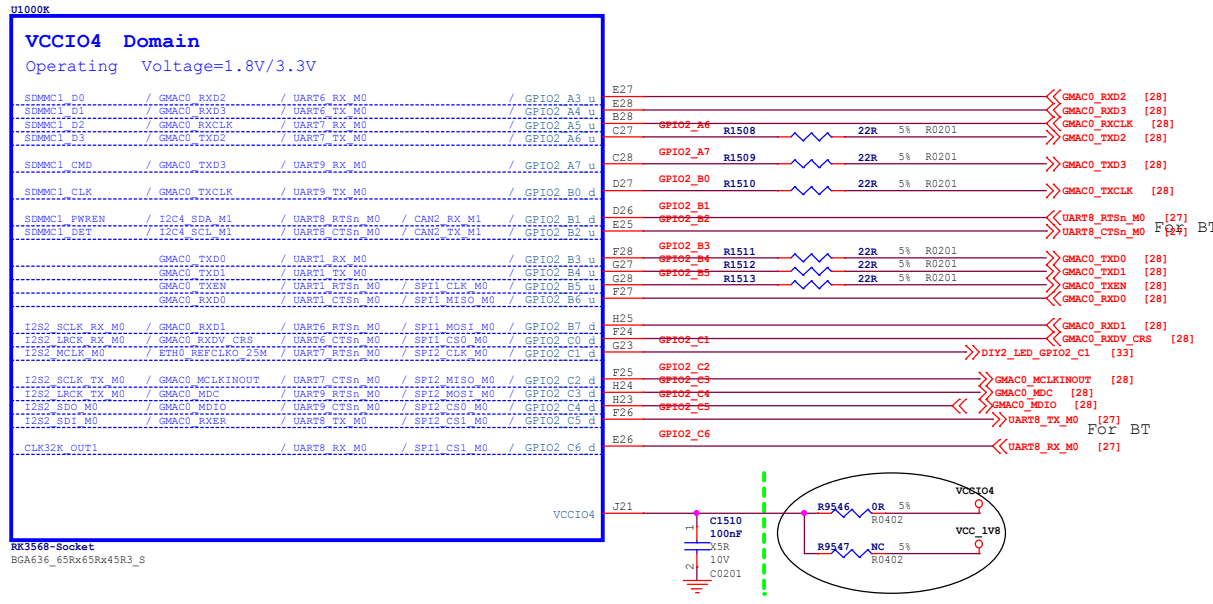
Title: RK3568 Flash/SD Controller  
File: ROC-3568-PC  
REV: V1.1

Create Date: Monday, March 30, 2020  
Modify Date: Tuesday, August 09, 2022

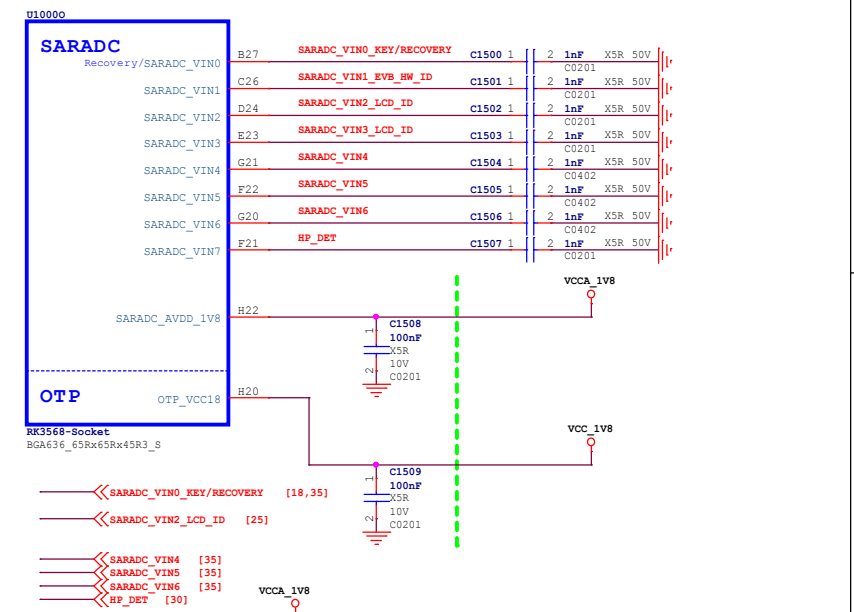
Page Num: 5  
Page Total: 36



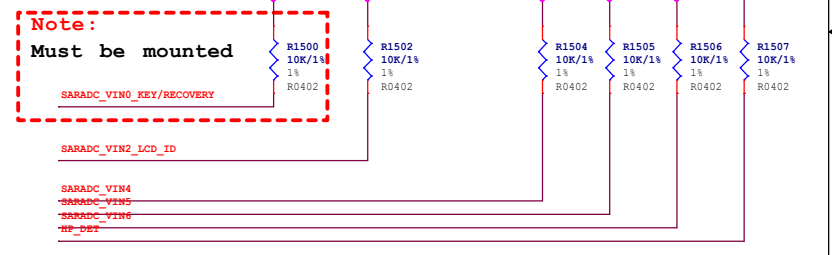
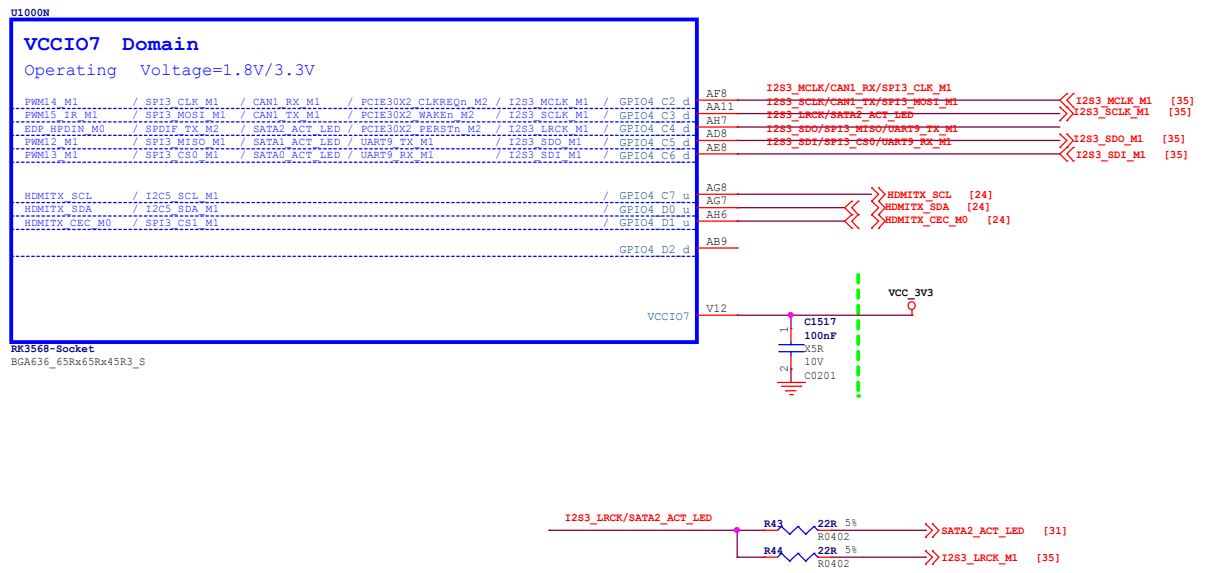
# RK3568\_K (VCCIO4 Domain)



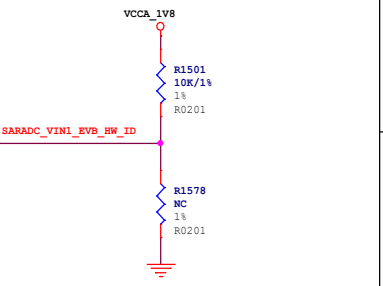
# RK3568\_O (SARADC/OTP)



# RK3568\_N (VCCIO7 Domain)



SARADC_VIN1_EVB_HW_ID	Rup	Rdown	ADC	
EVB1	10K	DNP	1023	1.8V
EVB2	20K	100K	852	1.5V
EVB3	18K	36K	681	1.2V
EVB4	51K	51K	512	0.9V
EVB5	36K	18K	340	0.6V
EVB6	100K	20K	170	0.3V
EVB7	DNP	10K	0	0V
EVB8				



**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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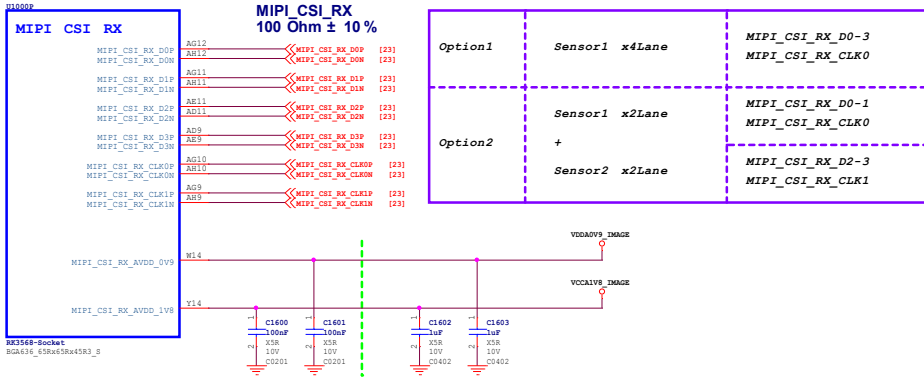
**Title:** RK3568 SARADC/GPIO  
**File:** ROC-3568-PC  
**Rev:** V1.1

**Create Date:** Monday, March 30, 2020  
**Modify Date:** Tuesday, August 09, 2022

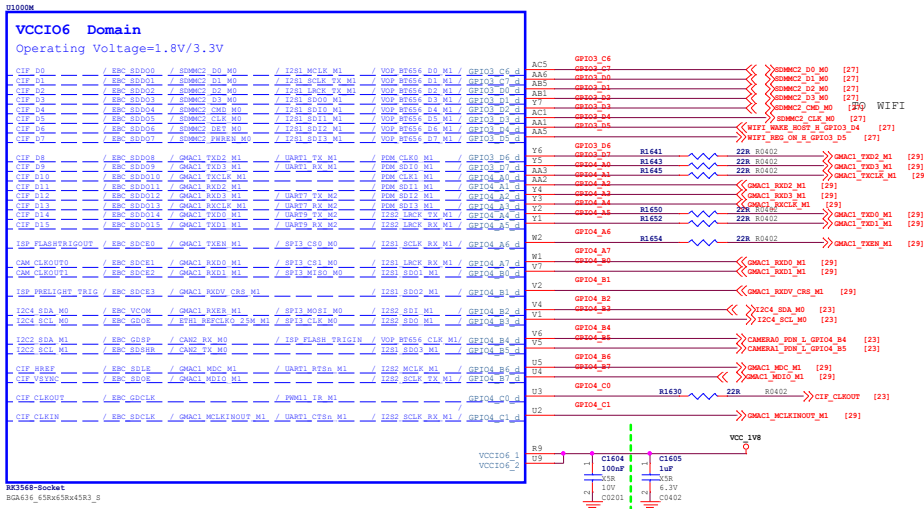
**Page Num:** 7  
**Page Total:** 36



# RK3568\_P(MIPI\_CSI\_RX)



# RK3568\_M(VCCIO6 Domain)



Mode	16bit	12bit	10bit	8bit
CFI_D0	D0	--	--	--
CFI_D1	D1	--	--	--
CFI_D2	D2	--	--	--
CFI_D3	D3	--	--	--
CFI_D4	D4	D0	--	--
CFI_D5	D5	D1	--	--
CFI_D6	D6	D2	D0	--
CFI_D7	D7	D3	D1	--
CFI_D8	D8	D4	D2	D0
CFI_D9	D9	D5	D3	D1
CFI_D10	D10	D6	D4	D2
CFI_D11	D11	D7	D5	D3
CFI_D12	D12	D8	D6	D4
CFI_D13	D13	D9	D7	D5
CFI_D14	D14	D10	D8	D6
CFI_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input  
 Support BT656 YCbCr 422 8bit input  
 Support RAW 8/10/12bit input  
 Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling  
 Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

**Note:**  
 Caps of between dashed green lines and U1000 should be placed under the U1000 package.  
 Other caps should be placed close to the U1000 package

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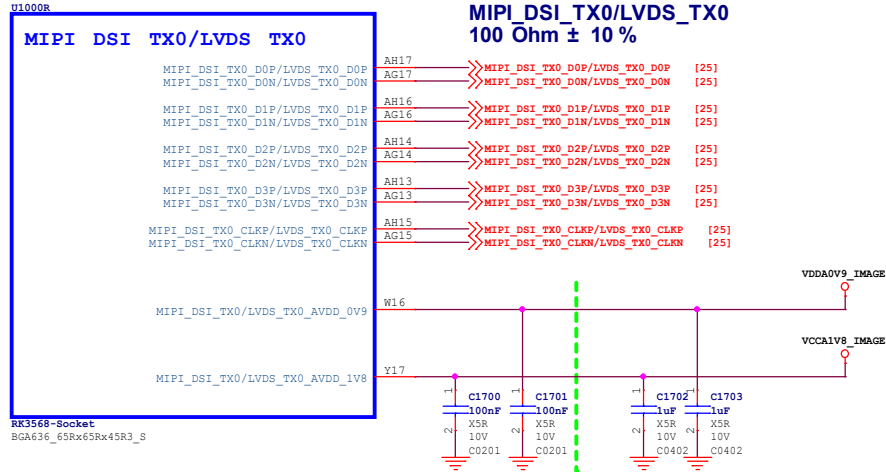
**Title: RK3568 VI Interface**

**File: ROC-3568-PC**

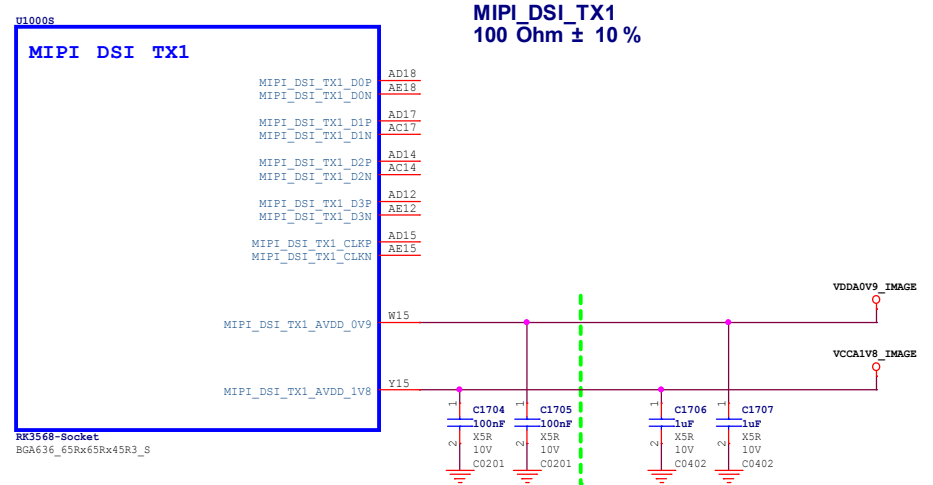
Create Date: Monday, March 30, 2020 Page: Num 8  
 Modify Date: Tuesday, August 09, 2022 Page: Total 36



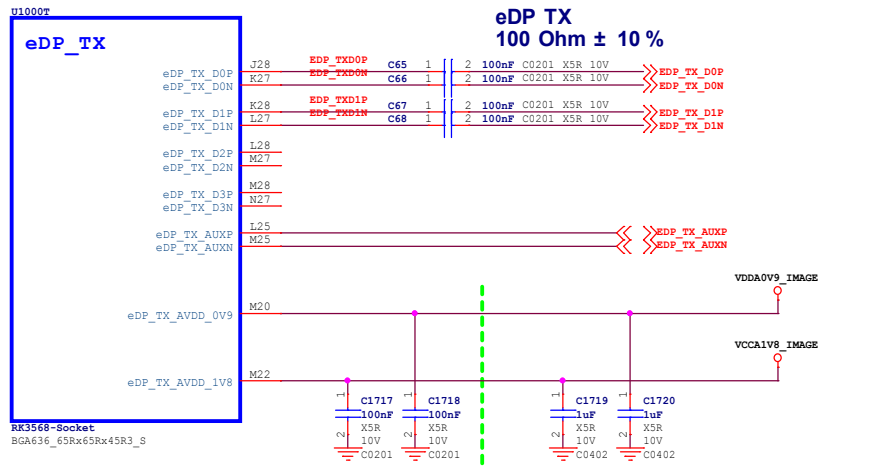
# RK3568\_R (MIPI\_DSI\_TX0/LVDS\_TX0)



# RK3568\_S (MIPI\_DSI\_TX1)

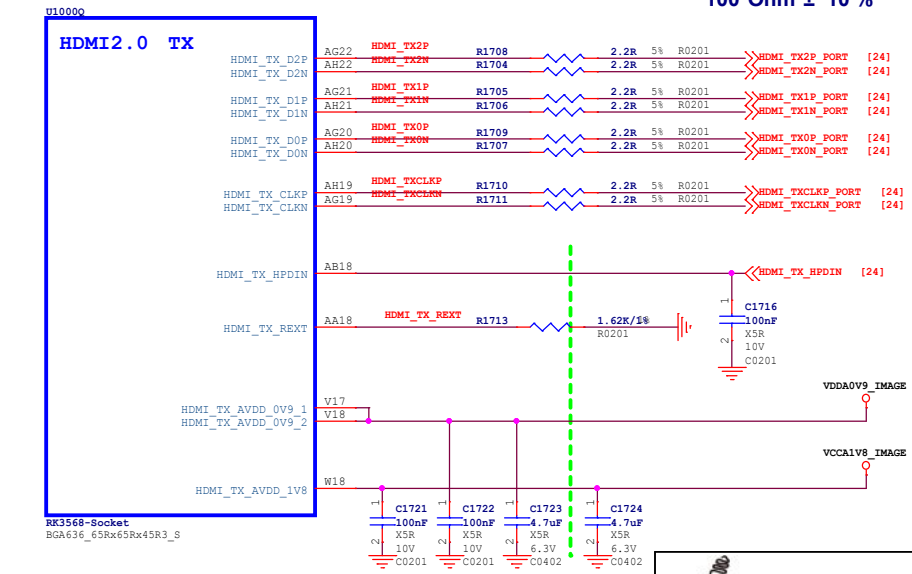



# RK3568\_T (eDP TX)



**Note:**  
 Caps of between dashed green lines and U1000 should be placed under the U1000 package.  
 Other caps should be placed close to the U1000 package.

# RK3568\_Q (HDMI2.0 TX)



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**Title: RK3568\_V0 Interface 1**

**File: ROC-3568-PC** REV: V1.1

**Create Date: Monday, March 30, 2020** Page Num: 9

**Modify Date: Tuesday, August 09, 2022** Page Total: 36

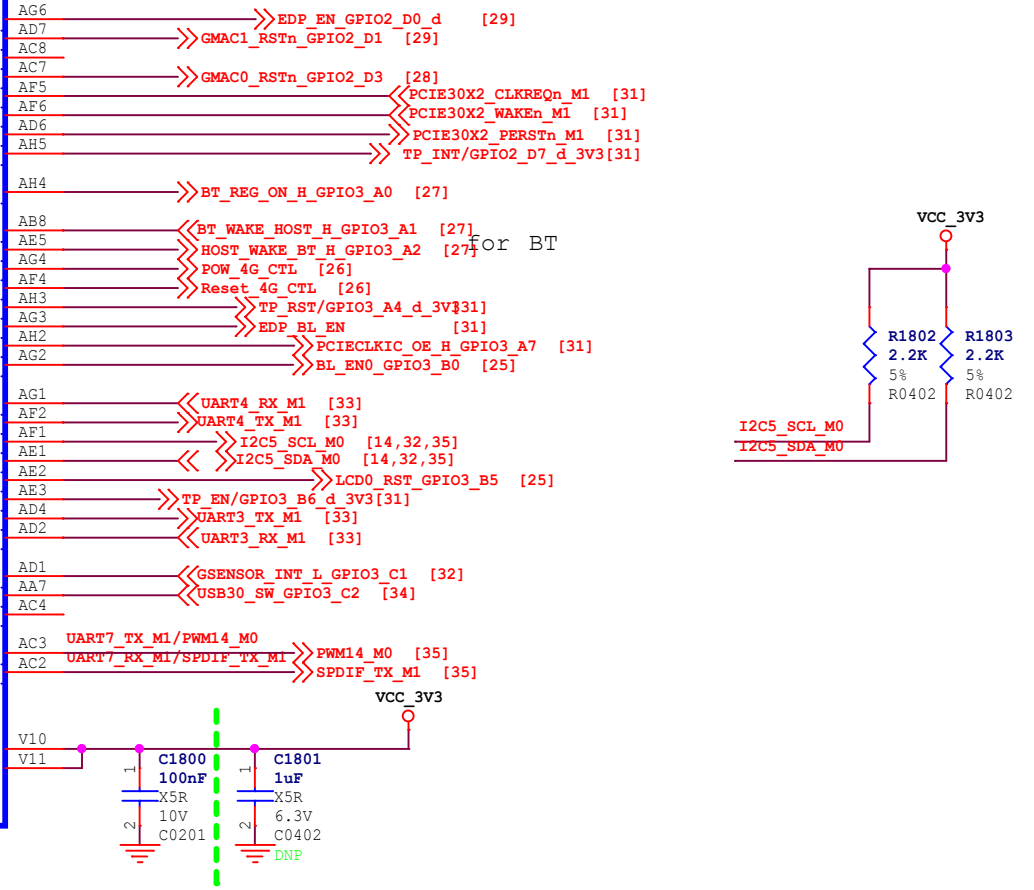
# RK3568\_L (VCCIO5 Domain)

U1000L

## VCCIO5 Domain


Operating Voltage=1.8V/3.3V

LCDC D0	/ VOP BT656 D0 M0	/ SPI0 MISO M1	/ PCIE20 CLKREQn M1	/ I2S1 MCLK M2	/ GPIO2 D0 d
LCDC D1	/ VOP BT656 D1 M0	/ SPI0 MOSI M1	/ PCIE20 WAKEn M1	/ I2S1 SCLK TX M2	/ GPIO2 D1 d
LCDC D2	/ VOP BT656 D2 M0	/ SPI0 CS0 M1	/ PCIE30X1 CLKREQn M1	/ I2S1 LRCK TX M2	/ GPIO2 D2 d
LCDC D3	/ VOP BT656 D3 M0	/ SPI0 CLK M1	/ PCIE30X1 WAKEn M1	/ I2S1 SDIO M2	/ GPIO2 D3 d
LCDC D4	/ VOP BT656 D4 M0	/ SPI2 CS1 M1	/ PCIE30X2 CLKREQn M1	/ I2S1 SDI1 M2	/ GPIO2 D4 d
LCDC D5	/ VOP BT656 D5 M0	/ SPI2 CS0 M1	/ PCIE30X2 WAKEn M1	/ I2S1 SDI2 M2	/ GPIO2 D5 d
LCDC D6	/ VOP BT656 D6 M0	/ SPI2 MOSI M1	/ PCIE30X2 PERSTn M1	/ I2S1 SDI3 M2	/ GPIO2 D6 d
LCDC D7	/ VOP BT656 D7 M0	/ SPI2 MISO M1	/ UART8 TX M1	/ I2S1 SDO0 M2	/ GPIO2 D7 d
LCDC CLK	/ VOP BT656 CLK M0	/ SPI2 CLK M1	/ UART8 RX M1	/ I2S1 SDO1 M2	/ GPIO3 A0 d
LCDC D8	/ VOP BT1120 D0	/ SPI1 CS0 M1	/ PCIE30X1 PERSTn M1	/ SDMMC2 D0 M1	/ GPIO3 A1 d
LCDC D9	/ VOP BT1120 D1	/ GMAC1 TXD2 M0	/ I2S3 MCLK M0	/ SDMMC2 D1 M1	/ GPIO3 A2 d
LCDC D10	/ VOP BT1120 D2	/ GMAC1 TXD3 M0	/ I2S3 SCLK M0	/ SDMMC2 D2 M1	/ GPIO3 A3 d
LCDC D11	/ VOP BT1120 D3	/ GMAC1 RXD2 M0	/ I2S3 LRCK M0	/ SDMMC2 D3 M1	/ GPIO3 A4 d
LCDC D12	/ VOP BT1120 D4	/ GMAC1 RXD3 M0	/ I2S3 SDO M0	/ SDMMC2 CMD M1	/ GPIO3 A5 d
LCDC D13	/ VOP BT1120 CLK	/ GMAC1 TXCLK M0	/ I2S3 SDI M0	/ SDMMC2 CLK M1	/ GPIO3 A6 d
LCDC D14	/ VOP BT1120 D5	/ GMAC1 RXCLK M0	/ SDMMC2 DET M1	/ GPIO3 A7 d	
LCDC D15	/ VOP BT1120 D6	/ ETH1 REFCLK0 Z5M M0	/ SDMMC2 PWREN M1	/ GPIO3 B0 d	
LCDC D16	/ VOP BT1120 D7	/ GMAC1 RXD0 M0	/ UART4 RX M1	/ PWM8 M0	/ GPIO3 B1 d
LCDC D17	/ VOP BT1120 D8	/ GMAC1 RXD1 M0	/ UART4 TX M1	/ PWM9 M0	/ GPIO3 B2 d
LCDC D18	/ VOP BT1120 D9	/ GMAC1 RXDV CRS M0	/ I2C5 SCL M0	/ PDM SDI0 M2	/ GPIO3 B3 d
LCDC D19	/ VOP BT1120 D10	/ GMAC1 RXER M0	/ I2C5 SDA M0	/ PDM SDI1 M2	/ GPIO3 B4 d
LCDC D20	/ VOP BT1120 D11	/ GMAC1 TXD0 M0	/ I2C3 SCL M1	/ PWM10 M0	/ GPIO3 B5 d
LCDC D21	/ VOP BT1120 D12	/ GMAC1 TXD1 M0	/ I2C3 SDA M1	/ PWM11 IR M0	/ GPIO3 B6 d
LCDC D22	/ PWM12 M0	/ GMAC1 TXEN M0	/ UART3 TX M1	/ PDM SDI2 M2	/ GPIO3 B7 d
LCDC D23	/ PWM13 M0	/ GMAC1 MCLKINOUT M0	/ UART3 RX M1	/ PDM SDI3 M2	/ GPIO3 C0 d
LCDC HSYNC	/ VOP BT1120 D13	/ SPI1 MOSI M1	/ PCIE20 PERSTn M1	/ I2S1 SDO2 M2	/ GPIO3 C1 d
LCDC VSYNC	/ VOP BT1120 D14	/ SPI1 MISO M1	/ UART5 TX M1	/ I2S1 SDO3 M2	/ GPIO3 C2 d
LCDC DEN	/ VOP BT1120 D15	/ SPI1 CLK M1	/ UART5 RX M1	/ I2S1 SCLK RX M2	/ GPIO3 C3 d
PWM14 M0	/ VOP PWM M1	/ GMAC1 MDC M0	/ UART7 TX M1	/ PDM CLK1 M2	/ GPIO3 C4 d
PWM15 IR M0	/ SPDIF TX M1	/ GMAC1 MDIO M0	/ UART7 RX M1	/ I2S1 LRCK RX M2	/ GPIO3 C5 d



RK3568-Socket  
BGA636\_65Rx65Rx45R3\_S

**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package



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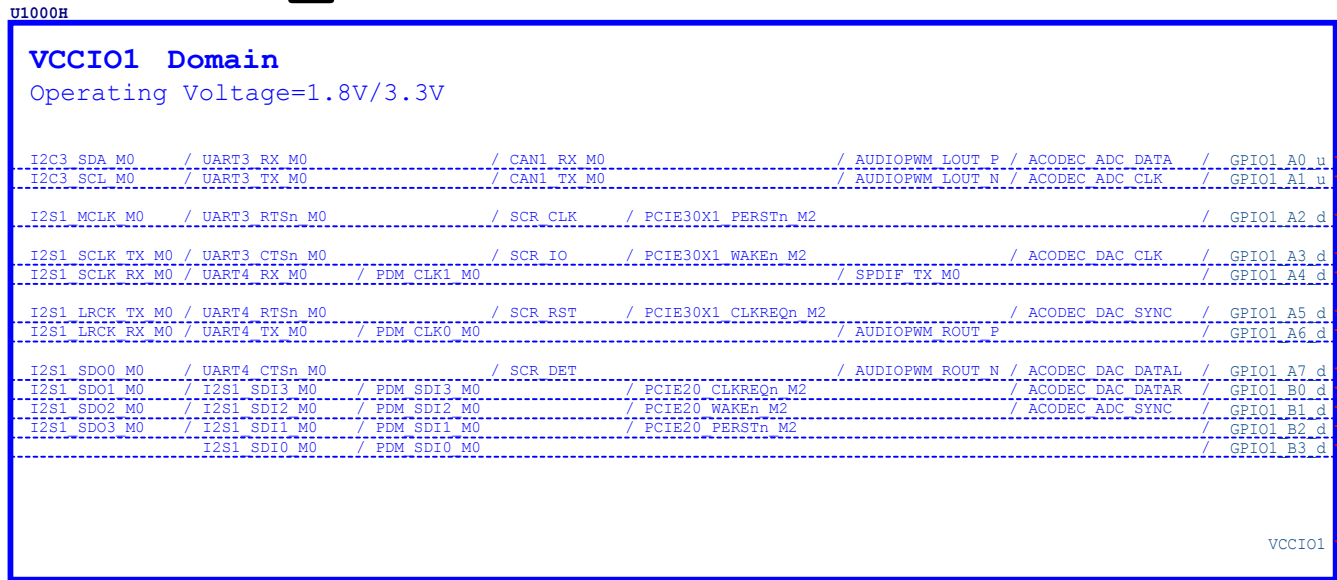
**Title: RK3568 VO Interface 2**

**File: ROC-3568-PC** REV: V1.1

Create Date: Wednesday, May 06, 2020 Page Num: 10

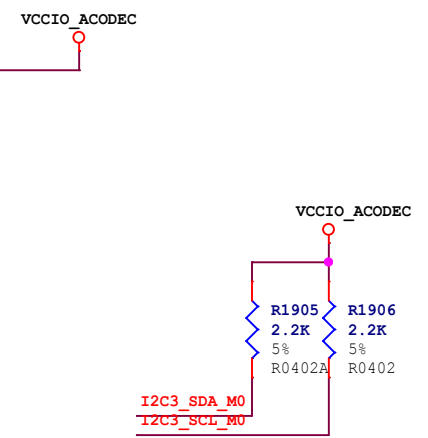
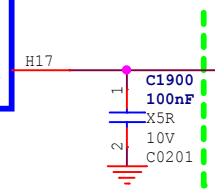
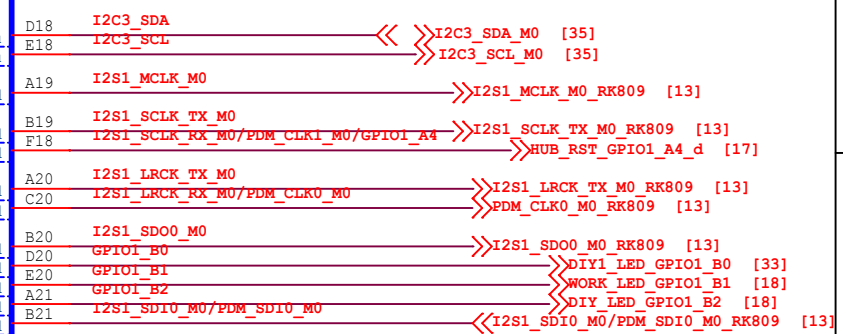
Modify Date: Tuesday, August 09, 2022 Page Total: 36

# RK3568\_H (VCCIO1 Domain)




RK3568-Socket  
BGA636\_65Rx65Rx45R3\_S

Default:RK809+PDM MIC



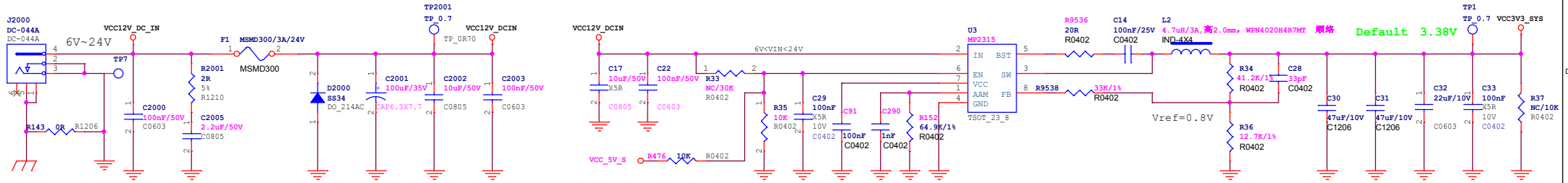
**Note:**  
Caps of between dashed green lines and U1000 should be placed under the U1000 package



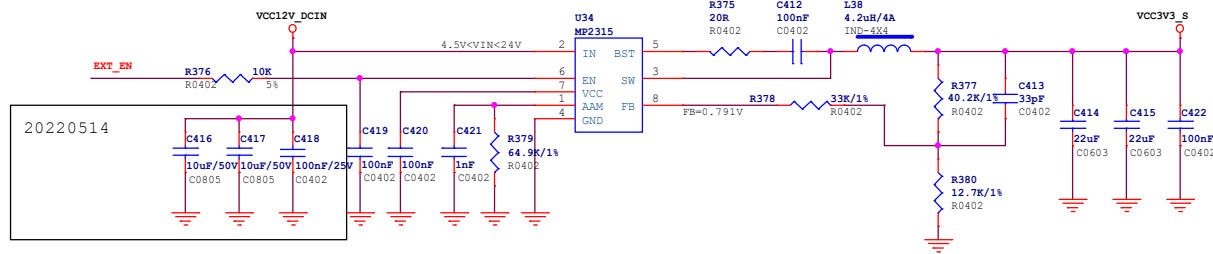
[www.t-firefly.com](http://www.t-firefly.com)

<b>Title: RK3568 Audio Interface</b>	
<b>File: ROC-3568-PC</b>	REV: V1.1
Create Date: Monday, March 30, 2020	Page Num: 11
Modify Date: Tuesday, August 09, 2022	Page Total: 36

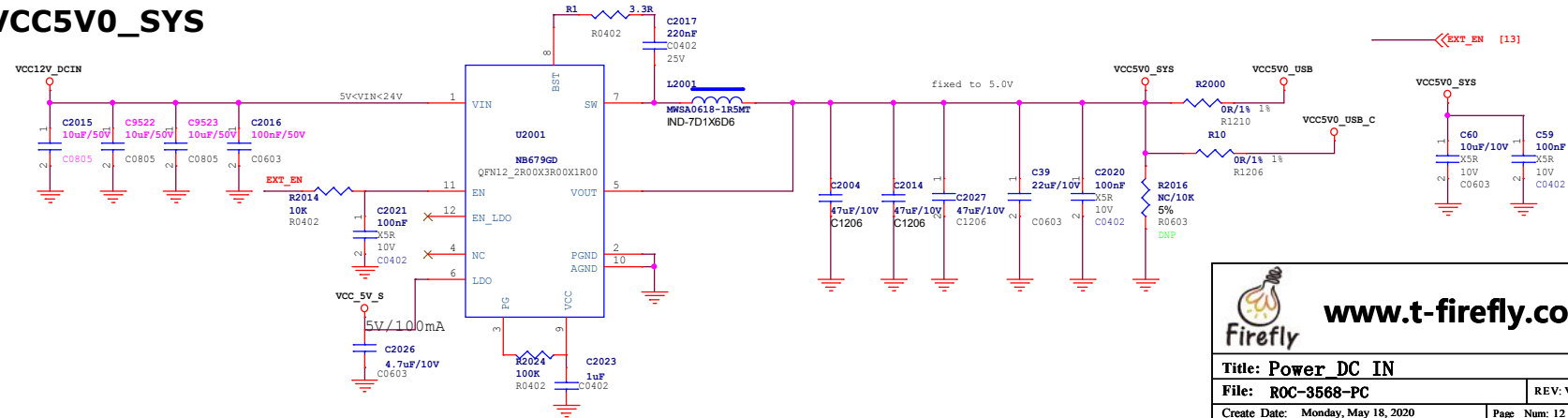
# 12V/3A DCIN




# VCC3V3\_SYS



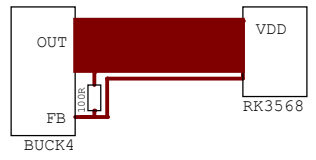
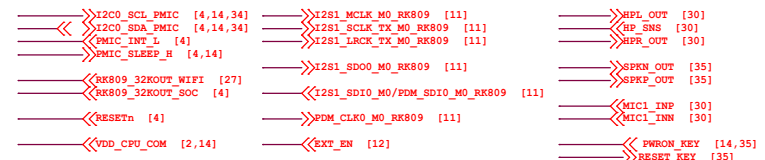
# VCC5V0\_SYS



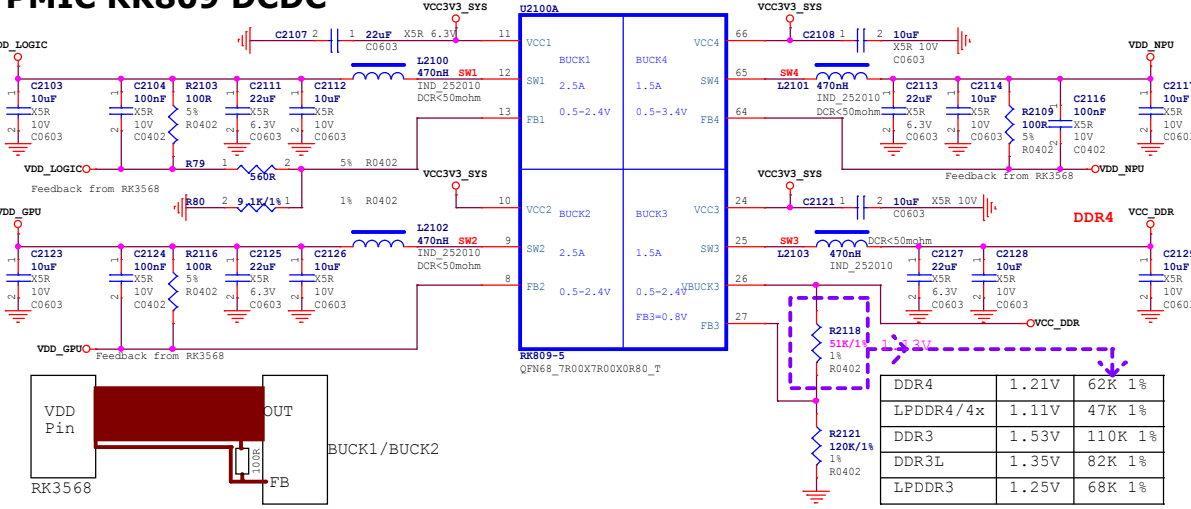


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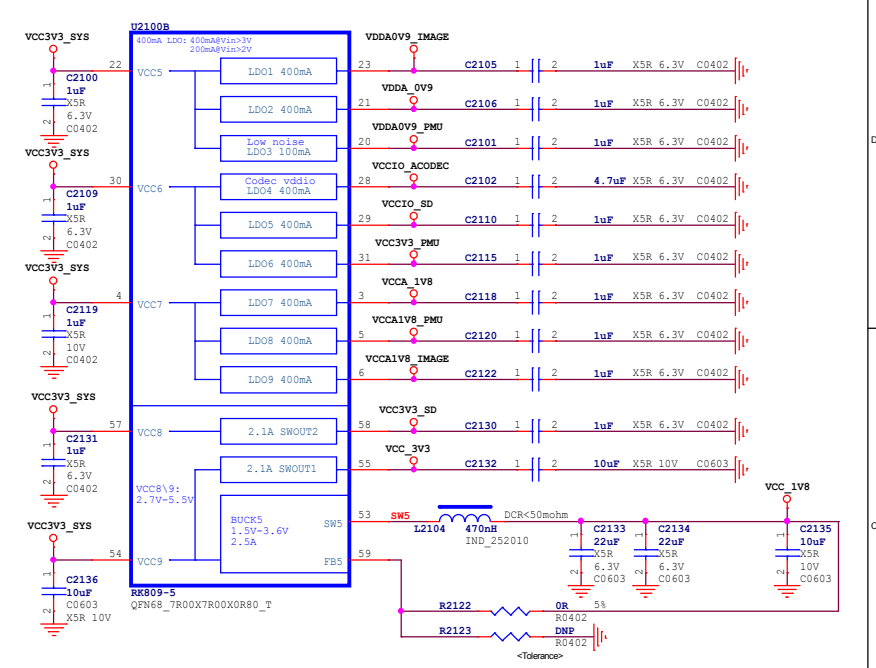
<b>Title: Power DC IN</b>		REV: V1.1
<b>File: ROC-3568-PC</b>		Page Num: 12
<b>Create Date: Monday, May 18, 2020</b>	Page Total: 36	
<b>Modify Date: Tuesday, August 09, 2022</b>		



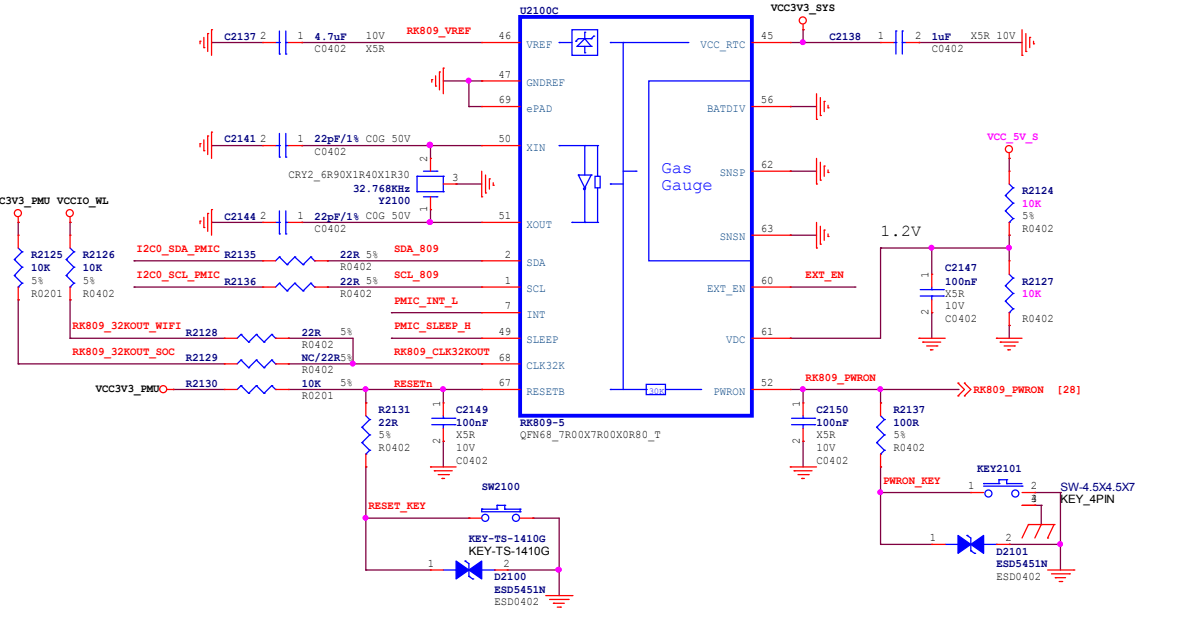
### PMIC RK809 DCDC



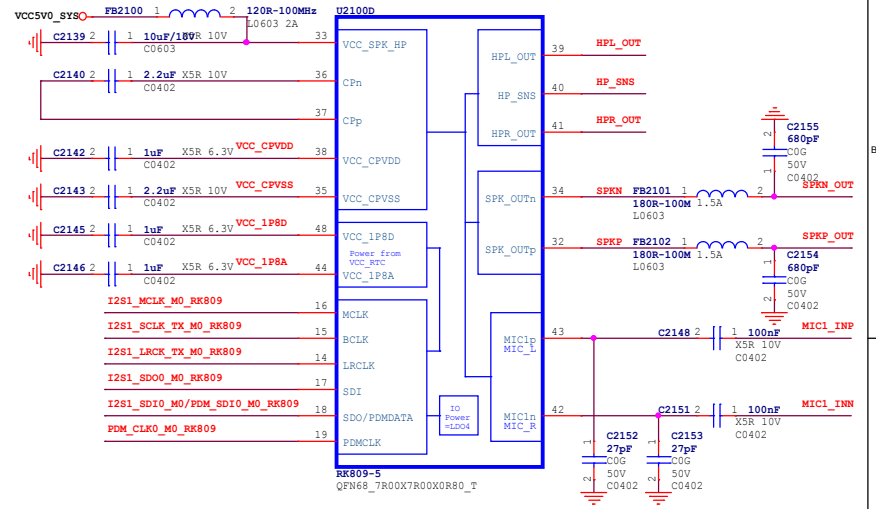
### PMIC RK809 LDO



### PMIC RK809 Management



### PMIC RK809 CODEC

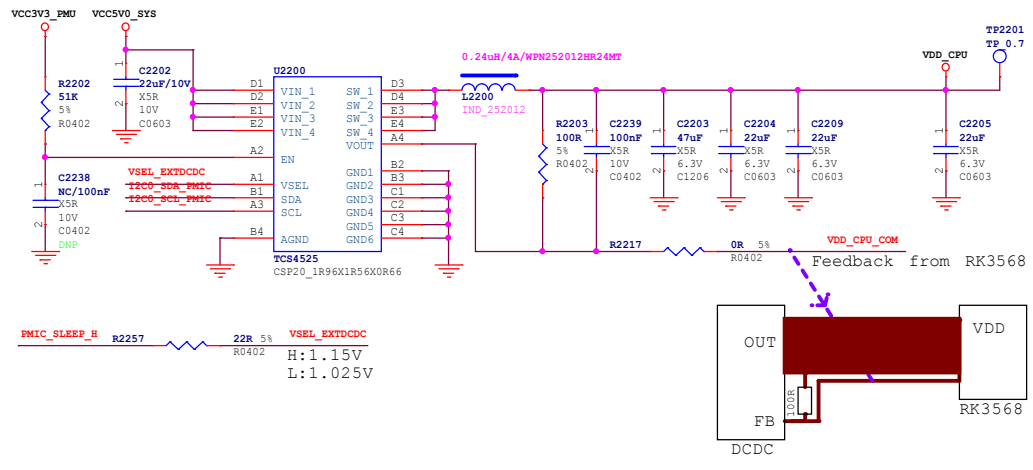


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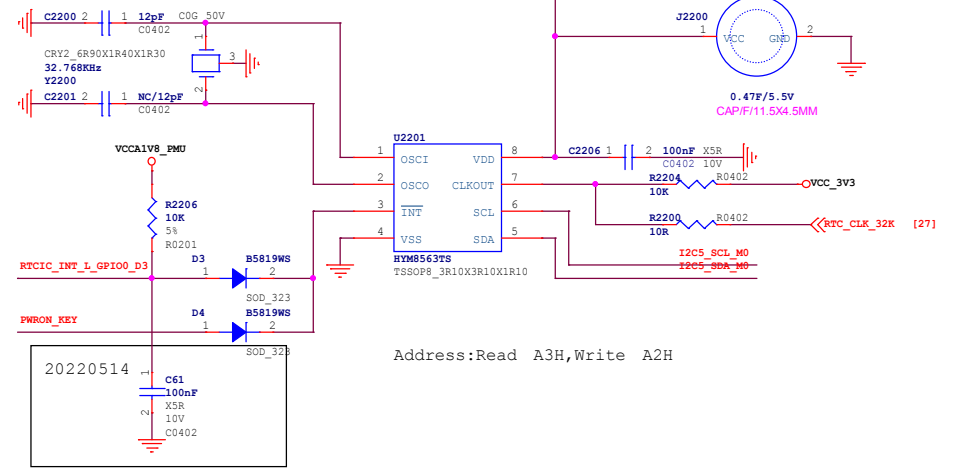
Title: Power PMIC  
 File: ROC-3568-PC  
 Create Date: Monday, May 18, 2020  
 Modify Date: Tuesday, August 09, 2022  
 Page Num: 13  
 Page Total: 36


<<PMIC\_SLEEP\_H [4,13] <<VDD\_CPU\_COM [2] <<PWRON\_KEY [13,36] <<RTCIC\_INT\_L\_GPIO0\_D3 [4] <<I2C0\_SCL\_PMIC [4,13,24] <<I2C0\_SDA\_PMIC [4,13,24] <<I2C5\_SCL\_M0 [10,32,35] <<I2C5\_SDA\_M0 [10,32,35]

# VDD\_CPU



# RTC IC

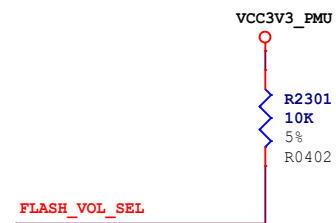
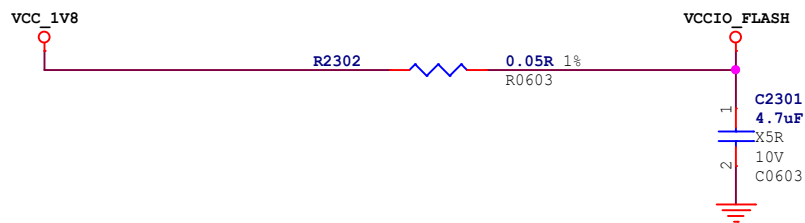



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Title: Power other		REV: V1.1
File: ROC-3568-PC		
Create Date: Monday, May 18, 2020	Page Num: 14	
Modify Date: Tuesday, August 09, 2022	Page Total: 36	

# Flash Power Manage

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)



Note:  
 FLASH VOL SEL state decided  
 to VCCIO2 domain IO driven by default  
 Logic=L:3.3V IO driven  
 Logic=H:1.8V IO driven



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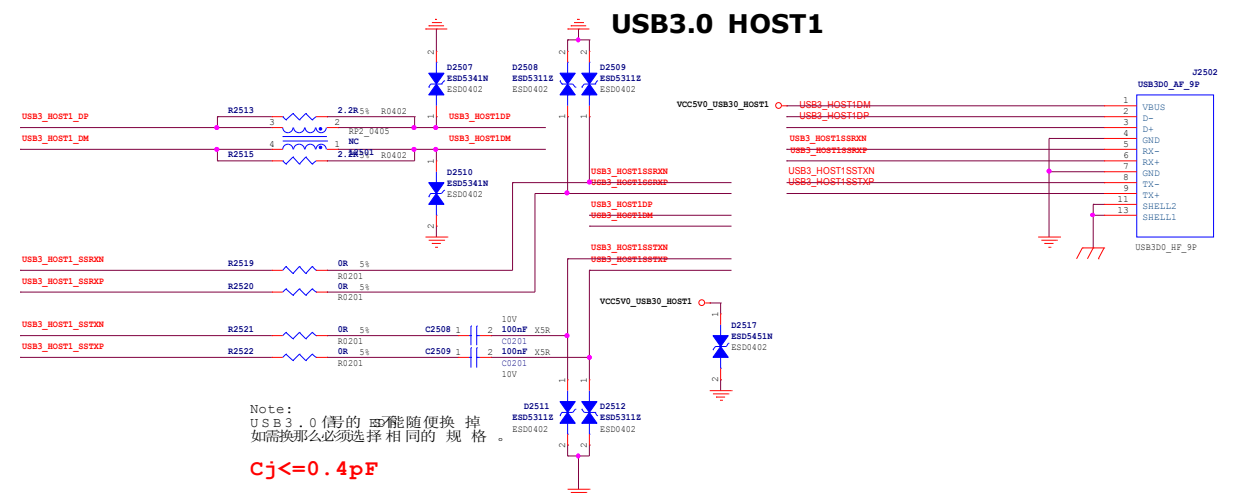
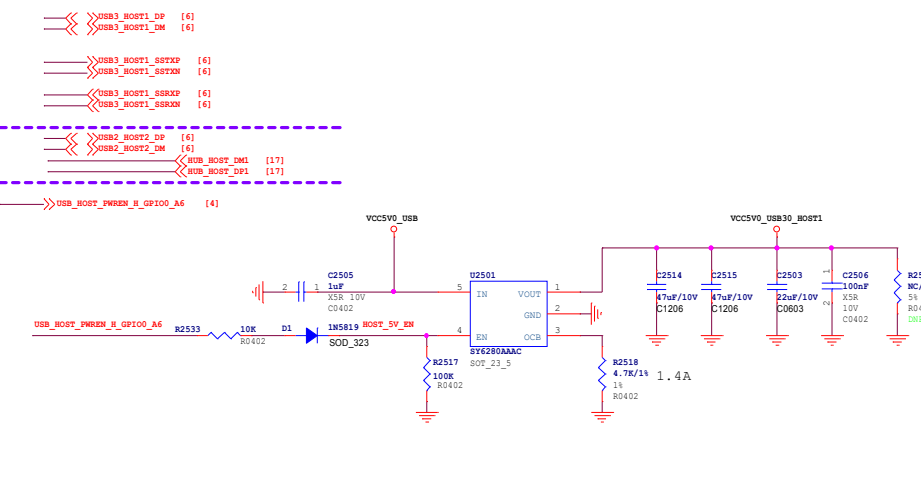
Title: Power Flash Power Manage

File: ROC-3568-PC REV: V1.1

Create Date: Tuesday, May 19, 2020 Page Num: 15

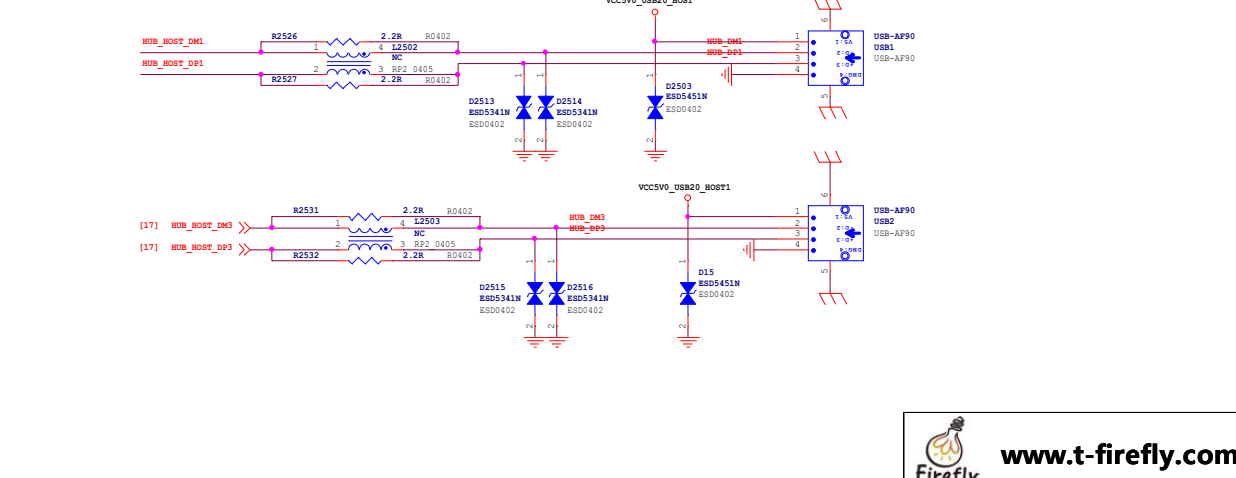
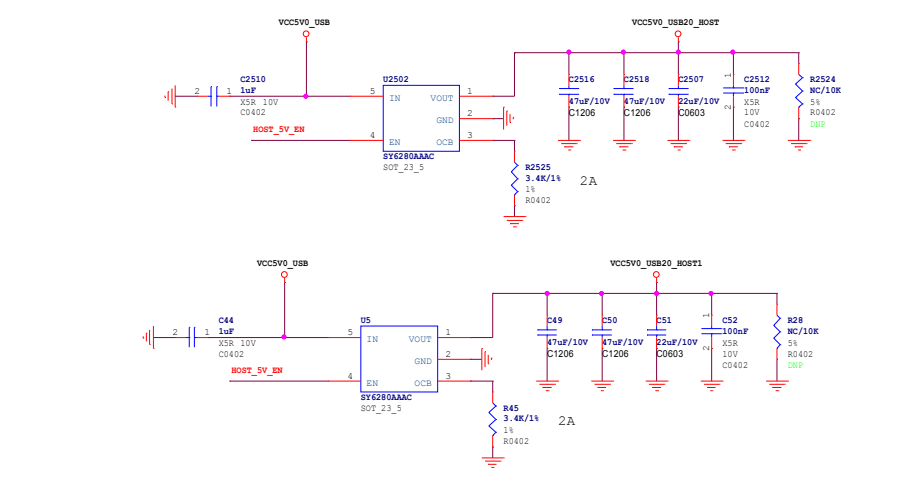
Modify Date: Tuesday, August 09, 2022 Page Total: 36






Note:  
USB3.0 信号的匹配随便换掉  
如需换那么必须选择相同的规格。  
**Cj<=0.4pF**

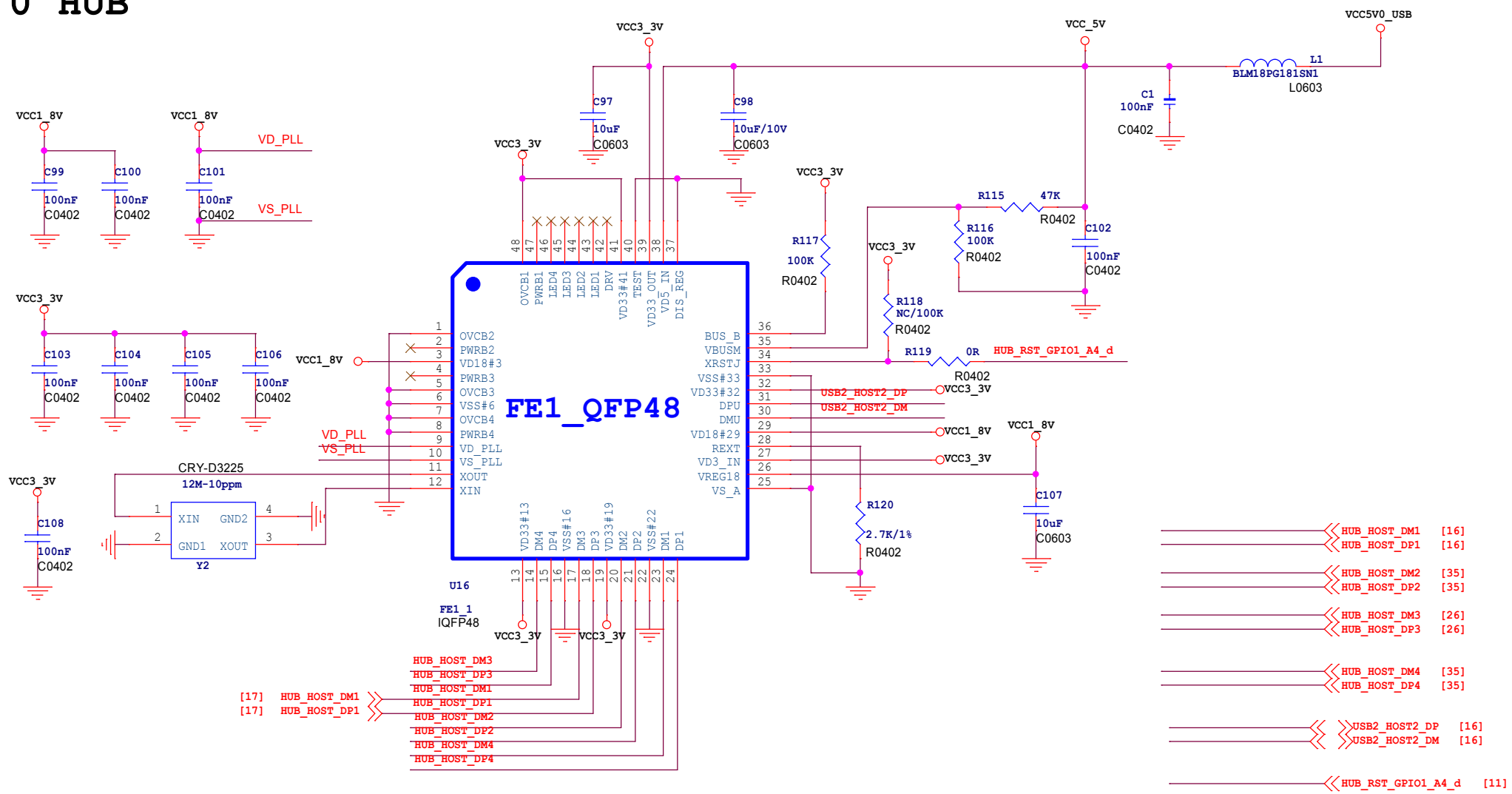
## USB2.0 HOST2 USB2.0 HOST3





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<b>Title: USB2/USB3 Port</b>		REV: V1.1
<b>File: ROC-3668-PC</b>		
Create Date: Tuesday, March 31, 2020	Page Num: 16	
Modify Date: Tuesday, August 09, 2022	Page Total: 36	

# USB2.0 HUB





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<b>Title:</b> USB2.0 HUB GL850G	
<b>File:</b> ROC-3568-PC	<b>REV:</b> V1.1
<b>Create Date:</b> Wednesday, November 04, 2020	<b>Page Num:</b> 17
<b>Modify Date:</b> Tuesday, August 09, 2022	<b>Page Total:</b> 36

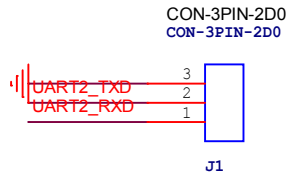
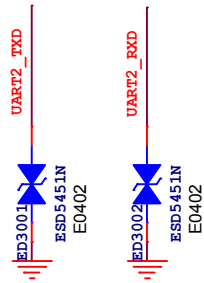
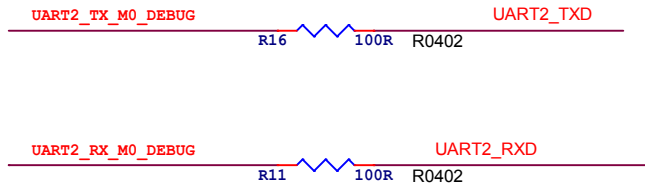
D

C

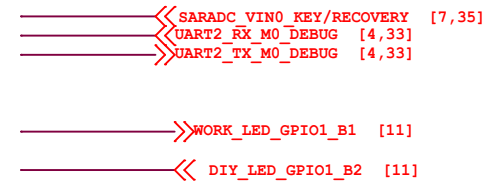
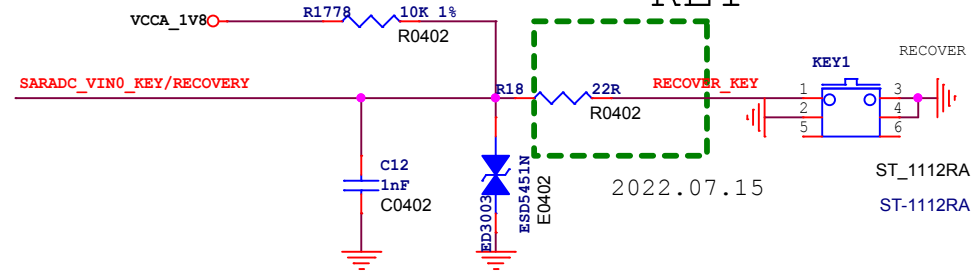
B

A

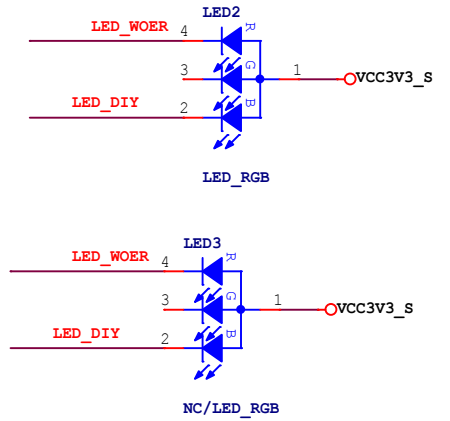
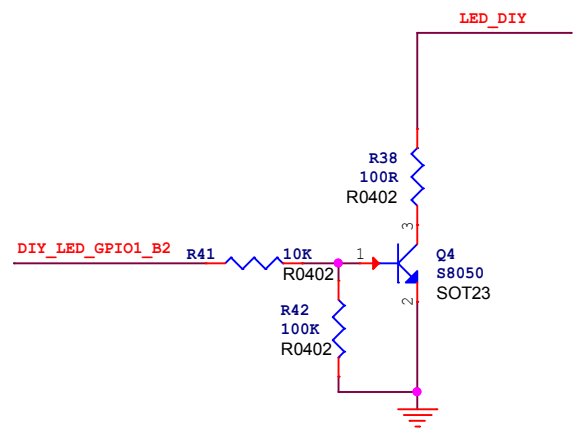
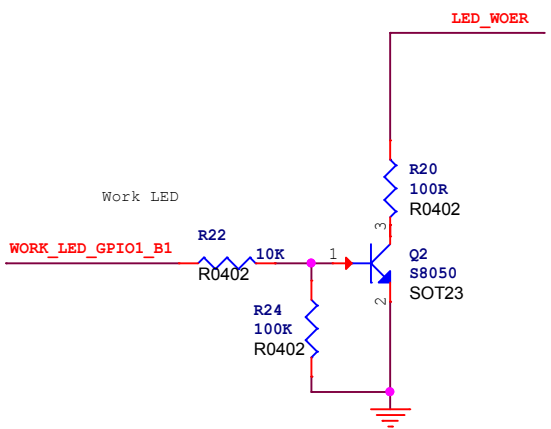
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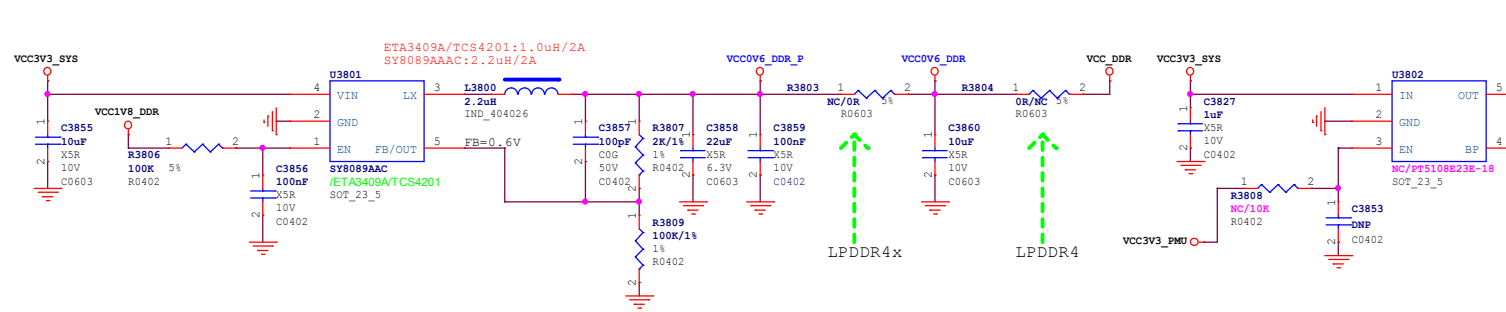
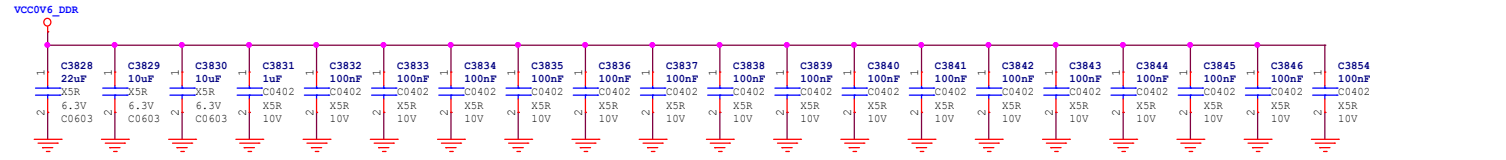
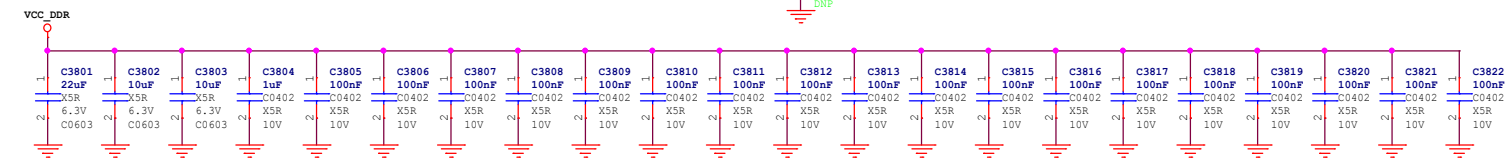
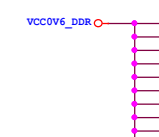
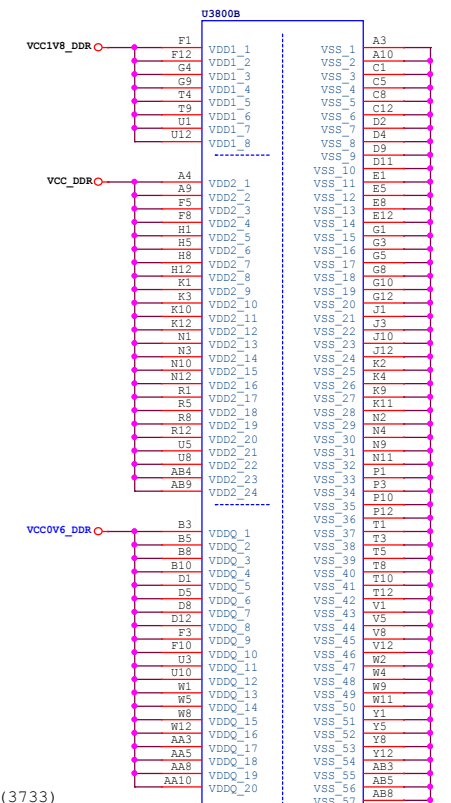
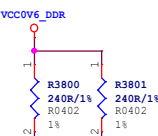
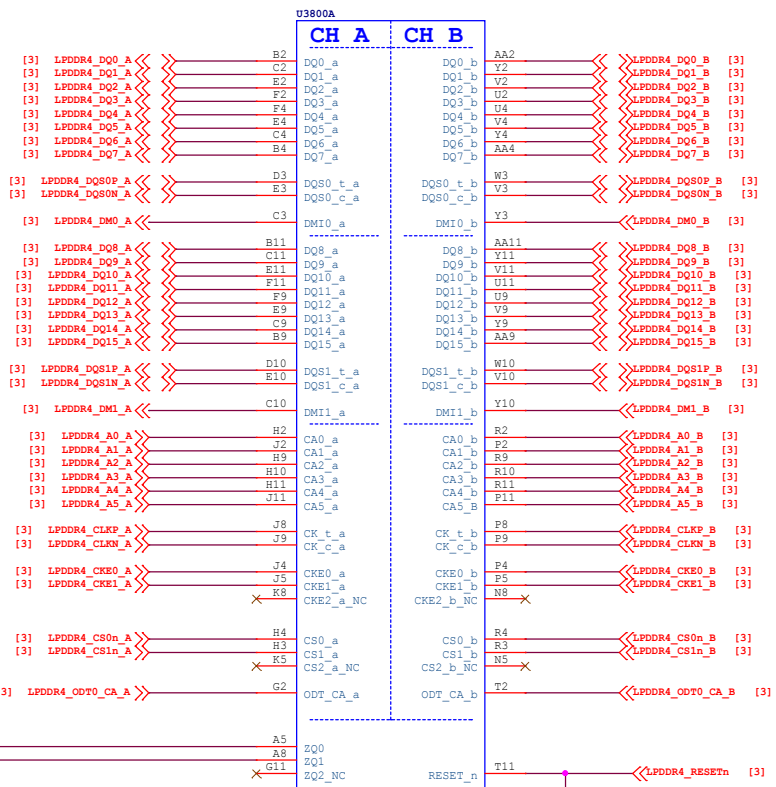
# KEY



# LED



Title: KEY/LED/DEBUG	
File: ROC-3568-PC	REV: V1.1
Create Date: Wednesday, November 04, 2020	Page Num: 18
Modify Date: Tuesday, August 09, 2022	Page Total: 36



LPDDR4: MT53D512M32D2S-053 WT:D (D9WHZ) (3733)  
 LPDDR4x: Hynix H9HCNNNBKMLHR-NME (3733)

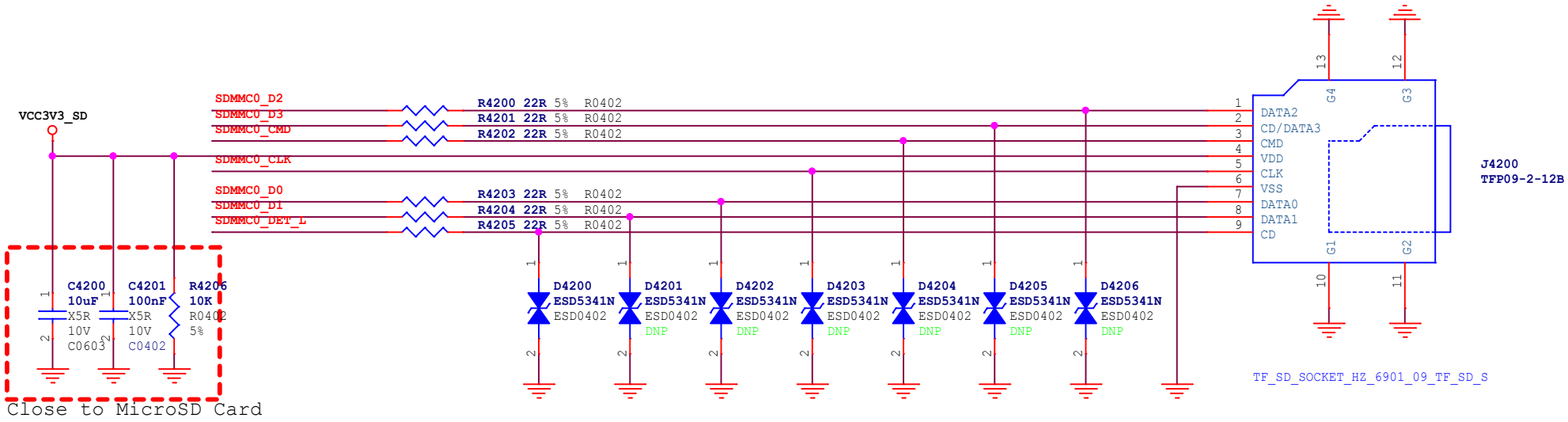
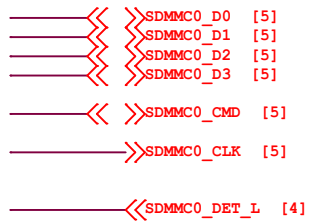
LPDDR4 200P  
 BGA200\_15R00X10R00X0R90

LPDDR4 200P  
 BGA200\_15R00X10R00X0R90

www.t-firefly.com


**Title: DRAM-LPDDR4X 1X32bit 200P**  
**File: ROC-3668-PC** REV: V1.1  
 Create Date: Thursday, January 14, 2021 Page Num: 19  
 Modify Date: Tuesday, August 09, 2022 Page Total: 36





Close to MicroSD Card

### MicroSD Card

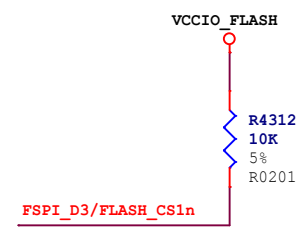
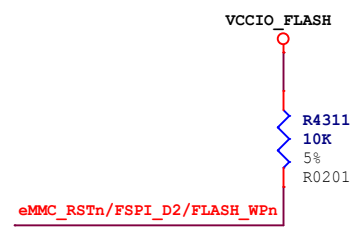
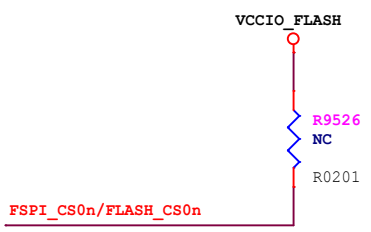
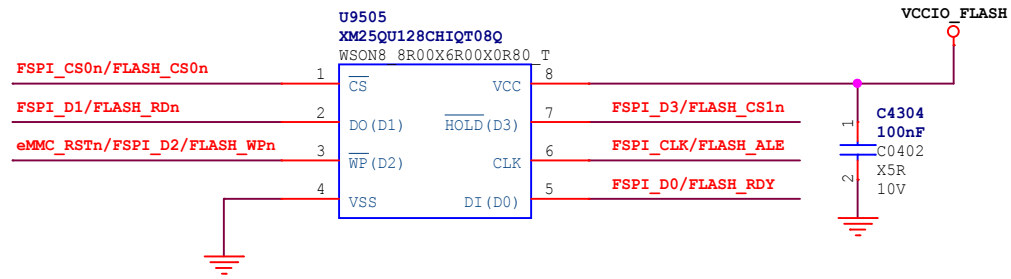



**www.t-firefly.com**

**Title: Flash-MicroSD Card**

<b>File: ROC-3568-PC</b>	REV: V1.1
Create Date: Thursday, May 07, 2020	Page Num: 21
Modify Date: Tuesday, August 09, 2022	Page Total: 36

>>FSPI\_CLK/FLASH\_ALE [5]  
 >>FSPI\_D0/FLASH\_RDY [5]  
 >>FSPI\_D1/FLASH\_RDn [5]  
 >>eMMC\_RSTn/FSPI\_D2/FLASH\_WPn [5]  
 >>FSPI\_D3/FLASH\_CS1n [5]  
 >>FSPI\_CS0n/FLASH\_CS0n [5]

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**Title: Flash-SPI FLASH**

**File: ROC-3568-PC** REV: V1.1

Create Date: Thursday, May 07, 2020 Page Num: 22

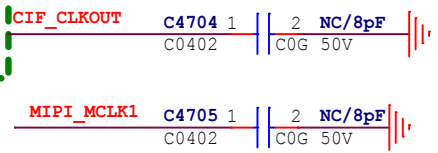
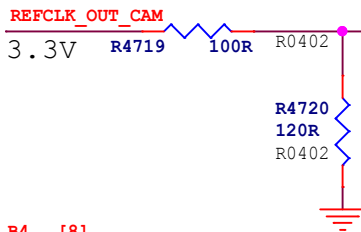
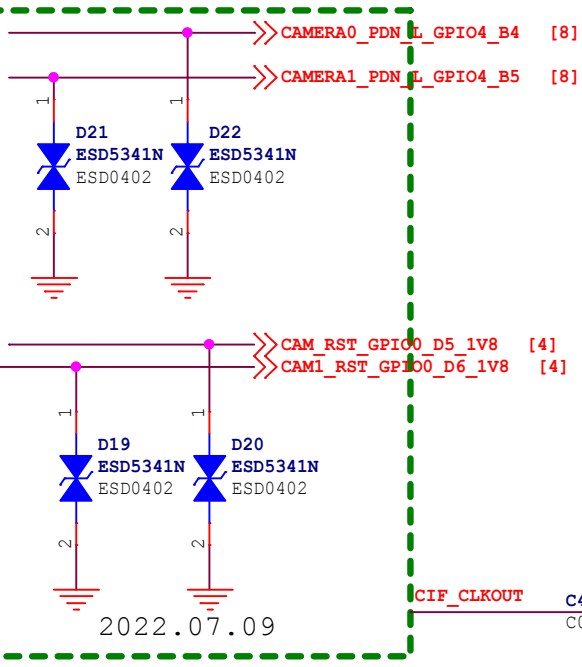
Modify Date: Tuesday, August 09, 2022 Page Total: 36



# MIPI-CSI\_RX CON

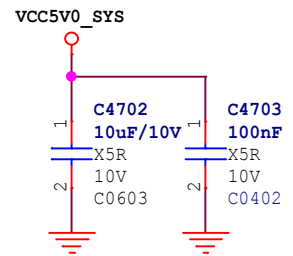
- MIPI\_CSI\_RX\_D0P [8,23]
- MIPI\_CSI\_RX\_D0N [8,23]
- MIPI\_CSI\_RX\_D1P [8,23]
- MIPI\_CSI\_RX\_D1N [8,23]
- MIPI\_CSI\_RX\_D2P [8,23]
- MIPI\_CSI\_RX\_D2N [8,23]
- MIPI\_CSI\_RX\_D3P [8,23]
- MIPI\_CSI\_RX\_D3N [8,23]
- MIPI\_CSI\_RX\_CLK0P [8,23]
- MIPI\_CSI\_RX\_CLK0N [8,23]
- MIPI\_CSI\_RX\_CLK1P [8,23]
- MIPI\_CSI\_RX\_CLK1N [8,23]

- CIF\_CLKOUT [8]
- REFCLK\_OUT\_CAM [4]
- I2C4\_SDA\_M0 [8,23]
- I2C4\_SCL\_M0 [8,23]

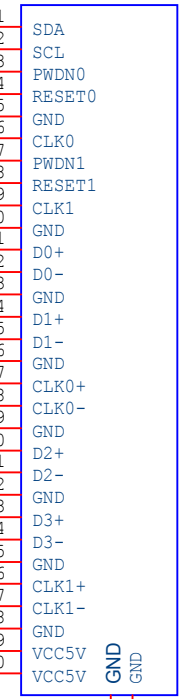



- I2C4\_SDA\_M0 [8,23]
- I2C4\_SCL\_M0 [8,23]
- SDA\_CAM0 1.8V
- SCL\_CAM0 1.8V
- CAMERA0\_PDN\_L\_GPIO4\_B4 1.8V
- MIPI\_PDNO\_CAM 1.8V
- CAM\_RST\_GPIO0\_D5\_1V8 1.8V
- MIPI\_RESETO\_CAM 1.8V
- CIF\_CLKOUT 1.8V
- MIPI\_MCLK0 1.8V
- CAMERA1\_PDN\_L\_GPIO4\_B5 1.8V
- MIPI\_PDN1\_CAM 1.8V
- CAM1\_RST\_GPIO0\_D6\_1V8 1.8V
- MIPI\_RESET1\_CAM 1.8V
- MIPI\_MCLK1 1.8V

- MIPI\_CSI\_RX\_D0P [8,23]
- MIPI\_CSI\_RX\_D0N [8,23]
- MIPI\_CSI\_RX\_D1P [8,23]
- MIPI\_CSI\_RX\_D1N [8,23]
- MIPI\_CSI\_RX\_CLK0P [8,23]
- MIPI\_CSI\_RX\_CLK0N [8,23]
- MIPI\_CSI\_RX\_D2P [8,23]
- MIPI\_CSI\_RX\_D2N [8,23]
- MIPI\_CSI\_RX\_D3P [8,23]
- MIPI\_CSI\_RX\_D3N [8,23]
- MIPI\_CSI\_RX\_CLK1P [8,23]
- MIPI\_CSI\_RX\_CLK1N [8,23]



J4701  
FPC\_30PIN\_0D5  
FPC\_30PIN\_0D5

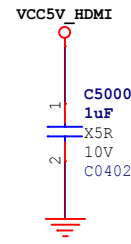
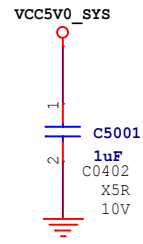




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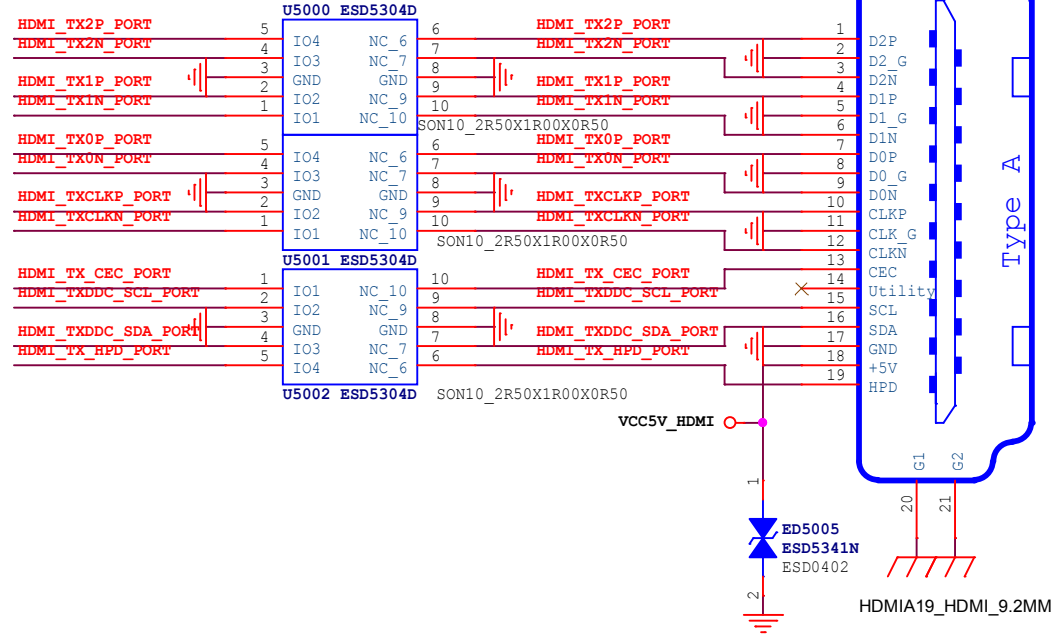
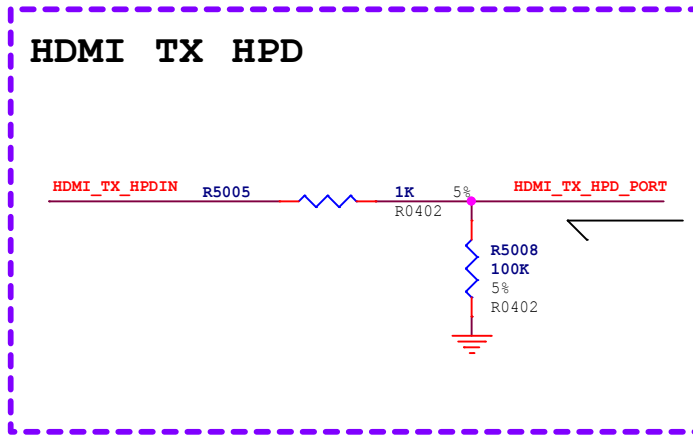
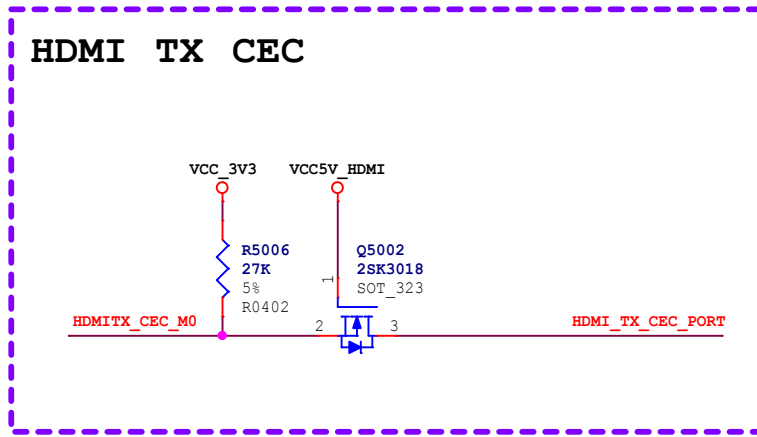
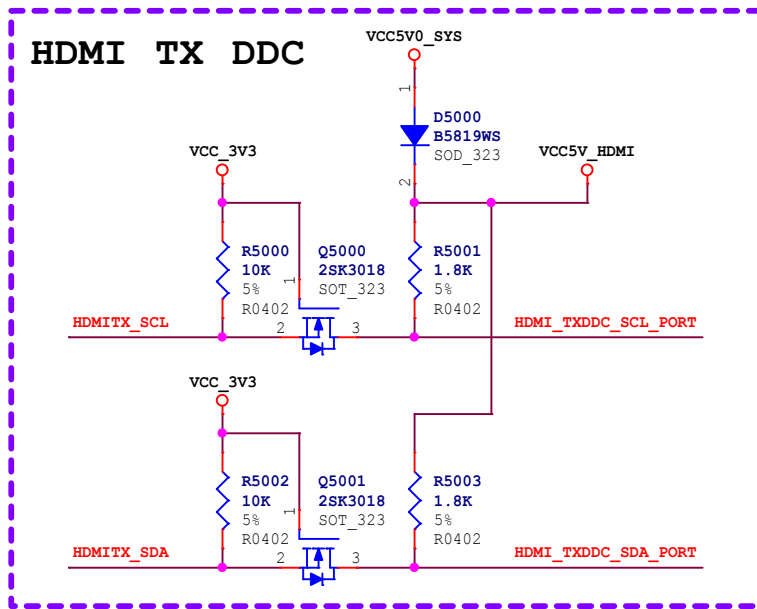

<b>Title: VI-Camera MIPI-CSI</b>	
<b>File: ROC-3568-PC</b>	<b>REV: V1.1</b>
<b>Create Date: Thursday, May 07, 2020</b>	<b>Page Num: 23</b>
<b>Modify Date: Tuesday, August 09, 2022</b>	<b>Page Total: 36</b>

- >>HDMI\_TX2P\_PORT [9]
- >>HDMI\_TX2N\_PORT [9]
- >>HDMI\_TX1P\_PORT [9]
- >>HDMI\_TX1N\_PORT [9]
- >>HDMI\_TX0P\_PORT [9]
- >>HDMI\_TX0N\_PORT [9]
- >>HDMI\_TXCLKP\_PORT [9]
- >>HDMI\_TXCLKN\_PORT [9]
- >>HDMITX\_SCL [7]
- >>HDMITX\_SDA [7]
- >>HDMITX\_CEC\_M0 [7]
- >>HDMI\_TX\_HPDIN [9]



$C_j \leq 0.4 \text{ pF}$

J7003  
HDMI\_TYPE\_A

[www.t-firefly.com](http://www.t-firefly.com)

**Title:** VO-HDMI2.0 TX

**File:** ROC-3568-PC REV: V1.1

**Create Date:** Thursday, May 07, 2020 Page Num: 24

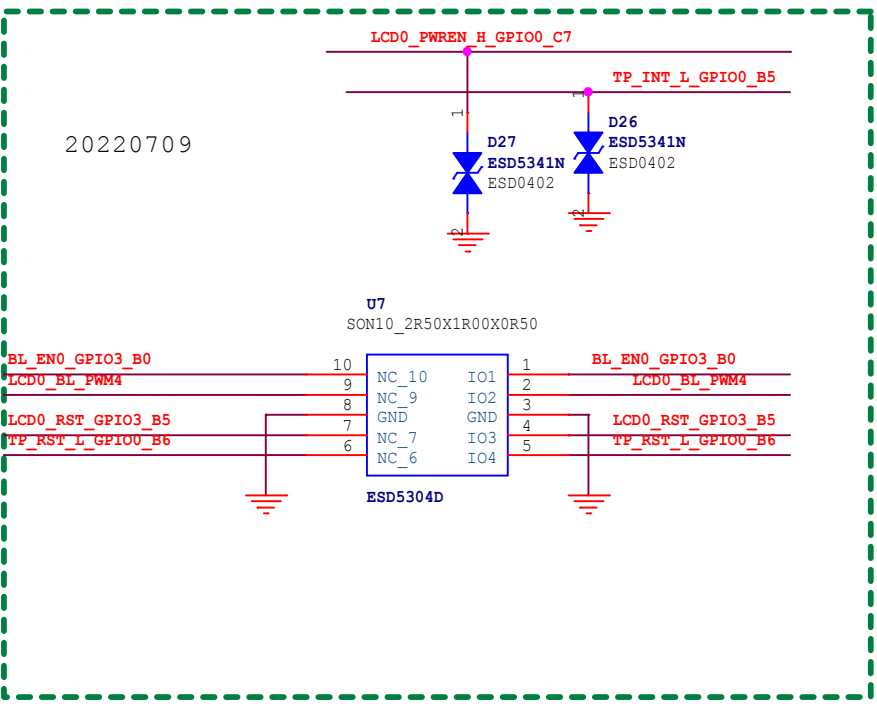
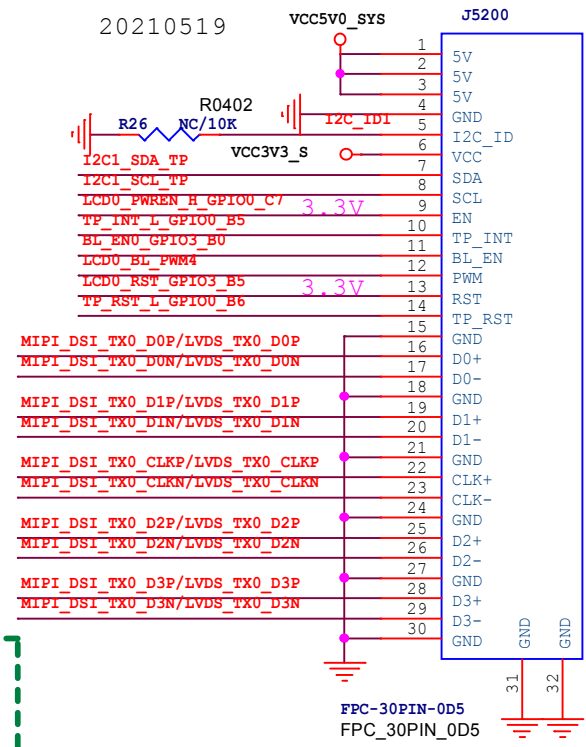
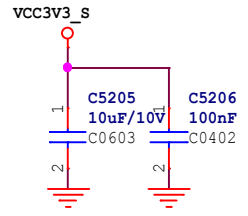
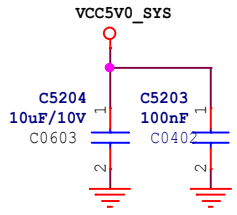
**Modify Date:** Tuesday, August 09, 2022 Page Total: 36


>>> MIPI\_DSI\_TX0\_D0P/LVDS\_TX0\_D0P [9]  
 >>> MIPI\_DSI\_TX0\_D0N/LVDS\_TX0\_D0N [9]  
 >>> MIPI\_DSI\_TX0\_D1P/LVDS\_TX0\_D1P [9]  
 >>> MIPI\_DSI\_TX0\_D1N/LVDS\_TX0\_D1N [9]  
 >>> MIPI\_DSI\_TX0\_D2P/LVDS\_TX0\_D2P [9]  
 >>> MIPI\_DSI\_TX0\_D2N/LVDS\_TX0\_D2N [9]  
 >>> MIPI\_DSI\_TX0\_D3P/LVDS\_TX0\_D3P [9]  
 >>> MIPI\_DSI\_TX0\_D3N/LVDS\_TX0\_D3N [9]  
 >>> MIPI\_DSI\_TX0\_CLKP/LVDS\_TX0\_CLKP [9]  
 >>> MIPI\_DSI\_TX0\_CLKN/LVDS\_TX0\_CLKN [9]

>>> I2C1\_SCL\_TP [4,35]  
 >>> I2C1\_SDA\_TP [4,35]  
 >>> TP\_INT\_L\_GPIO0\_B5 [4]  
 >>> TP\_RST\_L\_GPIO0\_B6 [4]  
 >>> LCD0\_BL\_PWM4 [4]  
 >>> LCD0\_PWREN\_H\_GPIO0\_C7 [4]

<<< BL\_EN0\_GPIO3\_B0 [10]  
 <<< LCD0\_RST\_GPIO3\_B5 [10]

<<< SARADC\_VIN2\_LCD\_ID [7]  
 SARADC\_VIN2\_LCD\_ID R5202 OR R0402 I2C\_ID1

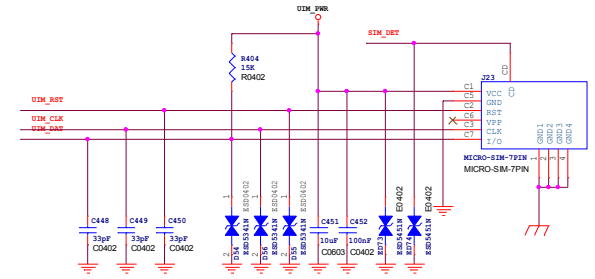
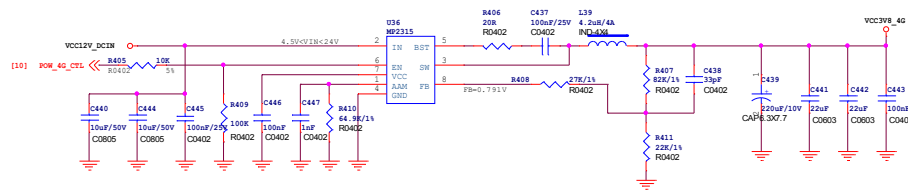




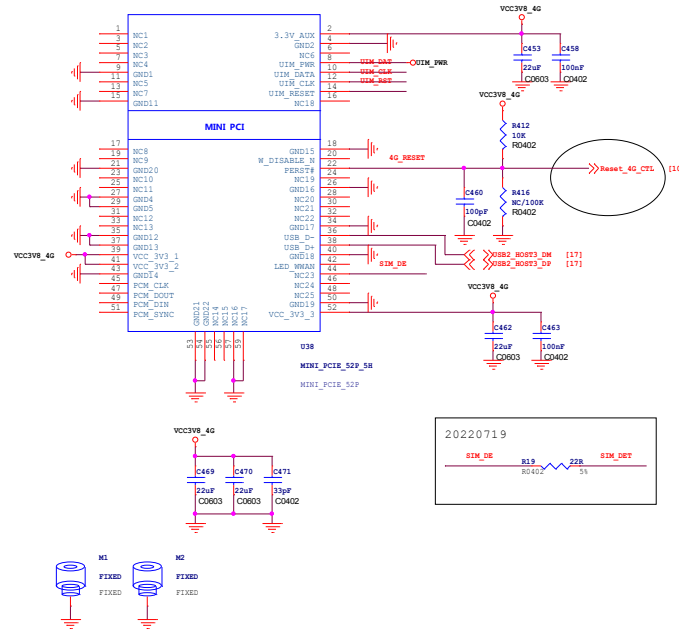
**www.t-firefly.com**

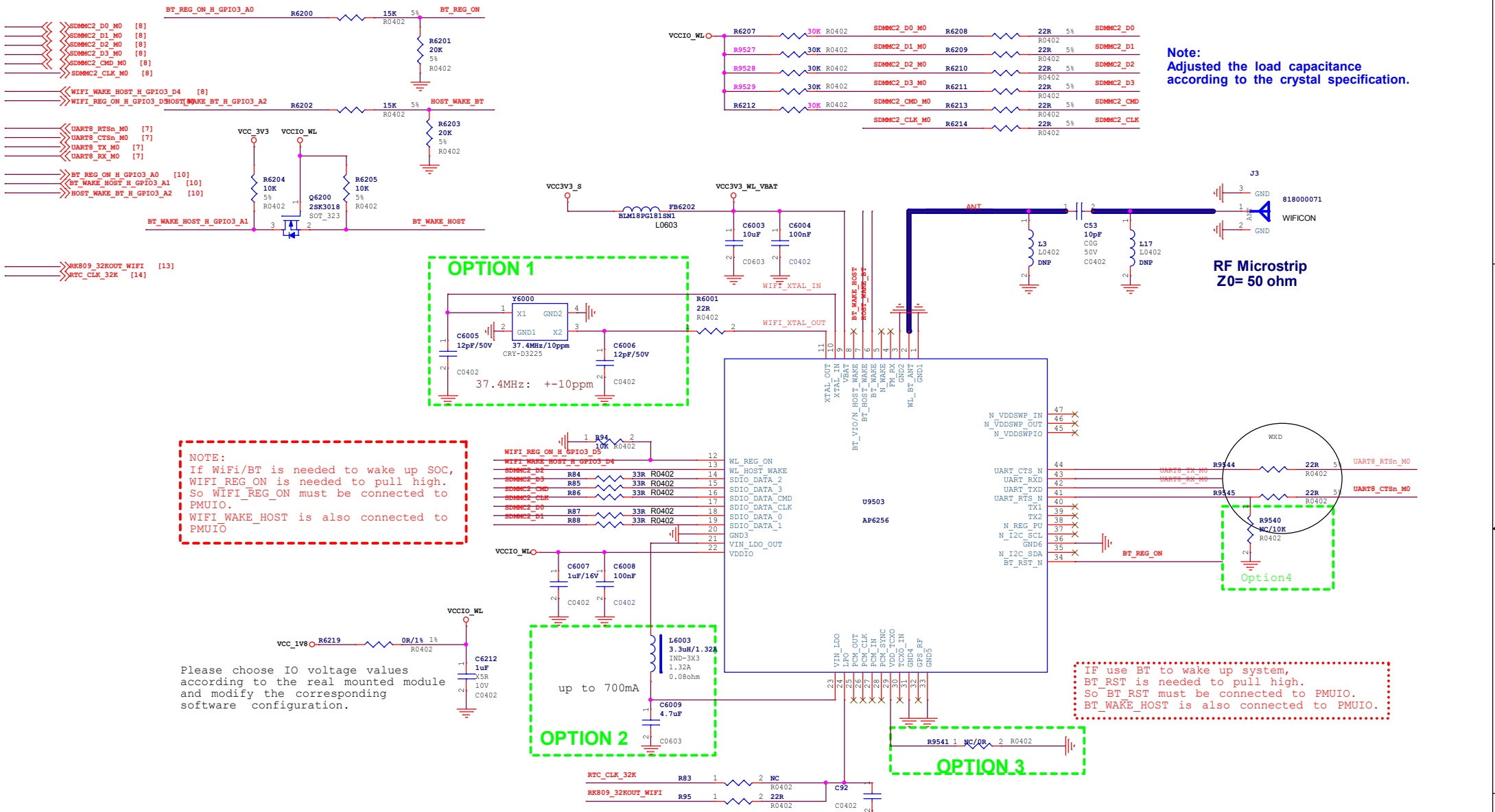
<b>Title: VO-LCM MIPI-DSI TX0/LVDS TX0</b>	
<b>File: ROC-3568-PC</b>	<b>REV: V1.1</b>
Create Date: Tuesday, May 19, 2020	Page Num: 25
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# 4G/5G SIM CARD



# MINI PCIE-4G





Note:  
Adjusted the load capacitance according to the crystal specification.


RF Microstrip  
Z0= 50 ohm

**NOTE:**  
If WiFi/BT is needed to wake up SOC, WiFi\_REG\_ON is needed to pull high. So WiFi\_REG\_ON must be connected to PMUIO.  
WiFi\_WAKE\_HOST is also connected to PMUIO

Please choose IO voltage values according to the real mounted module and modify the corresponding software configuration.

If use BT to wake up system, BT\_RST is needed to pull high. So BT\_RST must be connected to PMUIO.  
BT\_WAKE\_HOST is also connected to PMUIO.

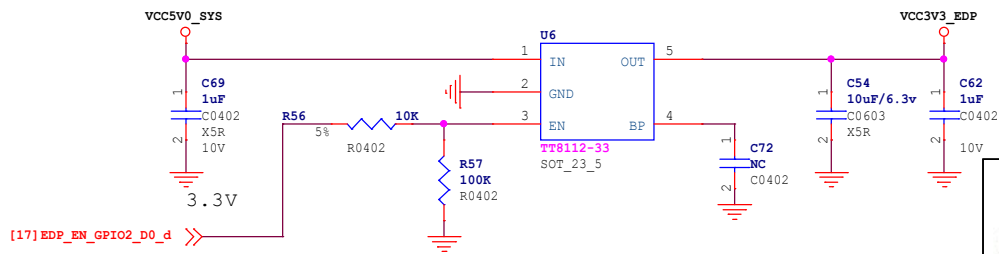
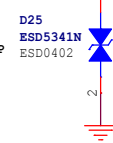
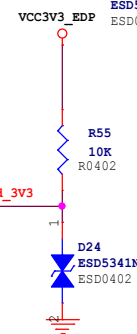
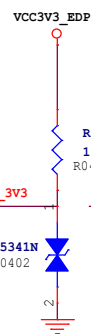
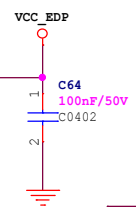
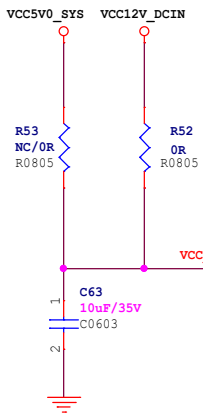
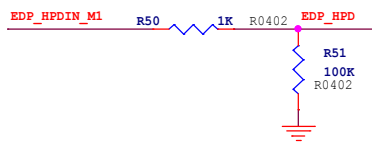
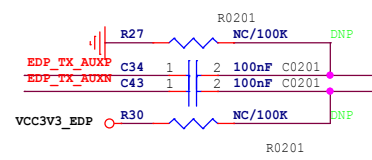
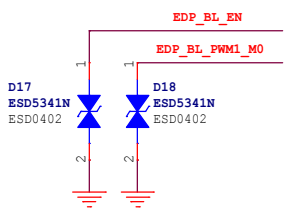
OPTION	WIFI				BT	Crystals	VCCIO_SDIO	OPTION1	OPTION2	OPTION3	OPTION4
	a	b/g/n	ac	5Ghz							
AP6236/AP6212	No	Yes	No	No	4.2/4.0	26MHz	1.71-3.63V	Yes	Yes	No	No
AP6256/AP6255	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.62-3.63V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	No
RTL8189FTV Module F89FTSM12-W3	No	Yes	No	No	No	Module Integrated	1.8-3.3V	No	No	No	No
RTL8723DS Module 6223A-SRD	No	Yes	No	No	4.2	Module Integrated	1.62-3.63V	No	No	No	Yes
QCA9377 Module 8223A-SR	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	No
RTL8821CS Module 6221A-SRC	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	No


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**Title: WIFI/BT-SDIO 2T2R + UART**  
**File: ROC-3568-PC**
REV: V1.1

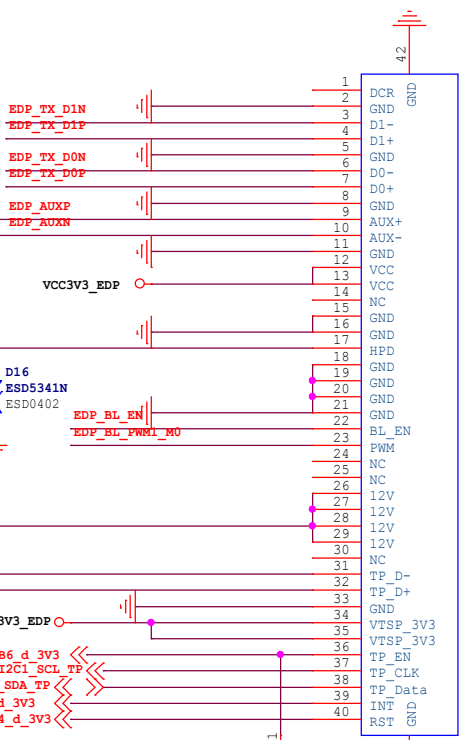
Create Date: Tuesday, June 23, 2020 Page Num: 27  
 Modify Date: Tuesday, August 09, 2022 Page Total: 36

EDP\_TX\_D0P  
 EDP\_TX\_D0N  
 EDP\_TX\_D1P  
 EDP\_TX\_D1N  
 EDP\_TX\_D2P  
 EDP\_TX\_D2N  
 EDP\_TX\_D3P  
 EDP\_TX\_D3N  
 EDP\_TX\_AUXP  
 EDP\_TX\_AUXN  
 EDP\_HPDIN\_M1  
 EDP\_BL\_PWM1\_M0  
 EDP\_BL\_EN



[17] EDP\_EN\_GPIO2\_D0\_d

[17] HUB\_HOST\_DM4  
 [17] HUB\_HOST\_DP4  
 VCC3V3\_EDP  
 [31] TP\_EN/GPIO3\_B6\_d\_3V3  
 [4,25] I2C1\_SCL TP  
 [4,25] I2C1\_SDA TP  
 [31] TP\_INT/GPIO2\_D7\_d\_3V3  
 [31] TP\_RST/GPIO3\_A4\_d\_3V3



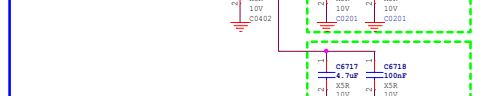
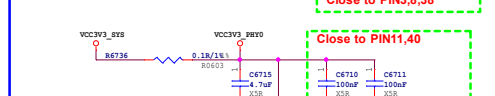
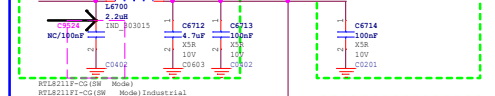
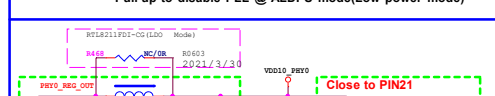
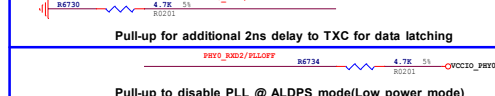
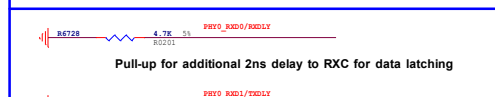
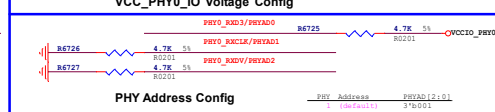
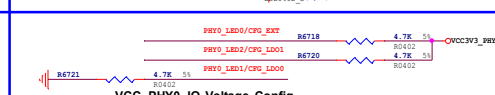
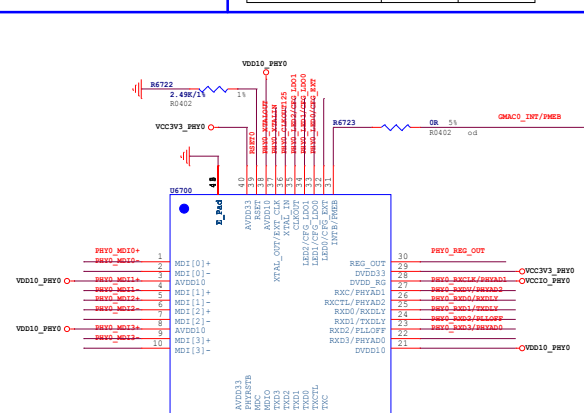
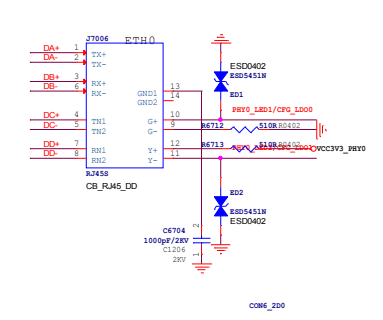
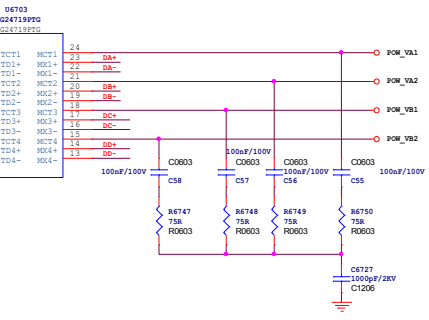
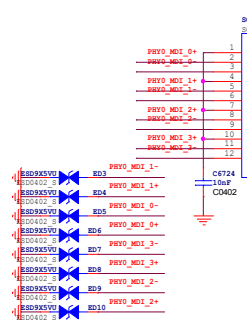
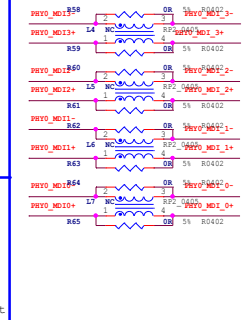
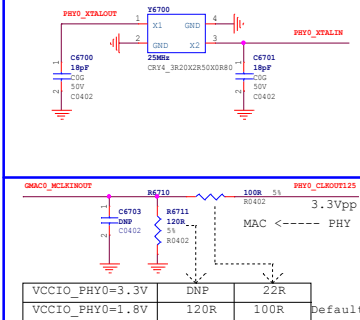
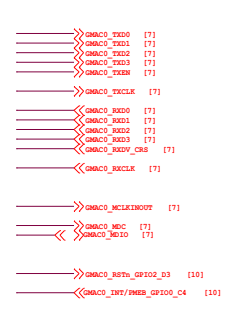
J7

FPC\_40\_0D5\_A  
 FPC\_40\_0D5\_A

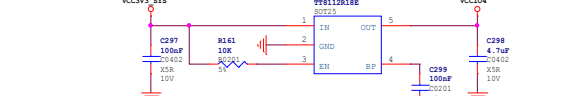
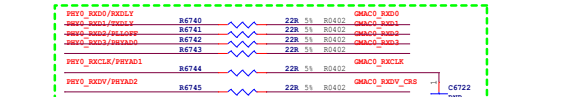
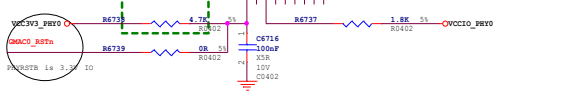
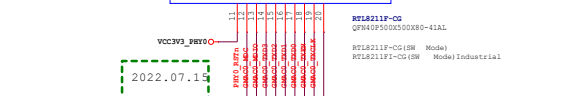
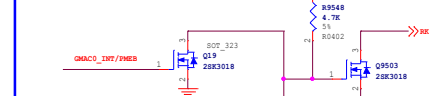
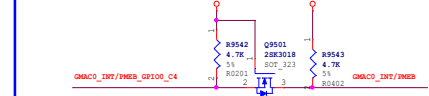
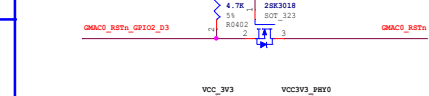
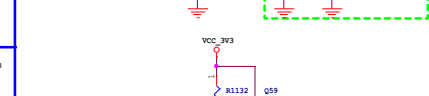
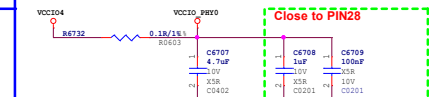
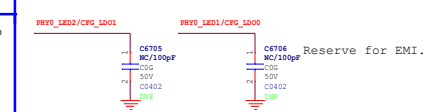


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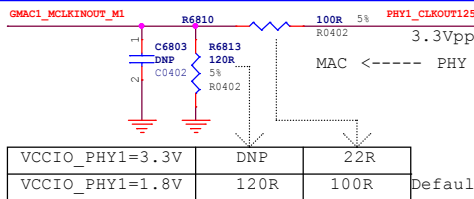
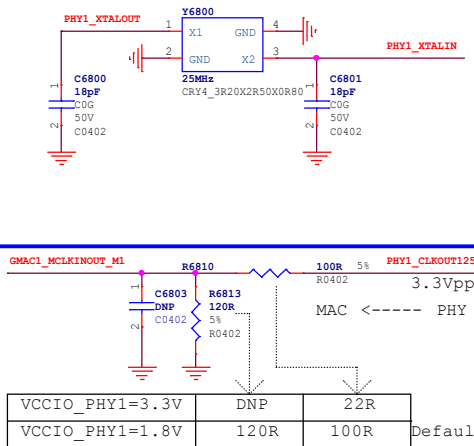
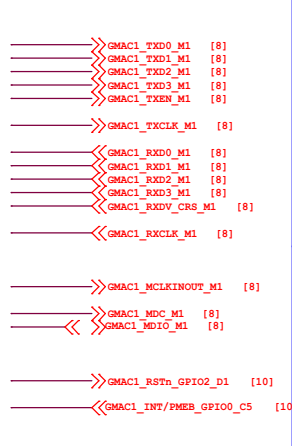
Title: VO-LCM eDP		REV: V1.1
File: ROC-3568-PC		
Create Date: Friday, July 08, 2022	Page Num: 27	
Modify Date: Tuesday, August 09, 2022	Page Total: 36	



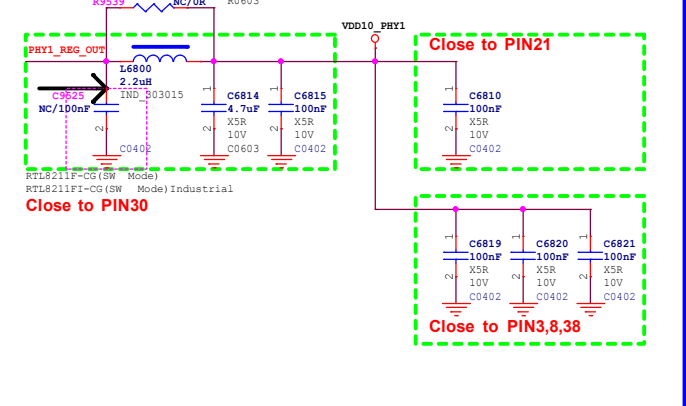
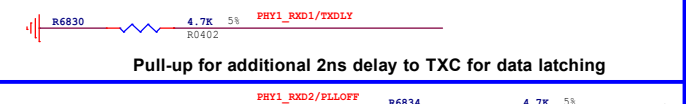
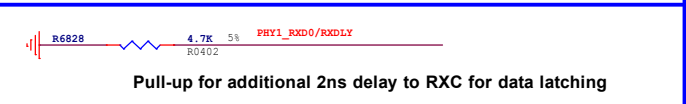
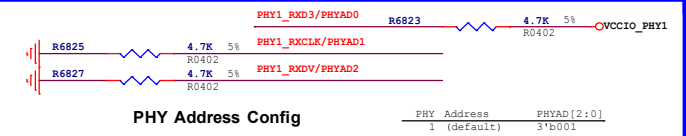
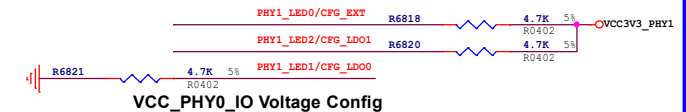
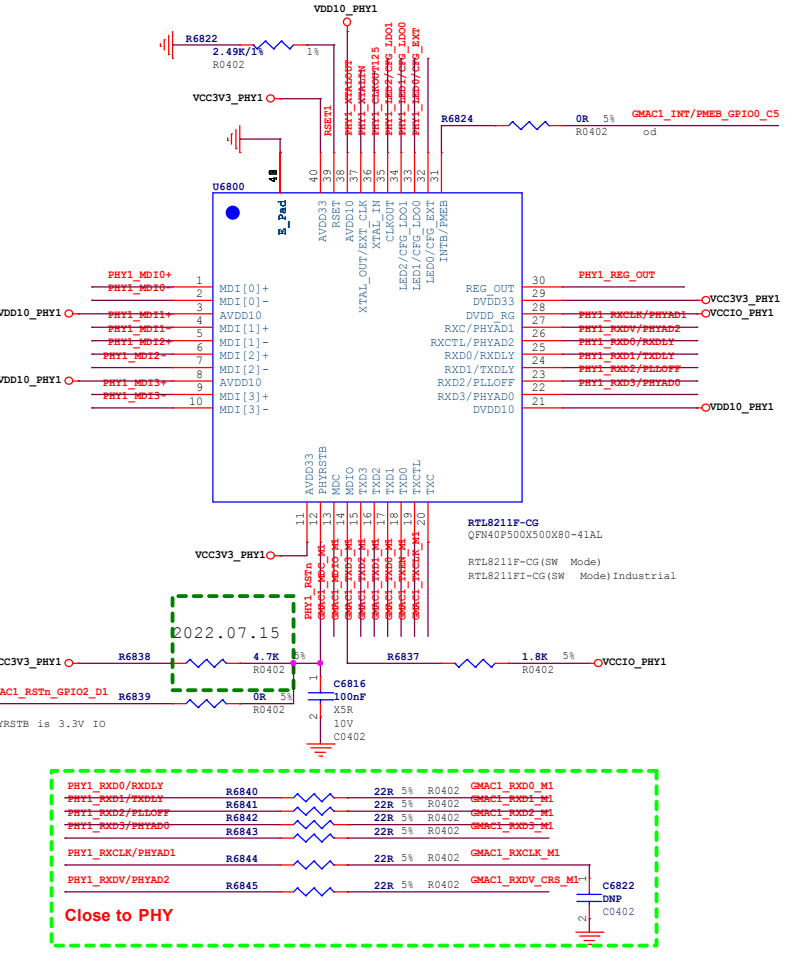
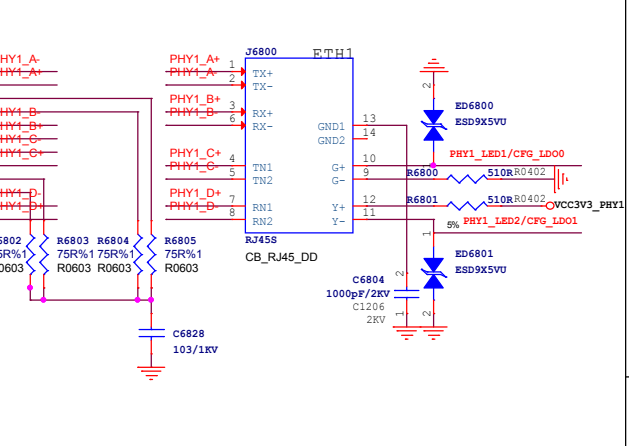
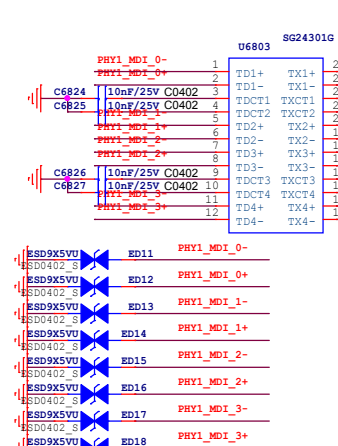
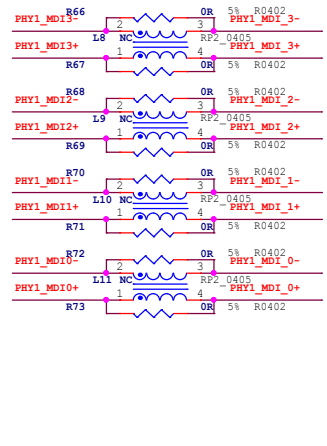
SRM1 Power Source	CPD_BXT	CPD_LED1(L1S)
External 3.3V	1*1b	2*1b0
Internal 3.0V (MCP1802)	1*1b0	2*1b0
Internal 1.8V	1*1b0	2*1b10



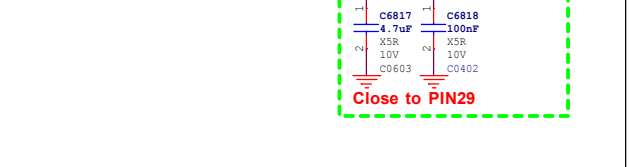
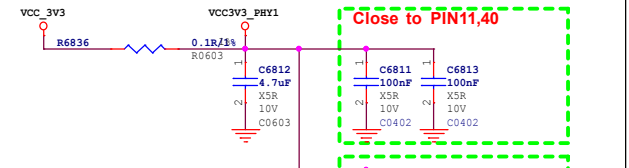
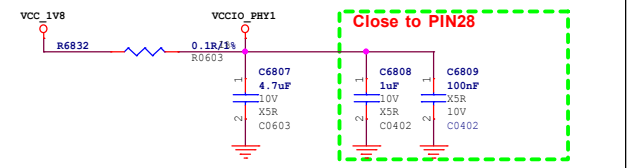
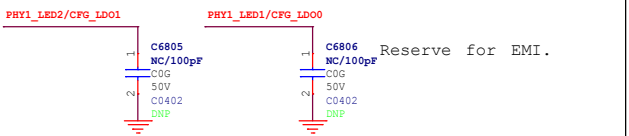





VCCIO_PHY1=3.3V	DNP	22R	Default
VCCIO_PHY1=1.8V	120R	100R	



RGMI1 Power Source	CFG EXT	CFG LDO[1:0]
External 3.3V	1'b1	2'b00
External 1.8V (default)	1'b1	2'b10
Internal 1.8V	1'b0	2'b10




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**Title: Ethernet-GEPHY RGMI11**  
**File: ROC-3568-PC**

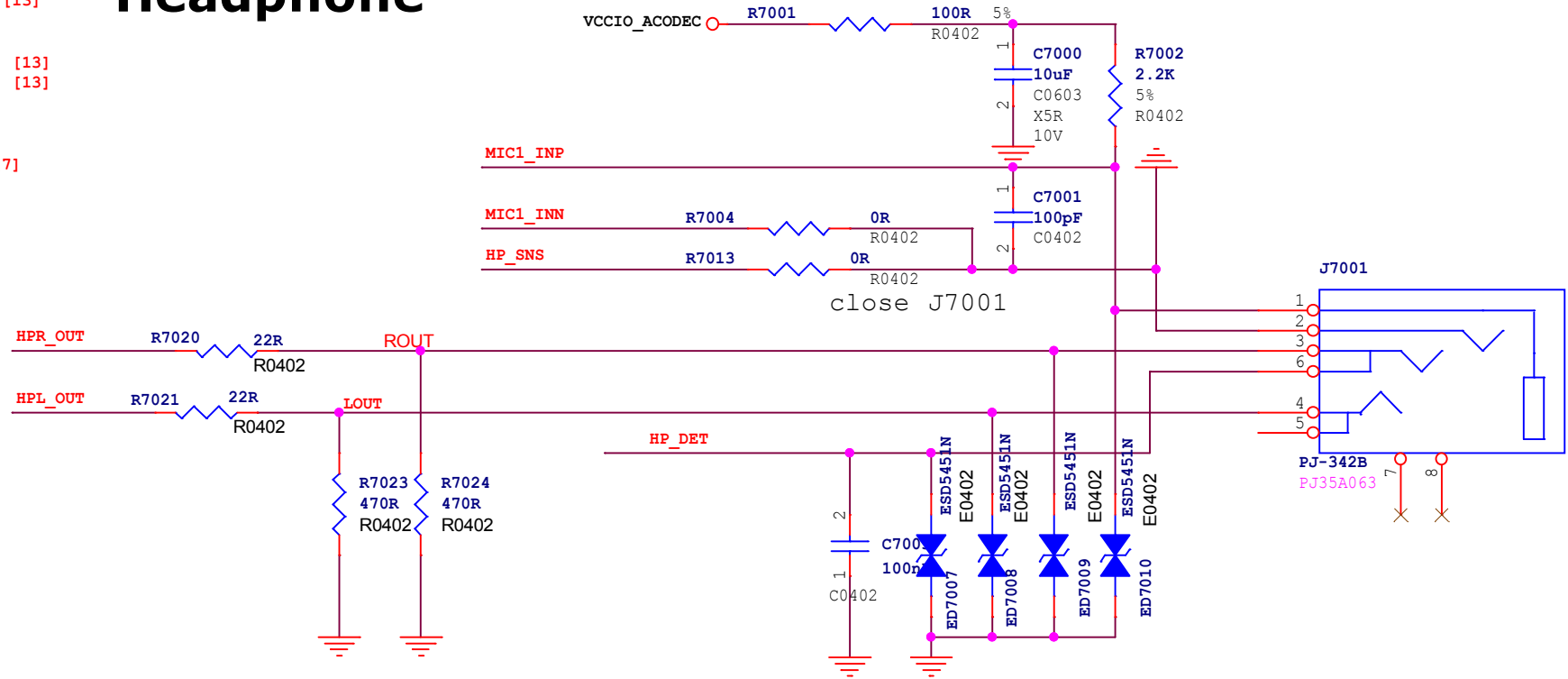
Create Date: Tuesday, May 19, 2020 Modify Date: Tuesday, August 09, 2022	Page Num: 29 Page Total: 36
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# Headphone

HPL\_OUT [13]  
HP\_SNS [13]  
HPR\_OUT [13]

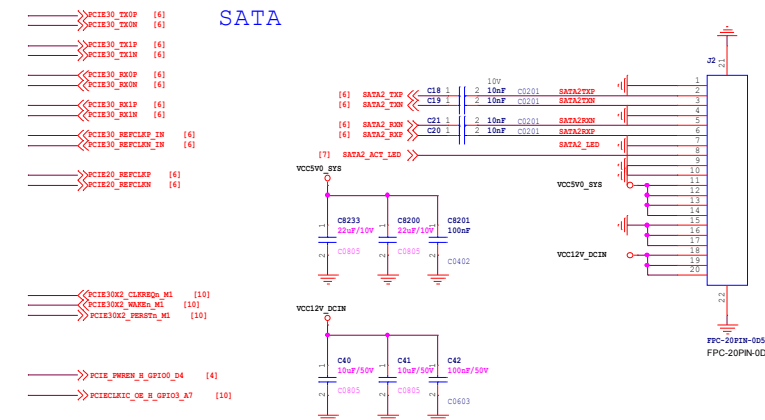
MIC1\_INP [13]  
MIC1\_INN [13]

HP\_DET [7]

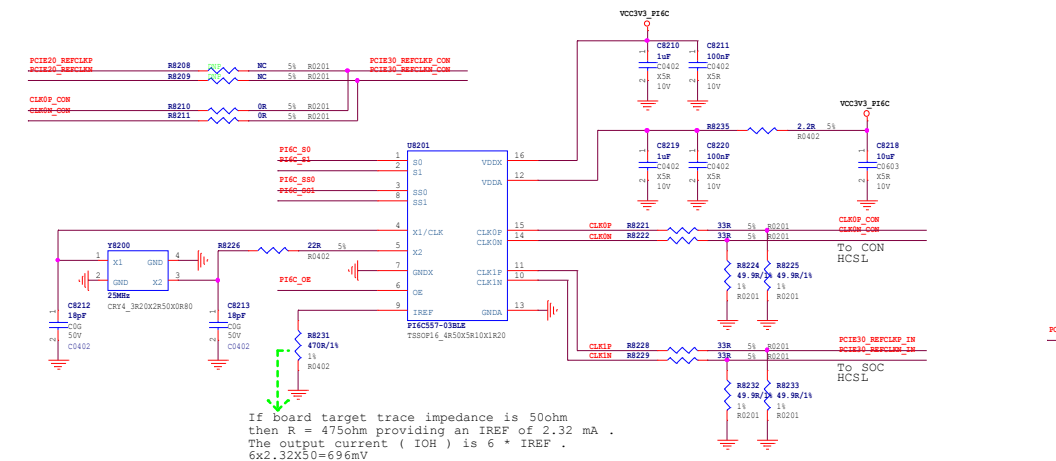
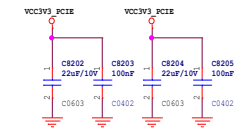
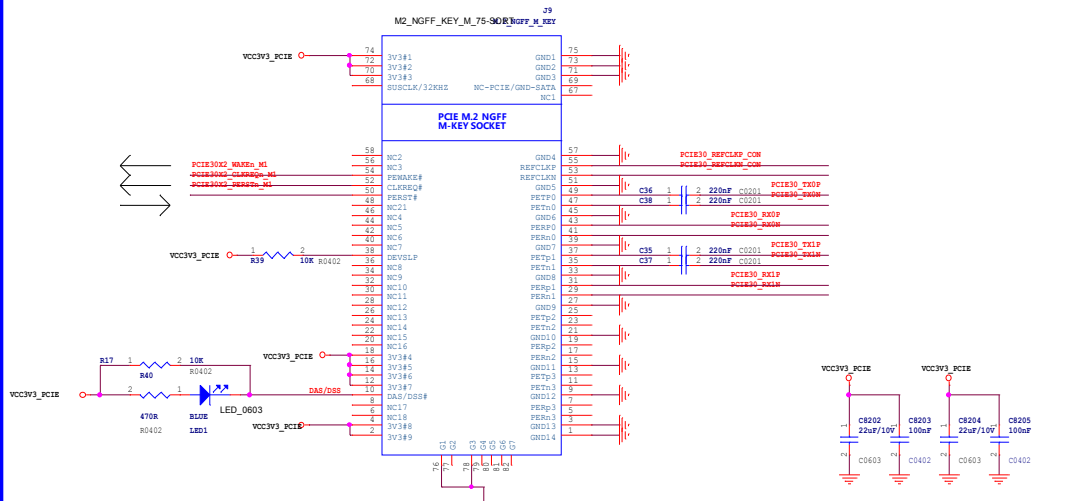


<b>Title:</b> Audio Port	
<b>File:</b> ROC-3568-PC	<b>REV:</b> V1.1
<b>Create Date:</b> Tuesday, May 19, 2020	<b>Page Num:</b> 30
<b>Modify Date:</b> Tuesday, August 09, 2022	<b>Page Total:</b> 36

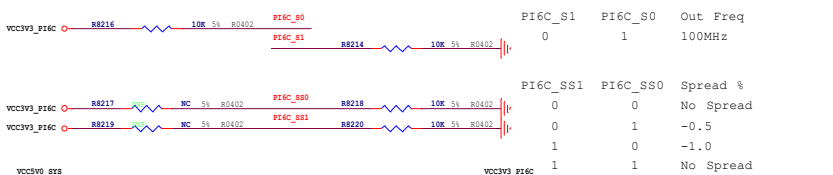
### SATA



### PCIe3.0 x 2Lanes (X 4Slot)



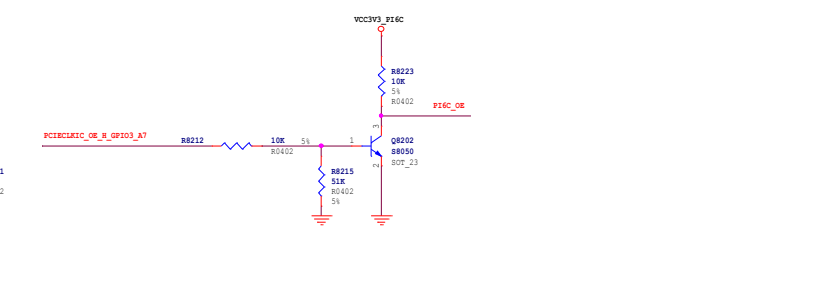
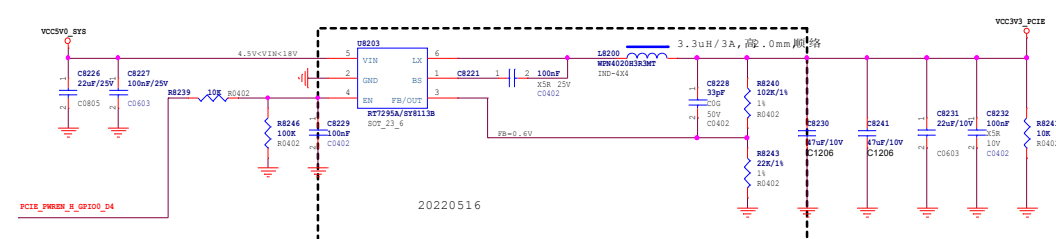
If board target trace impedance is 50ohm  
 when R = 475ohm providing an IREF of 2.32 mA .  
 The output current ( IOH ) is 6 \* IREF .  
 6x2.32x50=696mV



PI6C_S1	PI6C_S0	Out Freq
0	1	100MHz

PI6C_SS1	PI6C_SS0	Spread %
0	0	No Spread
0	1	-0.5
1	0	-1.0
1	1	No Spread



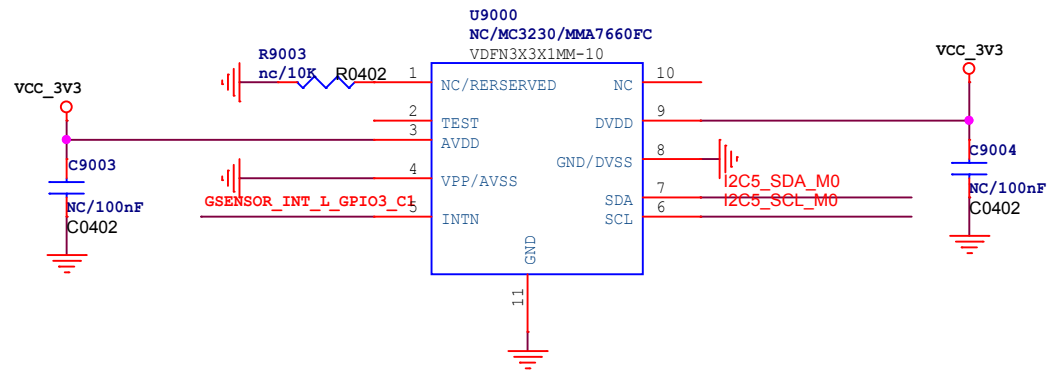
**Firefly** [www.t-firefly.com](http://www.t-firefly.com)

**Title: PCIe-PCIe3.0 Slot/SATA**  
**File: ROC-3568-PC**  
 Create Date: Thursday, May 07, 2020  
 Modify Date: Tuesday, August 09, 2022

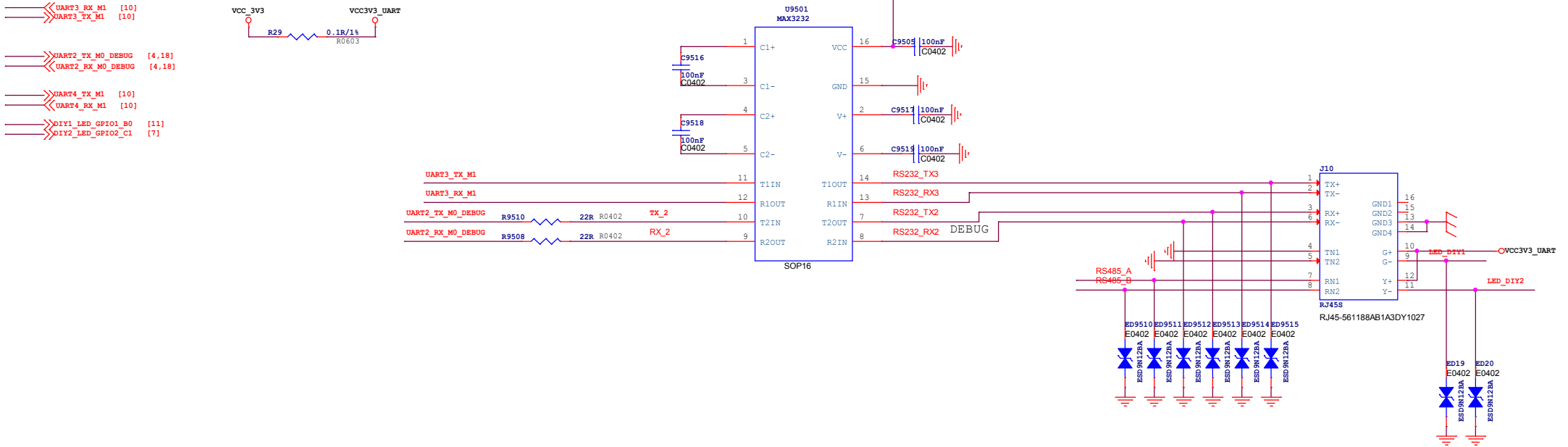
Page Num: 31  
 Page Total: 36

I2C5\_SCL\_M0 [10,14,35]  
 I2C5\_SDA\_M0 [10,14,35]  
 GSENSOR\_INT\_L\_GPIO3\_C1 [10]

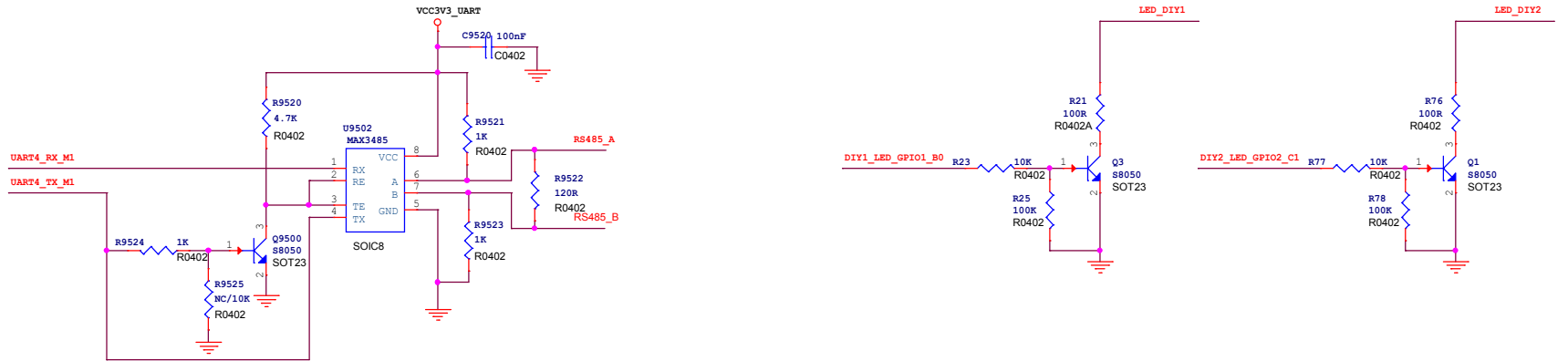
## Gyroscope+G-sensor




<b>Title:</b> Sensor		REV: V1.1
<b>File:</b> ROC-3568-PC		
<b>Create Date:</b> Tuesday, May 19, 2020	<b>Page Num:</b> 32	
<b>Modify Date:</b> Tuesday, August 09, 2022	<b>Page Total:</b> 36	



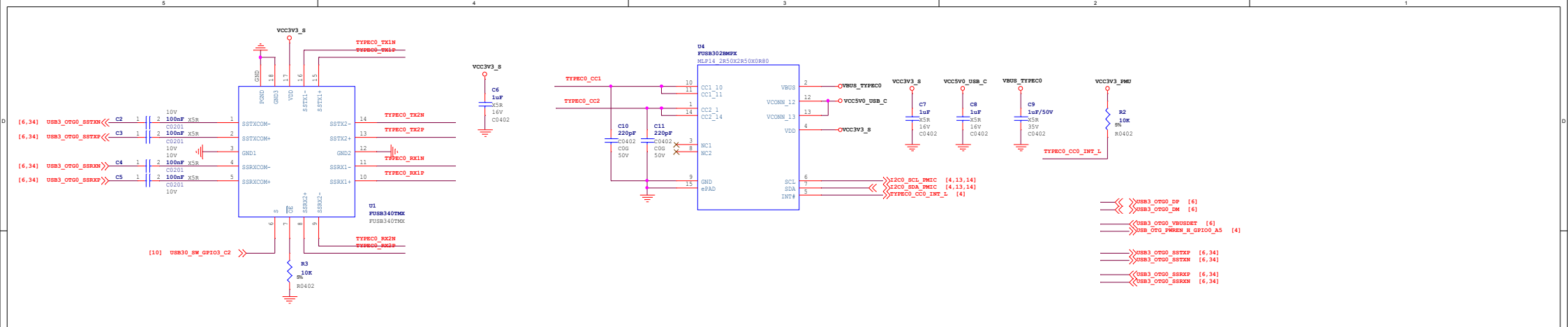
# RS485



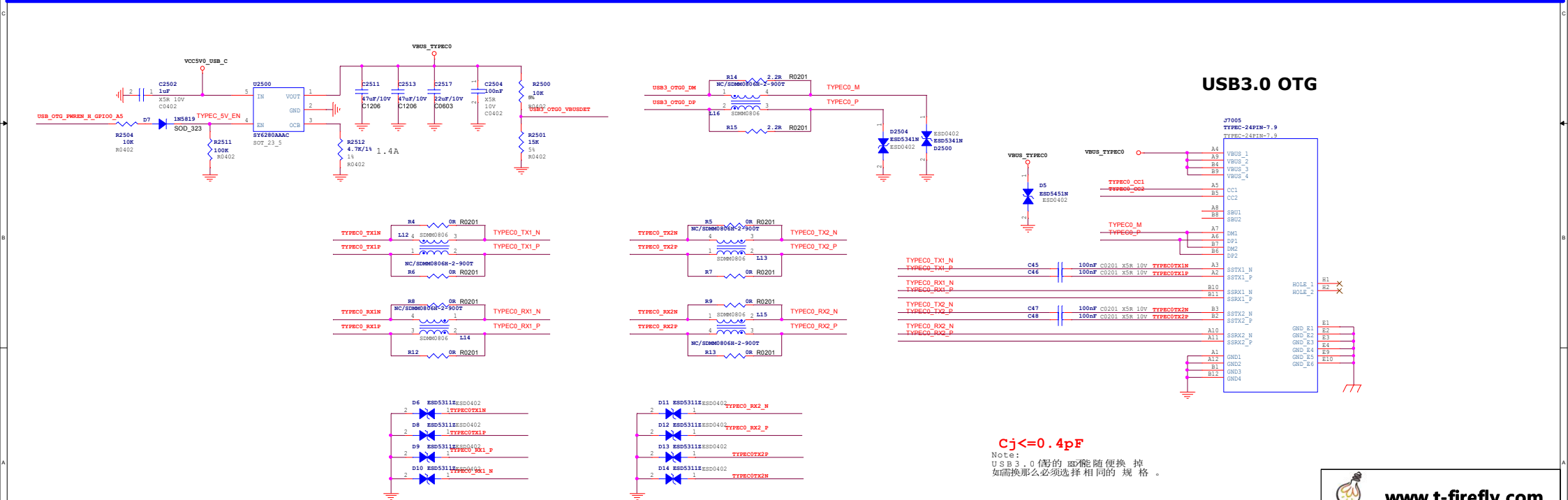

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**Title:** RS232/RS485  
**File:** ROC-3568-PC  
**Create Date:** Friday, July 10, 2020  
**Modify Date:** Tuesday, August 09, 2022

**REV:** V1.1  
**Page Num:** 33  
**Page Total:** 36




- << USB3\_OTG\_DM [6]
- << USB3\_OTG\_DP [6]
- << USB\_OTG\_VBUSDET [6]
- << USB\_OTG\_PRESN\_H\_OTF00\_A5 [4]
- << USB3\_OTG\_SSTXP [6,34]
- << USB3\_OTG\_SSTXN [6,34]
- << USB3\_OTG\_SSRXP [6,34]
- << USB3\_OTG\_SSRXN [6,34]



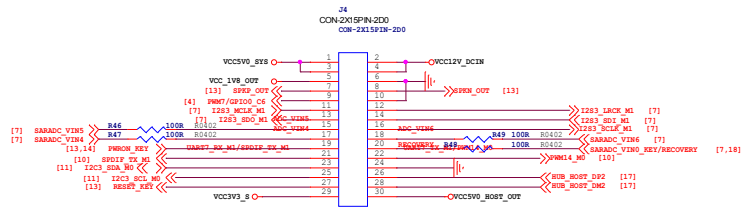
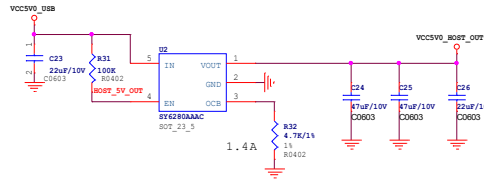
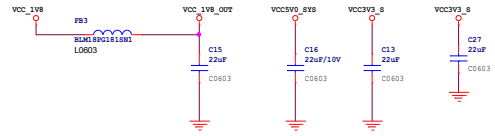
### USB3.0 OTG

**Cj <= 0.4pF**  
 Note:  
 USB3.0 (带的) 电容能随便换掉  
 如需换那么必须选择相同的规格。


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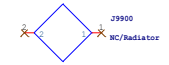
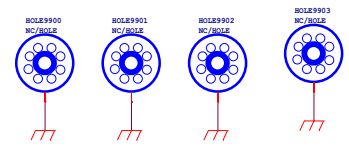
<b>Title: TYPE-C</b>		REV: V1.1
<b>File: ROC-3668-PC</b>		
Create Date: Thursday, April 08, 2021	Page Num: 34	
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SPK Note: 8ohm/1.3W Speaker Output



- 1. GND
- 3. GND
- 5. GND
- 7. 3.3V
- 9. GND
- 11. 1.8V
- 13. 5.0V
- 15. GND
- 17. SARADC\_VIN4
- 19. SARADC\_VIN5
- 21. I2C3\_SDA\_M0/UART3\_RX\_M0/CAN1\_RX\_M0/AUDIOPWM\_LOUT\_P/ACODEC\_ADC\_DATA/GPIO1\_A0\_u
- 23. GND
- 25. EDP\_BL\_PWM1\_M0/PWM1\_M0/GPUAVS/UART0\_RX/GPIO0\_C0\_d
- 27. GND
- 29. I2C1\_SDA/CAN0\_RX\_M0/PCIE20\_BUTTONRSTn/MCU\_JTAG\_TCK/GPIO0\_B4\_u

- 1. GND
- 3. SPK\_OUT
- 5. SPK\_OUT
- 7. GND
- 9. GND
- 11. I2S3\_MCLK\_M1/PWM14\_M1/SPI3\_CLK\_M1/CAN1\_RX\_M1/PCIE30X2\_CLKREQn\_M2/GPIO4\_C2\_d
- 13. I2S3\_LRCK\_M1/EDP\_HPDIN\_M0/SPDIF\_TX\_M2/SATA2\_ACT\_LED/PCIE30X2\_PERSTn\_M2/GPIO4\_C4\_d
- 15. I2S3\_SDO\_M1/PWM12\_M1/SPI3\_MISO\_M1/SATA1\_ACT\_LED/UART9\_TX\_M1/GPIO4\_C5\_d
- 17. GND
- 19. HUB\_HOST\_DP4
- 21. HUB\_HOST\_DM4
- 23. GND
- 25. HUB\_HOST\_DP3
- 27. HUB\_HOST\_DM3
- 29. 5V



- 2. 12V
- 4. 12V
- 6. 12V
- 8. 3.3V
- 10. GND
- 12. 1.8V
- 14. 5.0V
- 16. GND
- 18. SARADC\_VIN0\_KEY/RECOVERY
- 20. SARADC\_VIN6
- 22. I2C3\_SCL\_M0/UART3\_TX\_M0/CAN1\_TX\_M0/AUDIOPWM\_LOUT\_N/ACODEC\_ADC\_CLK/GPIO1\_A1\_u
- 24. GND
- 26. PWM7\_IR/SPI0\_CS0\_M0/PCIE30X2\_PERSTn\_M0/GPIO0\_C6\_d
- 28. GND
- 30. I2C1\_SCL/CAN0\_TX\_M0/PCIE30X1\_BUTTONRSTn/MCU\_JTAG\_TDO/GPIO0\_B3\_u