Table of Content

Description

Note

Option

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

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Size	Title:	REV
A3	Rock 3 Compute Module Plus	V1.1
	Page Name: Index and Notes	
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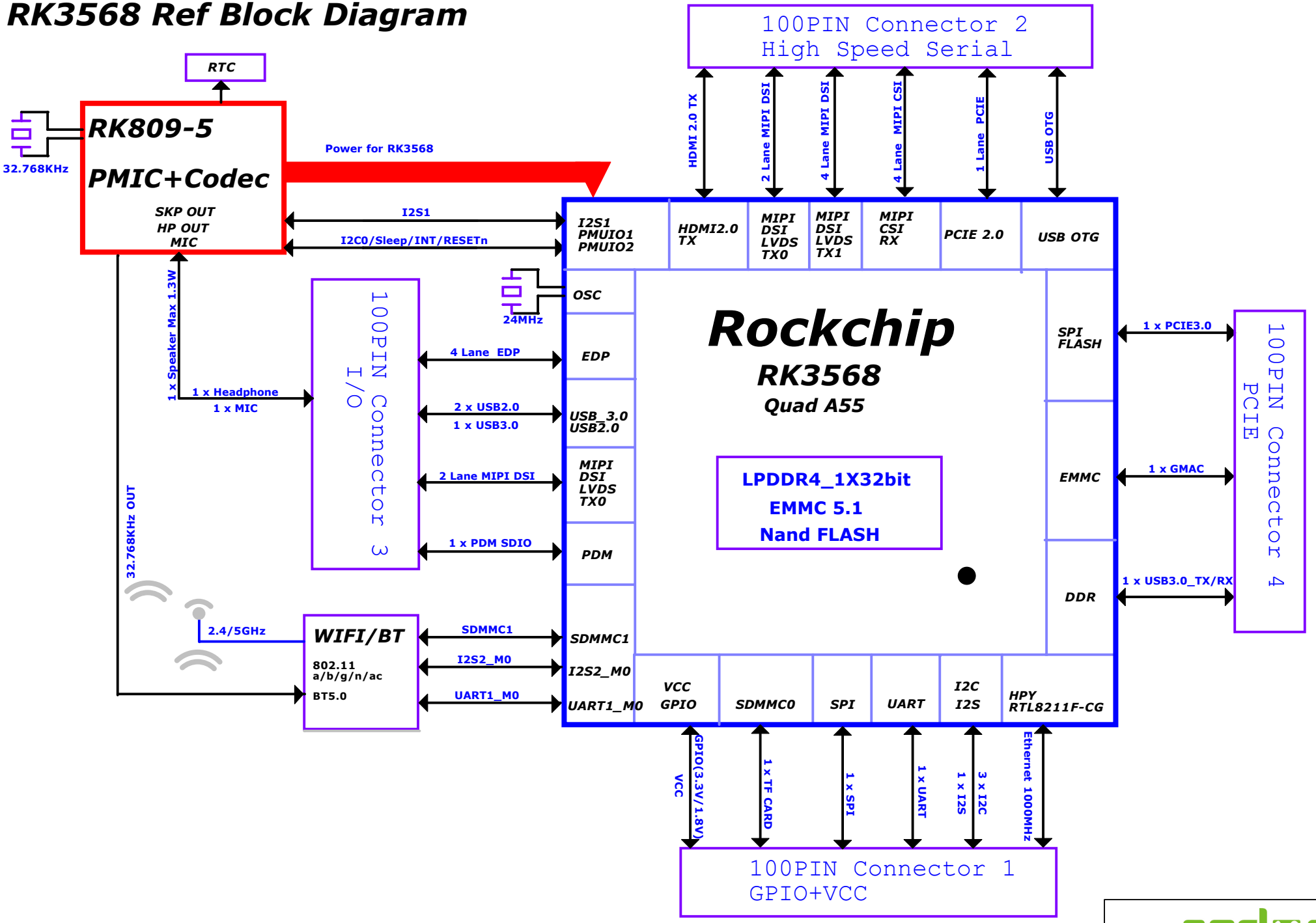
Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2021-04-10		1:Revision preliminary version	
V1.1	2021-10-29			

RK3568 Ref Block Diagram



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Size	Title:	Rock 3 Compute Module Plus	REV
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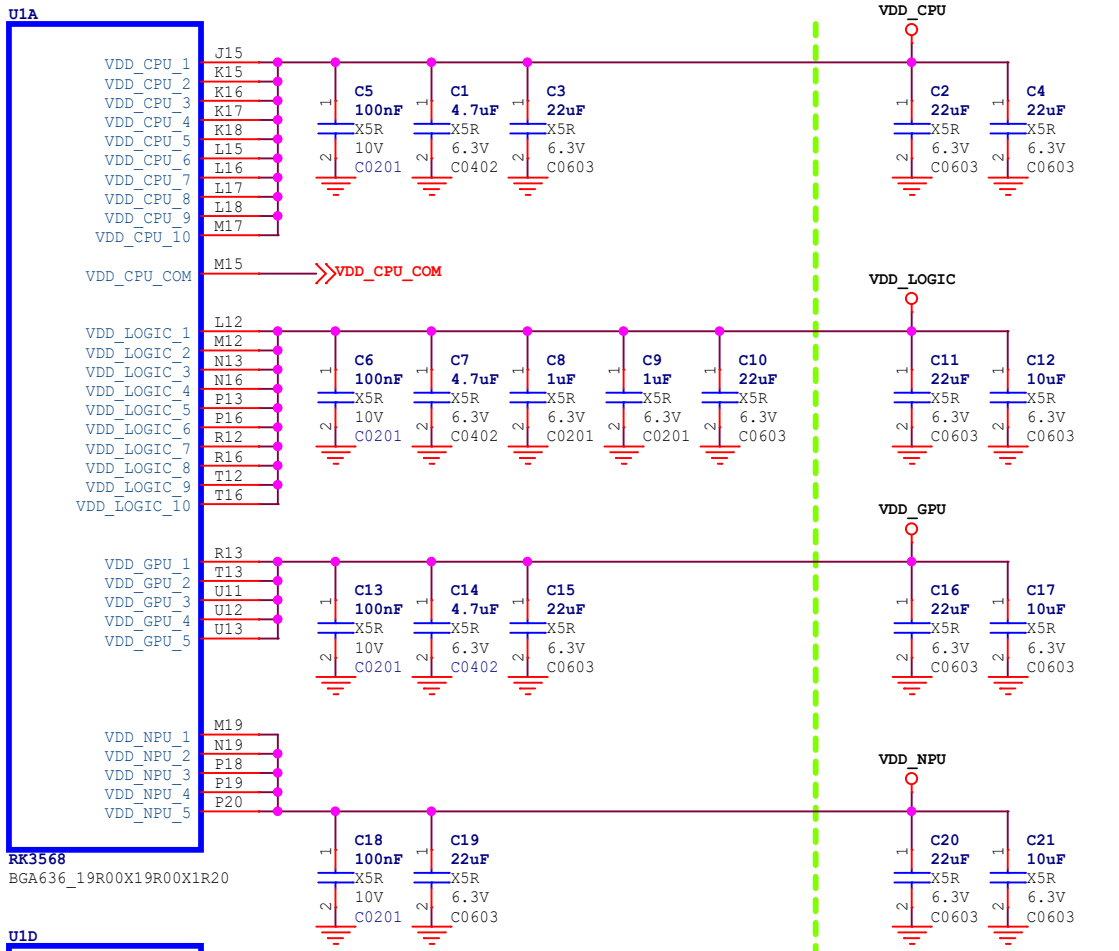
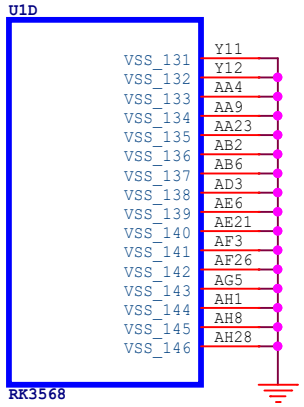
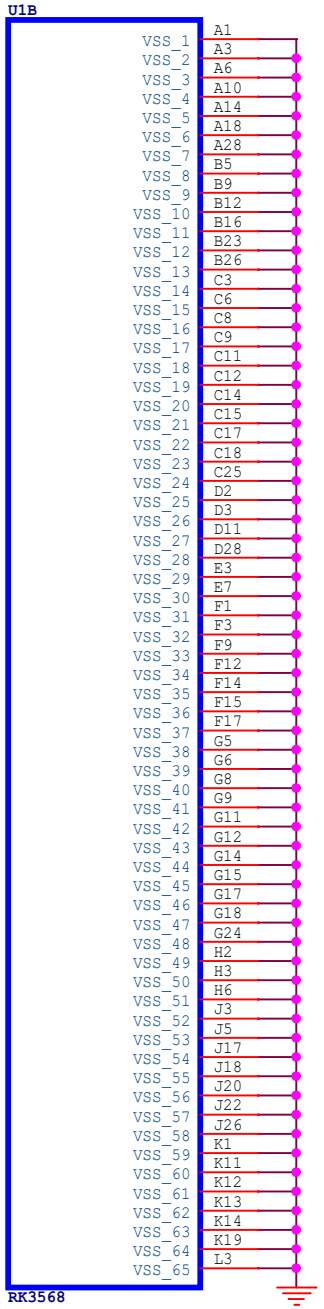
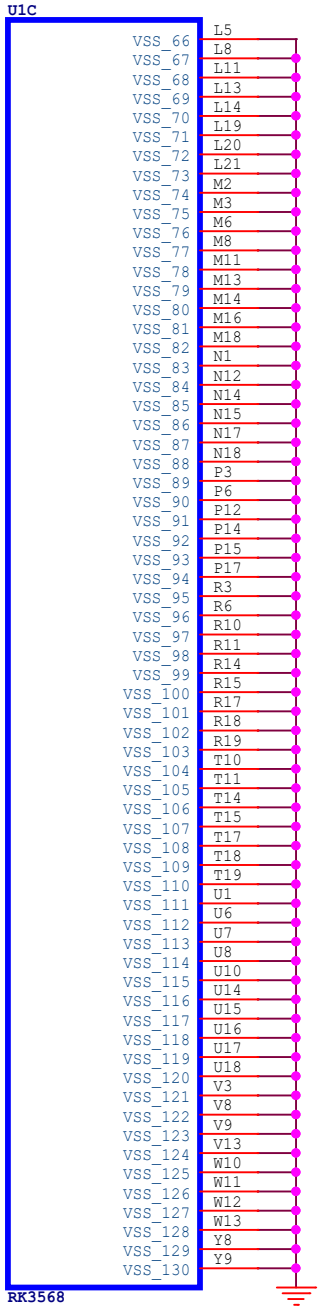
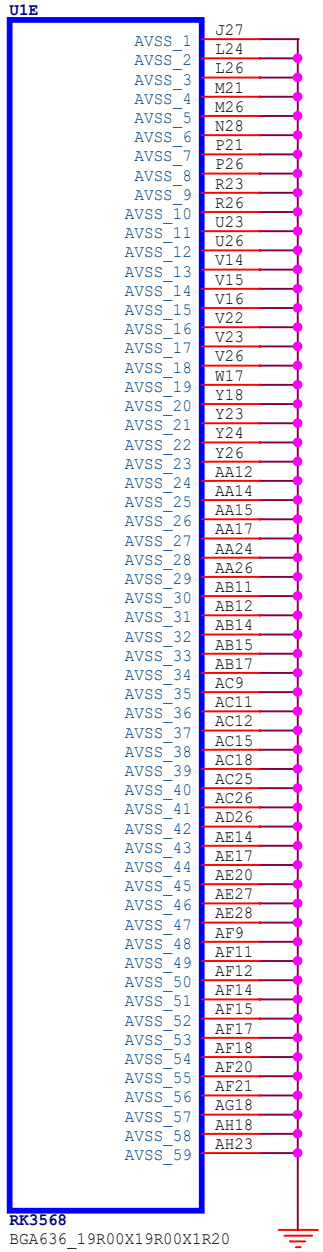
RK3568_ABCDE (Power&Gnd)











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Size	Title:	Rock 3 Compute Module Plus	REV
A4	Page Name:	RK3568_Power/GND	V1.1
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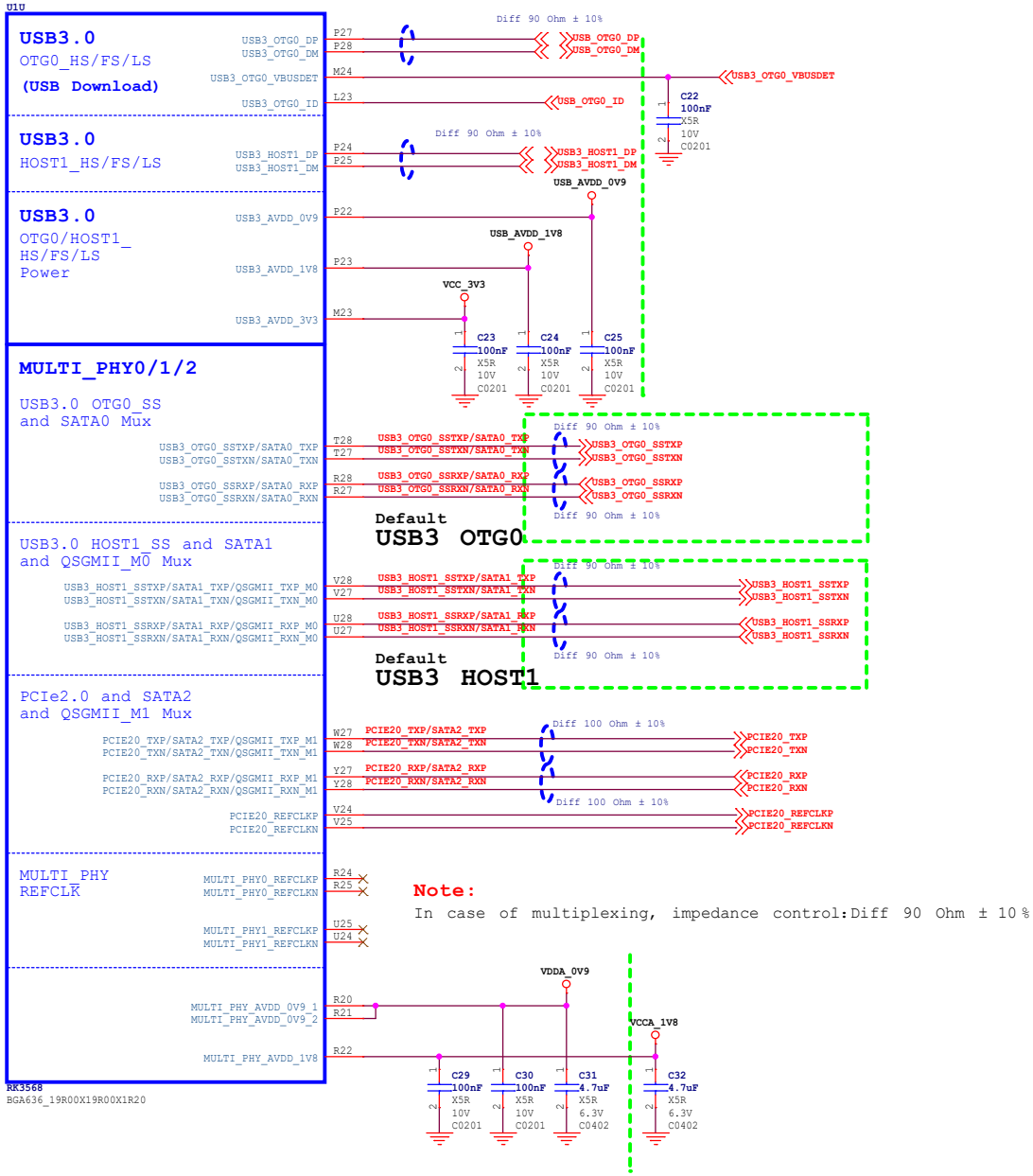
RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)



Note:
In case of multiplexing, impedance control:Diff 90 Ohm ± 10%

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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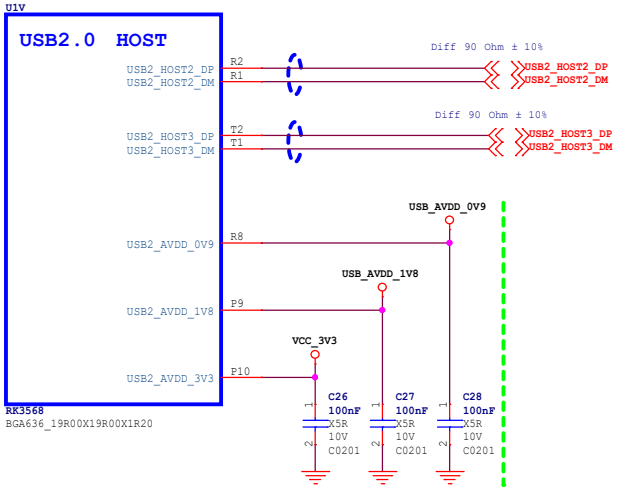
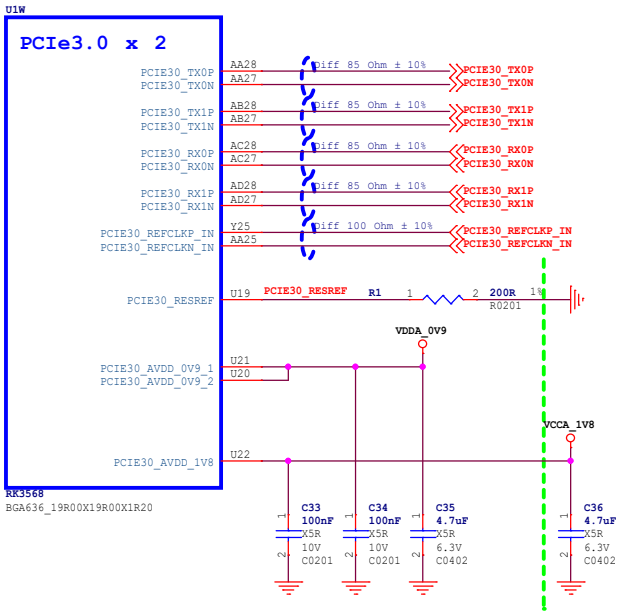
RK3568_V(USB2.0 HOST)



RK3568_W(PCIe3.0 x2)



Size A3	Title: Rock 3 Compute Module Plus		REV V1.1
	Page Name: RK3568_USB/PCIe/SATA PHY		
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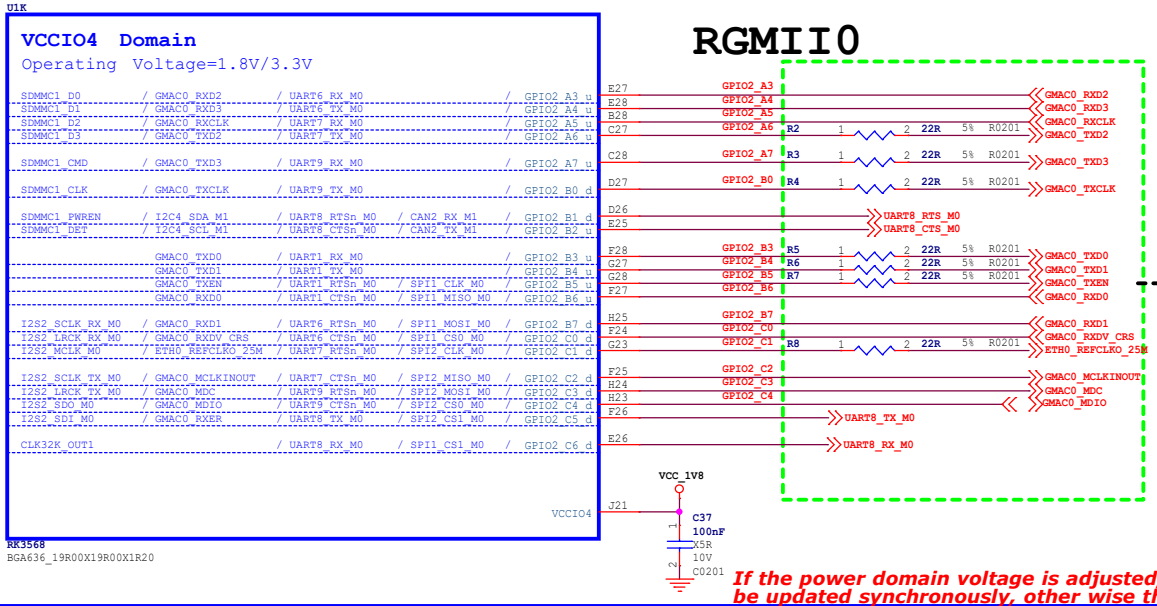
RK3568_K(VCCIO4 Domain)



RGMII0

Note:

If Ethernet PHY uses other models, please note whether the default pull-up and pull-down of GPIO affect Ethernet PHY function

At present, TXEN will be affected if it defaults to high level need to add a 4.7K resistance to ground

Note:

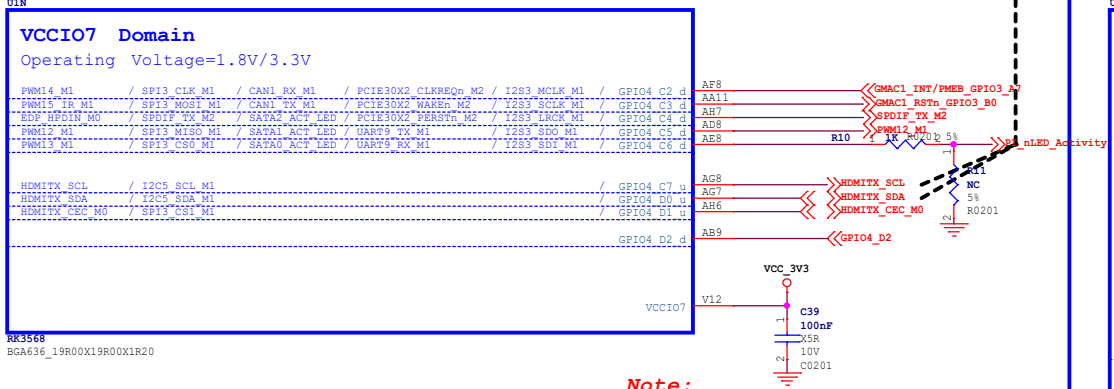
According to the actual choice of mounted Cannot be mounted at the same time
Default:1.8V
Select the voltage according to the application

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

RK3568_N(VCCIO7 Domain)

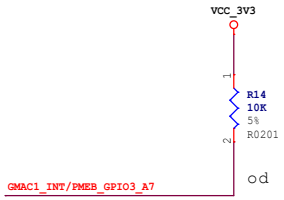
Note:

When use HDMI, HDMITX_SCL/SDA cannot be shared with other devices

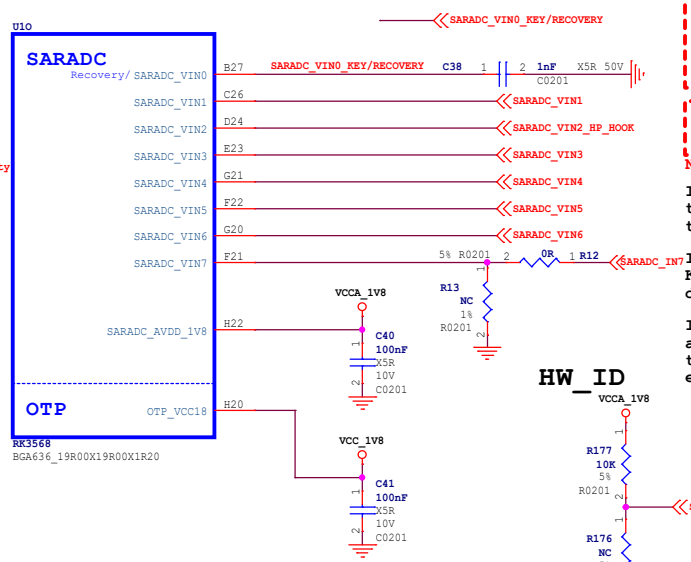


Note:

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!



RK3568_O(SARADC/OTP)



Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

Note:

Must be mounted

Note:

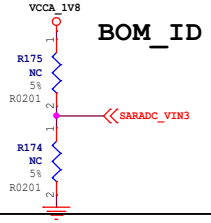
If there is no Key requirement, two test points must be reserved to facilitate firmware update

It is suggested to reserve a Key to facilitate the development debug

If SARADC_VIN0=0V at after power on and reset, then system will enter into loader mode.

HW_ID

BOM_ID



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A3	Page Name:	RK3568_ADC/RGMII0/HDMI	V1.1
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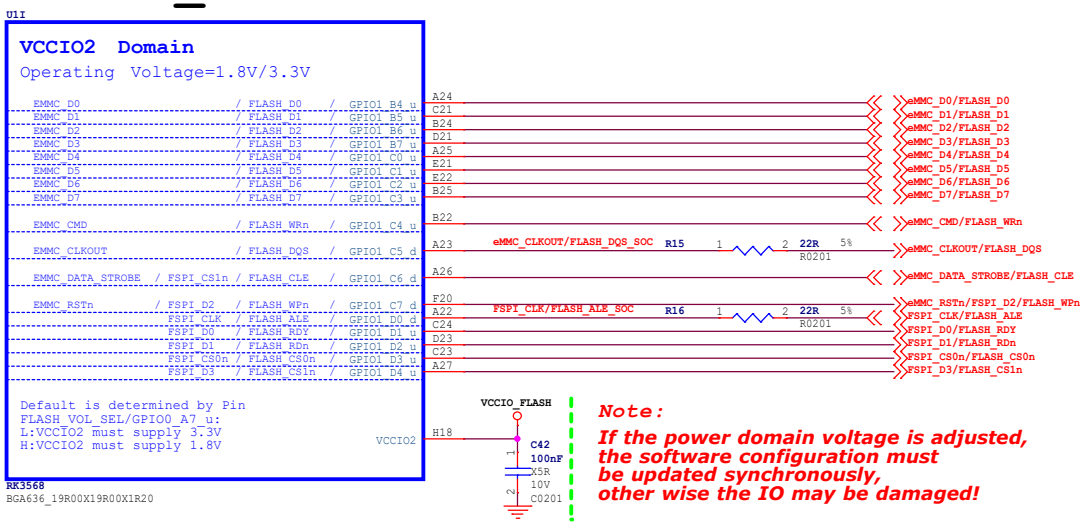
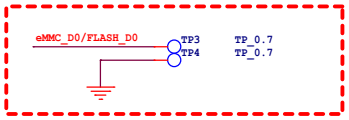
RK3568_I(VCCIO2 Domain)



Note:

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

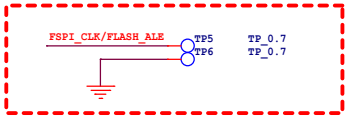


Note:

For eMMC or Nand Flash:
If eMMC_D0/FLASH_D0=0V at after power on and reset, then system will enter into Maskrom mode.

Layout note:

Test point must be placed on the line, and no branch can be added



Note:

For SPI Flash:
If FSPI_CLK=0V at after power on and reset, then system will enter into Maskrom mode.

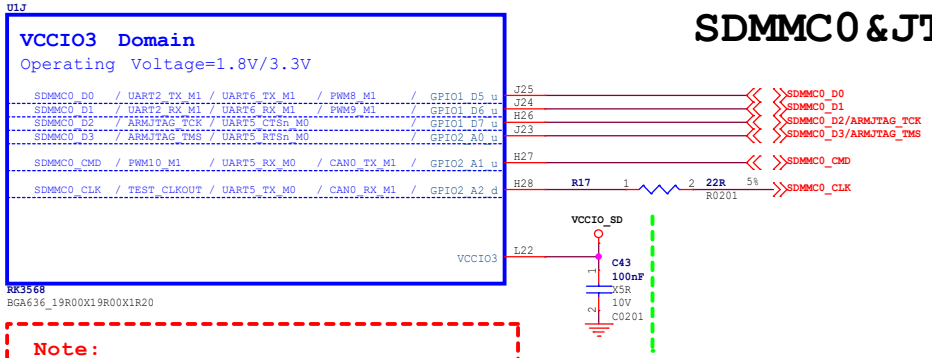
Note:
Reserve TestPoint for put the system into Maskrom mode to update the firmware When writing mismatched firmware or other conditions result in boot failure, use this test point

Except in this case, please use Recovery Key
Put the system into loader mode to update the firmware

RK3568_J(VCCIO3 Domain)

Default

SDMMC0&JTAG



Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

Size A3	Title: Rock 3 Compute Module Plus	REV V1.1
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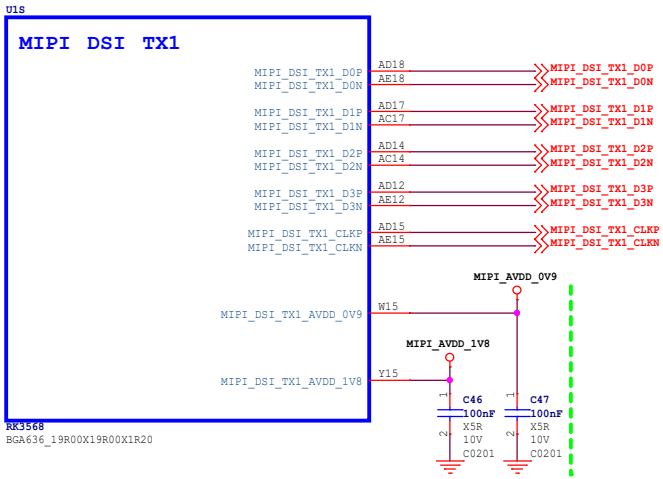
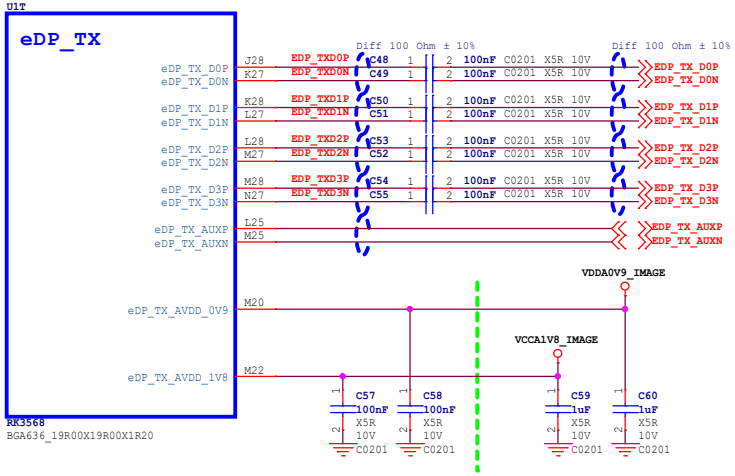
RK3568_R(MIPI_DSI_TX0/LVDS_TX0)

RK3568_S(MIPI_DSI_TX1)



RK3568_T(eDP TX)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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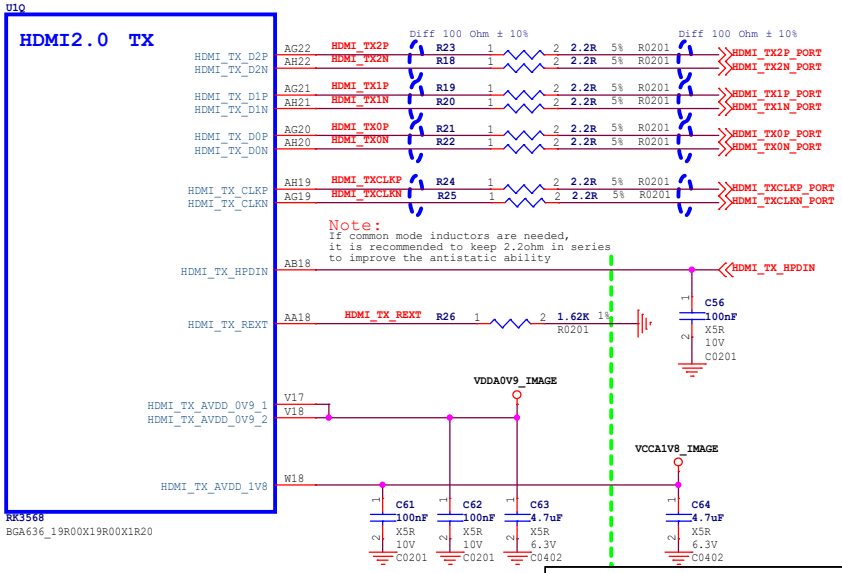
RK3568_Q(HDMI2.0 TX)



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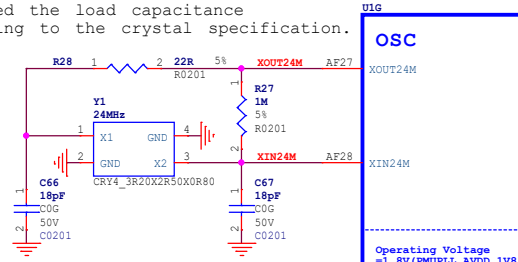
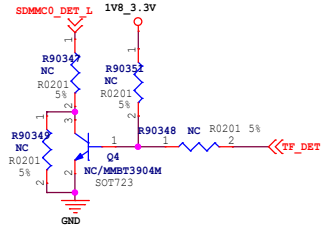
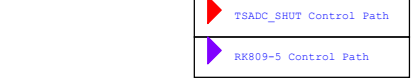
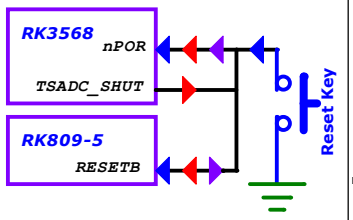
RK3568_G(OSC/PLL/PMUIO1/2)

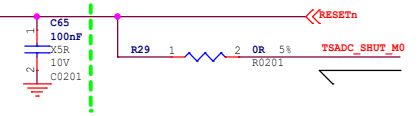
Note:
Adjusted the load capacitance according to the crystal specification.

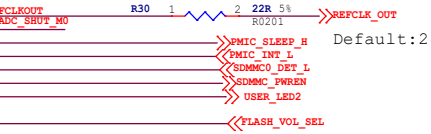




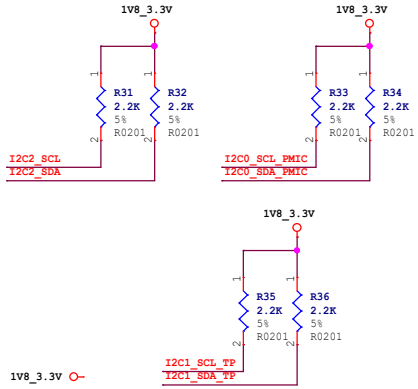


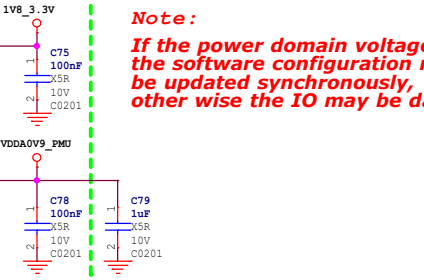






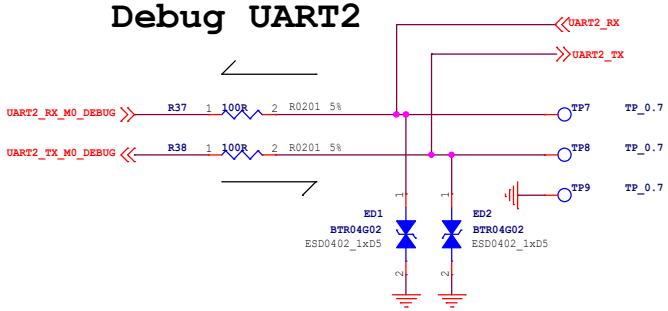
Default:24MHz

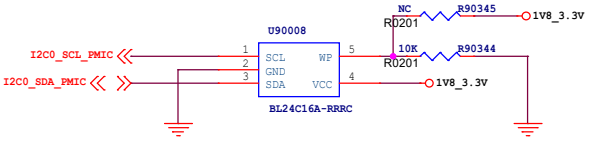




Note:
If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

Debug UART2





Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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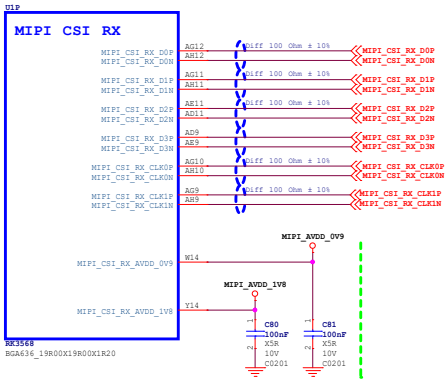
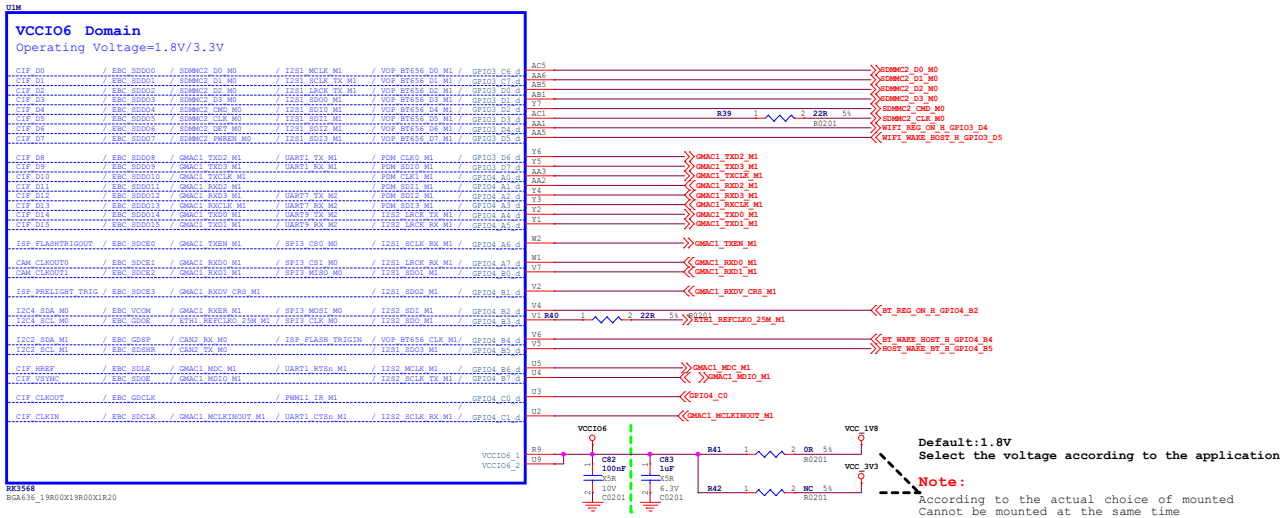
RK3568_P(MIPI_CSI_RX)



Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0
		MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

RK3568_M(VCCIO6 Domain)



Default:1.8V
Select the voltage according to the application

Note:
According to the actual choice of mounted
Cannot be mounted at the same time

Note:
If the power domain voltage is adjusted,
the software configuration must
be updated synchronously,
other wise the IO may be damaged!

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Note:
Camera MCLK can select the following clock:
1:CAM_CLKOUT0
2:CAM_CLKOUT1
3:CIF_CLKOUT
4:REFCLK_OUT

Attention to the voltage matching

Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

BT1120 16bit Mode:
Default: D0-D7 <--> Y0-Y7 , D8-D15 <--> C0-C7
Swap ON: D0-D7 <--> C0-C7 , D8-D15 <--> Y0-Y7

GMAC	Direction	GEPHY	GMAC	Direction	FEPHY
GMACx_TXD0	------->	PHYx_TXD0	GMACx_TXD0	------->	PHYx_TXD0
GMACx_TXD1	------->	PHYx_TXD1	GMACx_TXD1	------->	PHYx_TXD1
GMACx_TXD2	------->	PHYx_TXD2			
GMACx_TXD3	------->	PHYx_TXD3			
GMACx_TXEN	------->	PHYx_TXEN	GMACx_TXEN	------->	PHYx_TXEN
GMACx_TXCLK	------->	PHYx_TXCLK			
GMACx_RXD0	<-------	PHYx_RXD0	GMACx_RXD0	<-------	PHYx_RXD0
GMACx_RXD1	<-------	PHYx_RXD1	GMACx_RXD1	<-------	PHYx_RXD1
GMACx_RXD2	<-------	PHYx_RXD2			
GMACx_RXD3	<-------	PHYx_RXD3			
GMACx_RXDV	<-------	PHYx_RXDV	GMACx_RXDV	<-------	PHYx_RXDV
GMACx_RXCLK	<-------	PHYx_RXCLK			
GMACx_RXER			GMACx_RXER	<-------	PHYx_RXER
GMACx_MDC	------->	PHYx_MDC	GMACx_MDC	------->	PHYx_MDC
GMACx_MDIO	<------->	PHYx_MDIO	GMACx_MDIO	<------->	PHYx_MDIO
ETHx_REFCLKO_25M	------->	PHYx_XTALIN PHYx_CLKOUT125(Option)			
GMACx_MCLKINOUT	<-------		GMACx_MCLKINOUT	------->	PHYx_XTALIN/REFCLK
GPIO	------->	PHYx_RSTn	GPIO	------->	PHYx_RSTn
GPIO	<-------	PHYx_INT/PMEB	GPIO	<-------	PHYx_INT/PMEB

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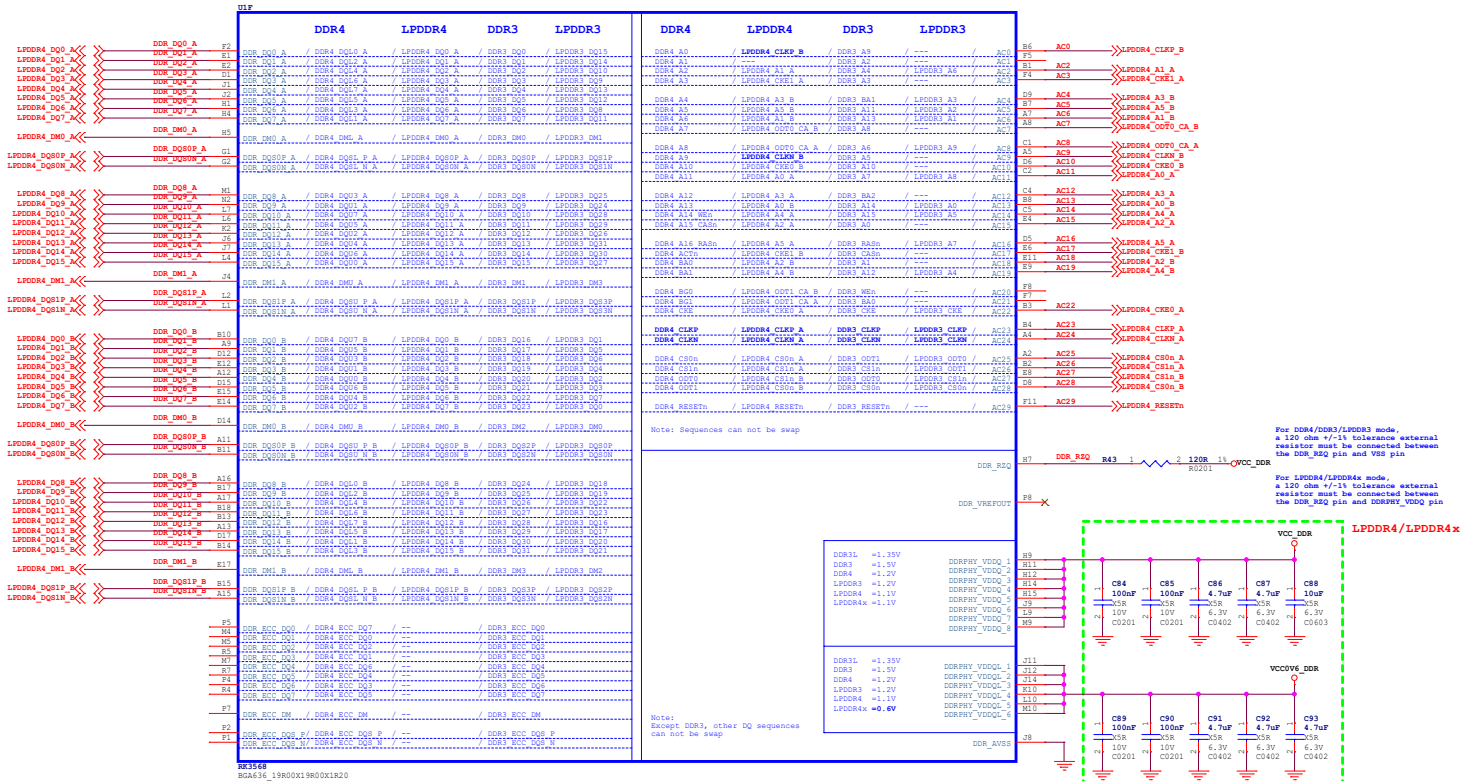
RK3568_F (DDR PHY)



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RK3568_L(VCCIO5 Domain)

U1L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC_D0	/ VOP_BT656_D0_M0	/ SPI0_MISO_M1	/ PCIE20_CLKREQn_M1	/ I2S1_MCLK_M2	/ GPIO2_D0_d
LCDC_D1	/ VOP_BT656_D1_M0	/ SPI0_MOSI_M1	/ PCIE20_WAKEn_M1	/ I2S1_SCLK_TX_M2	/ GPIO2_D1_d
LCDC_D2	/ VOP_BT656_D2_M0	/ SPI0_CS0_M1	/ PCIE30X1_CLKREQn_M1	/ I2S1_LRCK_TX_M2	/ GPIO2_D2_d
LCDC_D3	/ VOP_BT656_D3_M0	/ SPI0_CLK_M1	/ PCIE30X1_WAKEn_M1	/ I2S1_SDI0_M2	/ GPIO2_D3_d
LCDC_D4	/ VOP_BT656_D4_M0	/ SPI2_CS1_M1	/ PCIE30X2_CLKREQn_M1	/ I2S1_SDI1_M2	/ GPIO2_D4_d
LCDC_D5	/ VOP_BT656_D5_M0	/ SPI2_CS0_M1	/ PCIE30X2_WAKEn_M1	/ I2S1_SDI2_M2	/ GPIO2_D5_d
LCDC_D6	/ VOP_BT656_D6_M0	/ SPI2_MOSI_M1	/ PCIE30X2_PERSTn_M1	/ I2S1_SDI3_M2	/ GPIO2_D6_d
LCDC_D7	/ VOP_BT656_D7_M0	/ SPI2_MISO_M1	/ UART8_TX_M1	/ I2S1_SDO0_M2	/ GPIO2_D7_d
LCDC_CLK	/ VOP_BT656_CLK_M0	/ SPI2_CLK_M1	/ UART8_RX_M1	/ I2S1_SDO1_M2	/ GPIO3_A0_d
LCDC_D8	/ VOP_BT1120_D0	/ SPI1_CS0_M1	/ PCIE30X1_PERSTn_M1	/ SDMMC2_D0_M1	/ GPIO3_A1_d
LCDC_D9	/ VOP_BT1120_D1	/ GMAC1_TXD2_M0	/ I2S3_MCLK_M0	/ SDMMC2_D1_M1	/ GPIO3_A2_d
LCDC_D10	/ VOP_BT1120_D2	/ GMAC1_TXD3_M0	/ I2S3_SCLK_M0	/ SDMMC2_D2_M1	/ GPIO3_A3_d
LCDC_D11	/ VOP_BT1120_D3	/ GMAC1_RXD2_M0	/ I2S3_LRCK_M0	/ SDMMC2_D3_M1	/ GPIO3_A4_d
LCDC_D12	/ VOP_BT1120_D4	/ GMAC1_RXD3_M0	/ I2S3_SDO_M0	/ SDMMC2_CMD_M1	/ GPIO3_A5_d
LCDC_D13	/ VOP_BT1120_CLK	/ GMAC1_TXCLK_M0	/ I2S3_SDI_M0	/ SDMMC2_CLK_M1	/ GPIO3_A6_d
LCDC_D14	/ VOP_BT1120_D5	/ GMAC1_RXCLK_M0		/ SDMMC2_DET_M1	/ GPIO3_A7_d
LCDC_D15	/ VOP_BT1120_D6	/ ETH1_REFCLKO_25M_M0		/ SDMMC2_PWREN_M1	/ GPIO3_B0_d
LCDC_D16	/ VOP_BT1120_D7	/ GMAC1_RXD0_M0	/ UART4_RX_M1	/ PWM8_M0	/ GPIO3_B1_d
LCDC_D17	/ VOP_BT1120_D8	/ GMAC1_RXD1_M0	/ UART4_TX_M1	/ PWM9_M0	/ GPIO3_B2_d
LCDC_D18	/ VOP_BT1120_D9	/ GMAC1_RXDV_CRS_M0	/ I2C5_SCL_M0	/ PDM_SDI0_M2	/ GPIO3_B3_d
LCDC_D19	/ VOP_BT1120_D10	/ GMAC1_RXER_M0	/ I2C5_SDA_M0	/ PDM_SDI1_M2	/ GPIO3_B4_d
LCDC_D20	/ VOP_BT1120_D11	/ GMAC1_TXD0_M0	/ I2C3_SCL_M1	/ PWM10_M0	/ GPIO3_B5_d
LCDC_D21	/ VOP_BT1120_D12	/ GMAC1_TXD1_M0	/ I2C3_SDA_M1	/ PWM11_IR_M0	/ GPIO3_B6_d
LCDC_D22	/ PWM12_M0	/ GMAC1_TXEN_M0	/ UART3_TX_M1	/ PDM_SDI2_M2	/ GPIO3_B7_d
LCDC_D23	/ PWM13_M0	/ GMAC1_MCLKINOUT_M0	/ UART3_RX_M1	/ PDM_SDI3_M2	/ GPIO3_C0_d
LCDC_HSYNC	/ VOP_BT1120_D13	/ SPI1_MOSI_M1	/ PCIE20_PERSTn_M1	/ I2S1_SDO2_M2	/ GPIO3_C1_d
LCDC_VSYNC	/ VOP_BT1120_D14	/ SPI1_MISO_M1	/ UART5_TX_M1	/ I2S1_SDO3_M2	/ GPIO3_C2_d
LCDC_DEN	/ VOP_BT1120_D15	/ SPI1_CLK_M1	/ UART5_RX_M1	/ I2S1_SCLK_RX_M2	/ GPIO3_C3_d
PWM14_M0	/ VOP_PWM_M1	/ GMAC1_MDC_M0	/ UART7_TX_M1	/ PDM_CLK1_M2	/ GPIO3_C4_d
PWM15_IR_M0	/ SPDIF_TX_M1	/ GMAC1_MDIO_M0	/ UART7_RX_M1	/ I2S1_LRCK_RX_M2	/ GPIO3_C5_d

AG6 SPI0_MISO_M1
AD7 SPI0_MOSI_M1
AC8 SPI0_CSO_M1
AC7 SPI0_CLK_M1
AF5 WL_nDis
AF6 SPI2_CS0
AD6 SPI2_MOSI_M1
AH5 SPI2_MISO_M1

AH4 SPI2_CLK_M1

AB8 SPI1_CSO_M1
AE5 I2S3_MCLK_M0
AG4 BT_nDis
AF4 I2S3_LRCK_RX_M0
AH3 I2S3_SDO0_M0
AG3 I2S3_SDI0_M0
AH2 GPIO3_A7
AG2 CAM_GPIO

AG1 PWM8_M0
AF2 PWM9_M0
AF1 I2C5_SCL_M0
AE1 I2C5_SDA_M0
AE2 I2C3_SCL_M1
AE3 I2C3_SDA_M1
AD4 PWM12_M0
AD2 PWM13_M0

AD1 SPI1_MOSI_M1
AA7 SPI1_MISO_M1
AC4 SPI1_CLK_M1

AC3 nPWR_LED
AC2 PWM15_IR_M0

V10 VCCIO5_1
V11 VCCIO5_2

RK3568
BGA636_19R00X19R00X1R20

1V8_3.3V
C94 100nF X5R 10V C0201

Note:
If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

1V8_3.3V
R44 2.2K 5% R0201
R45 2.2K 5% R0201
I2C5_SCL_M0
I2C5_SDA_M0

1V8_3.3V
R46 2.2K 5% R0201
R47 2.2K 5% R0201
I2C3_SCL_M1
I2C3_SDA_M1

+1V8 R48 1 0R 2 R0603 5% VCC_1V8
+3V3 R49 1 0R 2 R0603 5% VCC_3V3
C95 100nF X5R 10V C0201
C96 100nF X5R 10V C0201

1V8_3.3V
R50 1 0R 2 R0603 5% GPIO_VREF
R51 1 NC 2 R0201 5% VCC_1V8
R53 1 NC 2 R0201 5% VCC_3V3
D1 TVS SOD_323
C97 4.7UF X5R 6.3V C0402
R52 NC 5% R0201

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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Size	Title:	Rock 3 Compute Module Plus	REV
A4	Page Name:	RK3568_GPIO2_GPIO3	V1.1
Date:	Tuesday, November 16, 2021	Sheet 12 of 25	

RK3568_H(VCCIO1 Domain)

U1H

VCCIO1 Domain

Operating Voltage=1.8V/3.3V

I2C3_SDA_M0	/ UART3_RX_M0	/ CAN1_RX_M0		/ AUDIOPWM_LOUT_P	/ ACODEC_ADC_DATA	/ GPIO1_A0_u
I2C3_SCL_M0	/ UART3_TX_M0	/ CAN1_TX_M0		/ AUDIOPWM_LOUT_N	/ ACODEC_ADC_CLK	/ GPIO1_A1_u
I2S1_MCLK_M0	/ UART3_RTSn_M0	/ SCR_CLK	/ PCIE30X1_PERSTn_M2			/ GPIO1_A2_d
I2S1_SCLK_TX_M0	/ UART3_CTSn_M0	/ SCR_IO	/ PCIE30X1_WAKEn_M2		/ ACODEC_DAC_CLK	/ GPIO1_A3_d
I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0		/ SPDIF_TX_M0		/ GPIO1_A4_d
I2S1_LRCK_TX_M0	/ UART4_RTSn_M0	/ SCR_RST	/ PCIE30X1_CLKREQn_M2		/ ACODEC_DAC_SYNC	/ GPIO1_A5_d
I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0		/ AUDIOPWM_ROUT_P		/ GPIO1_A6_d
I2S1_SDO0_M0	/ UART4_CTSn_M0	/ SCR_DET		/ AUDIOPWM_ROUT_N	/ ACODEC_DAC_DATAL	/ GPIO1_A7_d
I2S1_SDO1_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0	/ PCIE20_CLKREQn_M2		/ ACODEC_DAC_DATAR	/ GPIO1_B0_d
I2S1_SDO2_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0	/ PCIE20_WAKEn_M2		/ ACODEC_ADC_SYNC	/ GPIO1_B1_d
I2S1_SDO3_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0	/ PCIE20_PERSTn_M2			/ GPIO1_B2_d
	I2S1_SDI0_M0	/ PDM_SDI0_M0				/ GPIO1_B3_d

VCCIO1

RK3568

BGA636_19R00X19R00X1R20

D18 — GPIO1_A0
E18 — GPIO1_A1

A19 — I2S1_MCLK_M0_SOC — R54 1 2 22R 5% R0201 — I2S1_MCLK_M0_RK809

B19 — I2S1_SCLK_TX_M0_SOC — R55 1 2 22R 5% R0201 — I2S1_SCLK_TX_M0_RK809

F18 — GPIO1_A4

A20 — I2S1_LRCK_TX_M0_SOC — R56 1 2 22R 5% R0201 — I2S1_LRCK_TX_M0_RK809

C20 — PDM_CLK0_M0_SOC — R57 1 2 22R 5% R0201 — PDM_CLK0_M0_RK809

B20 — I2S1_SDO0_M0_RK809
D20 — PCIE20_CLKREQn_M2
E20 — GPIO1_B1
A21 — Pcie_nRST
B21 — I2S1_SDI0_M0/PDM_SDI0_M0_RK809

VCCIO_ACODEC

H17 — C98 100nF X5R 10V C0201

Default 3.3V

Note:

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

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Size	Title:	Rock 3 Compute Module Plus	REV
A4	Page Name:	RK3568_Audio	V1.1
Date:	Tuesday, November 16, 2021	Sheet 13 of 25	

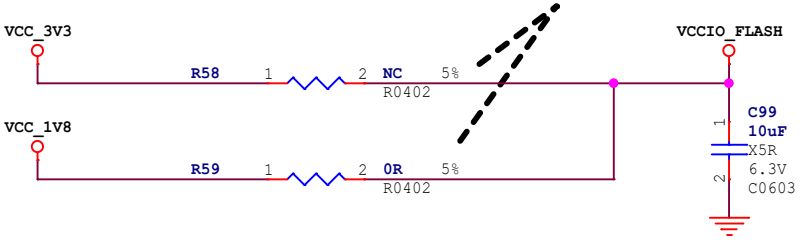
FLASH_VOL_SEL

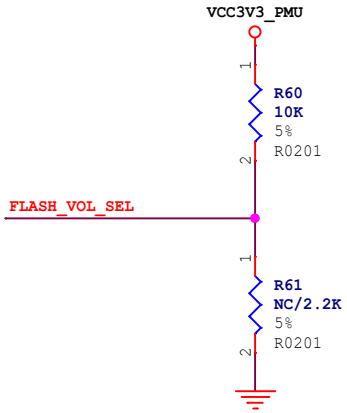
Flash Power Manage

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Optional 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 1.8V, Optional 3.3V	FLASH_VOL_SEL --> Logic=H(Default)

Note:

According to the actual choice of mounted
Cannot be mounted at the same time





Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L:3.3V IO driven
Logic=H:1.8V IO driven

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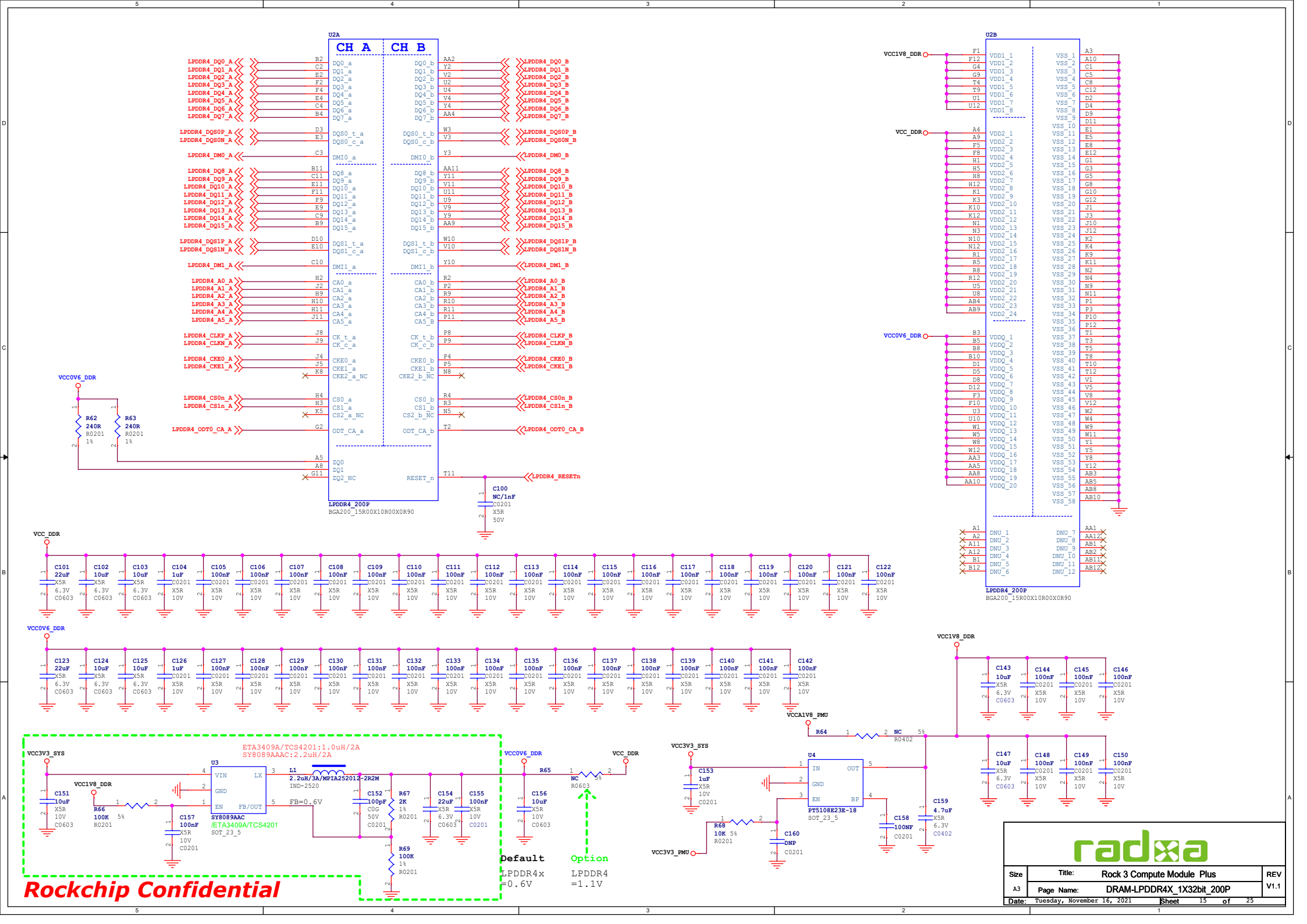
Size	Title:	Rock 3 Compute Module Plus	REV
A4	Page Name:	Power_Flash Power Manage	V1.1
Date:	Tuesday, November 16, 2021	Sheet 14 of 25	


U2A
CH A
CH B
LPDDR4_200P
BGA200_15R00X10R00X0R90
U2B
LPDDR4_200P
BGA200_15R00X10R00X0R90
VCC1V8_DDR
VCC_DDR
VCC0V6_DDR
R62 240R R0201 1%
R63 240R R0201 1%
C100 NC/1nF C0201 X5R 50V
ETA3409A/TCS4201:1.0uH/2A
SY8089AAAC:2.2uH/2A
U3
SY8089AAC
/ETA3409A/TCS4201
SOT_23_5
L1 2.2uH/3A/MPIA252012-2R2M IND-2520
FB=0.6V
R65 NC R0603
R66 100K R0201
R67 2K R0201
R69 100K R0201
C151 10uF X5R 10V C0603
C152 100pF C0G 50V C0201
C154 22uF X5R 6.3V C0603
C155 100nF X5R 10V C0201
C156 10uF X5R 10V C0603
C157 100nF X5R 10V C0201
Default
LPDDR4x
=0.6V
Option
LPDDR4
=1.1V
VCCA1V8_PMU
VCC3V3_PMU
VCC3V3_SYS
U4
PT5108E23E-18
SOT_23_5
R64 NC R0402
R68 10K R0201
C153 1uF X5R 10V C0201
C158 100NF C0201
C159 4.7uF X5R 6.3V C0402
C160 DNP C0201
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Size A3
Title: Rock 3 Compute Module Plus
REV V1.1
Page Name: DRAM-LPDDR4X_1X32bit_200P
Date: Tuesday, November 16, 2021
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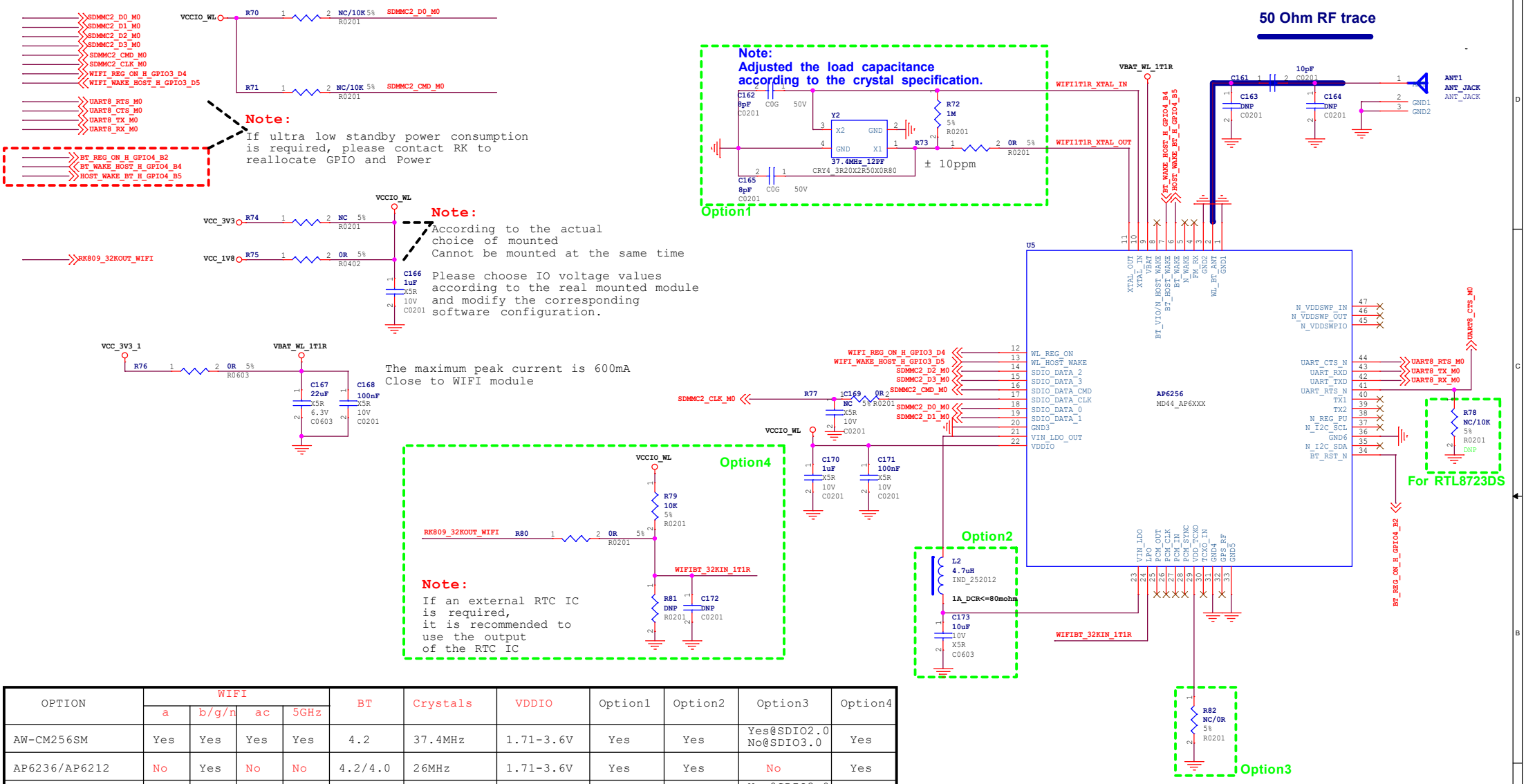
SDIO WIFI/BT MODULE

And Giga PHY0 Option



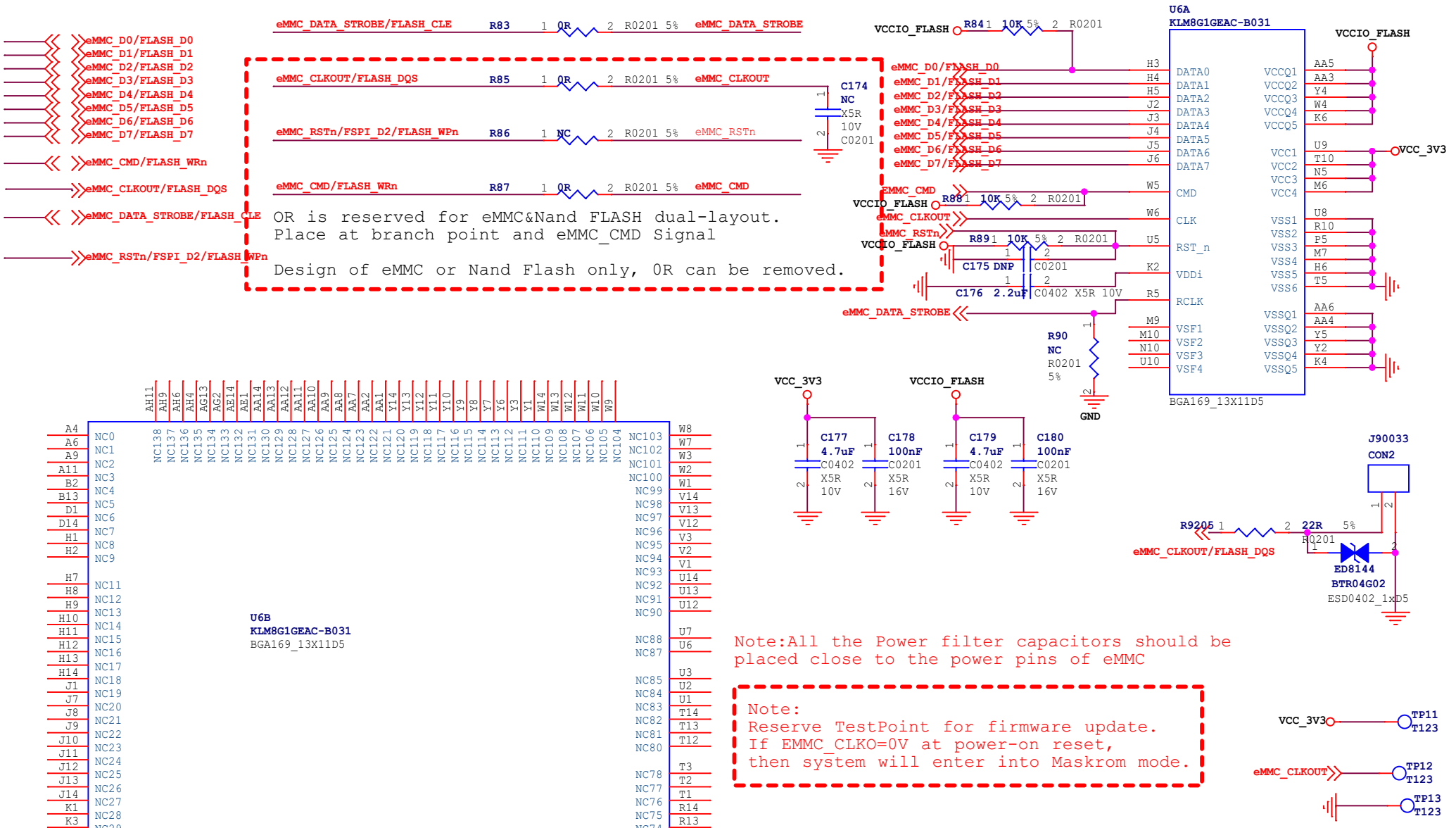
OPTION	WIFI				BT	Crystals	VDDIO	Option1	Option2	Option3	Option4
	a	b/g/n	ac	5GHz							
AW-CM256SM	Yes	Yes	Yes	Yes	4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	Yes
AP6236/AP6212	No	Yes	No	No	4.2/4.0	26MHz	1.71-3.6V	Yes	Yes	No	Yes
AP6256/AP6255	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	Yes
RTL8189ETV Module F89FTSM12-W3	No	Yes	No	No	No	Module Integrated	1.8-3.3V	No	No	No	No
RTL8723BS Module F23BDSM23-W2	No	Yes	No	No	4.0	Module Integrated	1.62-3.6V	No	No	No	No
RTL8723DS Module 6223A-SRD	No	Yes	No	No	4.2	Module Integrated	1.62-3.6V	No	No	No	No
QCA9377 Module 8223A-SR	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	Yes
RTL8821CS Module 6221A-SRC	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	No

Using RTL8189ETV/FTV modules,please notice WIFI REG ON is on pin12 or pin34, choose according to the actual condition.

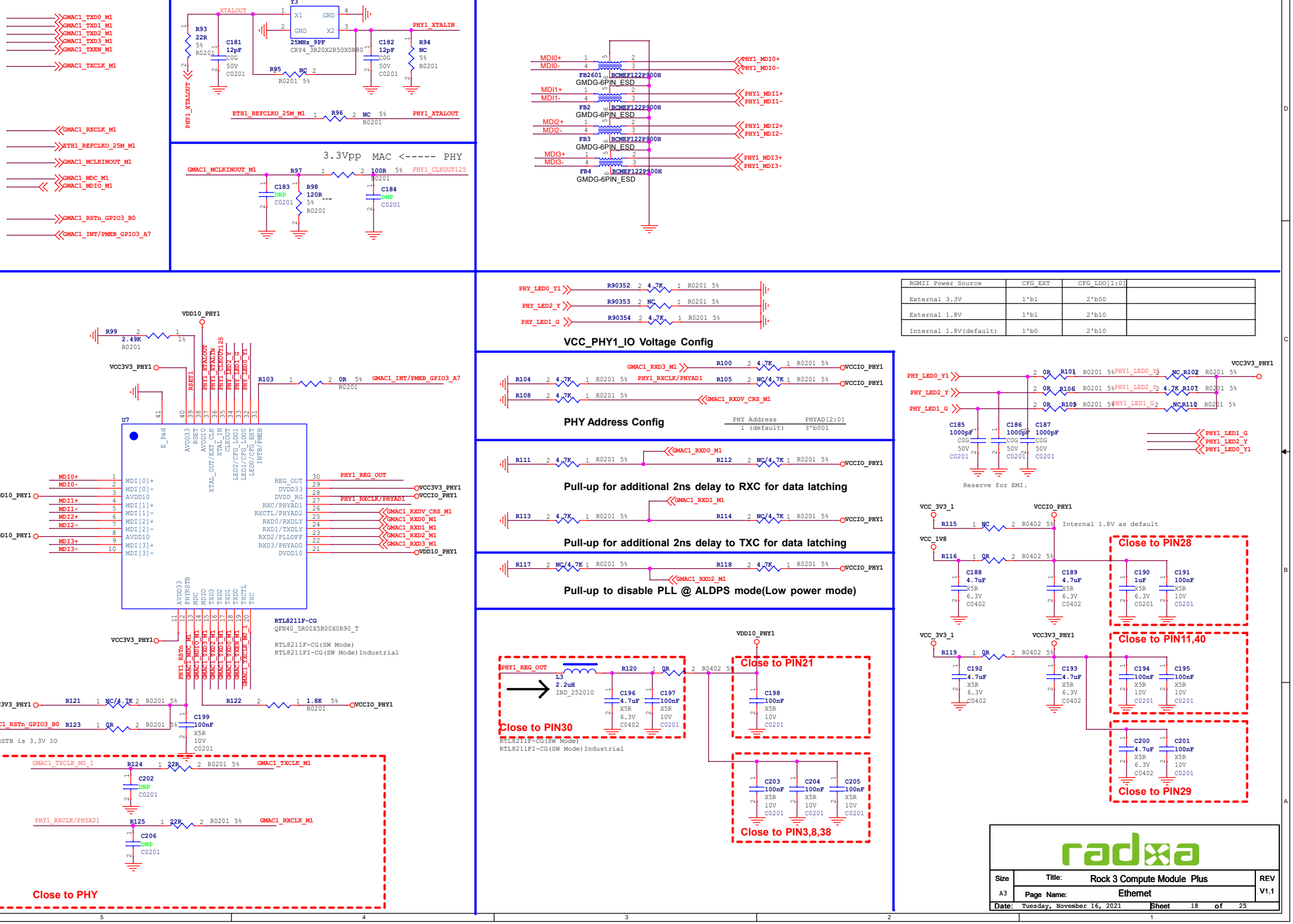
Note:
Yes: option circuit be mounted
No: option circuit not be mounted

Size A3	Title: Rock 3 Compute Module Plus	REV V1.1
	Page Name: WIFI/BT	
Date: Tuesday, November 16, 2021	Sheet 16 of 25	

eMMC FLASH



Size: A4	Title: Rock 3 Compute Module Plus	REV: V1.1
	Page Name: Memory-eMMC	
Date: Tuesday, November 16, 2021	Sheet 17 of 25	


GMAC1_TXD0_M1
GMAC1_TXD1_M1
GMAC1_TXD2_M1
GMAC1_TXD3_M1
GMAC1_TXEN_M1
GMAC1_TXCLK_M1
GMAC1_RXCLK_M1
ETH1_REFCLKO_25M_M1
GMAC1_MCLKINOUT_M1
GMAC1_MDC_M1
GMAC1_MDIO_M1
GMAC1_RSTn_GPIO3_B0
GMAC1_INT/PMEB_GPIO3_A7
Y3
25MHz_9PF
CRY4_3R20X2R50X0R80
R93 22R
C181 12pF
R95 NC
C182 12pF
R94 NC
PHY1_XTALIN
PHY1_XTALOUT
R96 NC
3.3Vpp MAC <----- PHY
R97 100R
C183 DNP
R98 120R
C184 DNP
PHY1_CLKOUT125
MDI0+
MDI0-
MDI1+
MDI1-
MDI2+
MDI2-
MDI3+
MDI3-
FB2601 BCMEF122P900H GMDG-6PIN_ESD
FB2 BCMEF122P900H GMDG-6PIN_ESD
FB3 BCMEF122P900H GMDG-6PIN_ESD
FB4 BCMEF122P900H GMDG-6PIN_ESD
PHY1_MDI0+
PHY1_MDI0-
PHY1_MDI1+
PHY1_MDI1-
PHY1_MDI2+
PHY1_MDI2-
PHY1_MDI3+
PHY1_MDI3-
VDD10_PHY1
VCC3V3_PHY1
R99 2.49K
R103 0R
U7
E_Pad
RSET1
PHY1_REG_OUT
PHY1_RXCLK/PHYAD1
GMAC1_RXDV_CRS_M1
GMAC1_RXD0_M1
GMAC1_RXD1_M1
GMAC1_RXD2_M1
GMAC1_RXD3_M1
RTL8211F-CG
QFN40_5R00X5R00X0R90_T
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
VCCIO_PHY1
R121 NC/4.7K
R122 1.8K
R123 0R
C199 100nF
PHYRSTB is 3.3V IO
GMAC1_TXCLK_M0_1
R124 22R
C202 DNP
PHY1_RXCLK/PHYAD1
R125 22R
C206 DNP
GMAC1_TXCLK_M1
GMAC1_RXCLK_M1
Close to PHY
PHY_LED0_Y1
PHY_LED2_Y
PHY_LED1_G
R90352 4.7K
R90353 NC
R90354 4.7K
VCC_PHY1_IO Voltage Config
R100 4.7K
R104 4.7K
R105 NC/4.7K
R108 4.7K
PHY Address Config
PHY Address PHYAD[2:0]
1 (default) 3'b001
R111 4.7K
Pull-up for additional 2ns delay to RXC for data latching
R112 NC/4.7K
R113 4.7K
R114 NC/4.7K
Pull-up for additional 2ns delay to TXC for data latching
R117 NC/4.7K
R118 4.7K
Pull-up to disable PLL @ ALDPS mode(Low power mode)
L3 2.2uH IND_252010
R120 0R
C196 4.7uF
C197 100nF
C198 100nF
Close to PIN30
Close to PIN21
C203 100nF
C204 100nF
C205 100nF
Close to PIN3,8,38
RGMII Power Source | CFG_EXT | CFG_LDO[1:0]
External 3.3V | 1'b1 | 2'b00
External 1.8V | 1'b1 | 2'b10
Internal 1.8V(default) | 1'b0 | 2'b10
R101 0R
R102 NC
R106 0R
R107 4.7K
R109 0R
R110 NC
C185 1000pF
C186 1000pF
C187 1000pF
Reserve for EMI.
VCC_3V3_1
VCCIO_PHY1
VCC_1V8
R115 NC
R116 0R
Internal 1.8V as default
C188 4.7uF
C189 4.7uF
C190 1uF
C191 100nF
Close to PIN28
R119 0R
C192 4.7uF
C193 4.7uF
C194 100nF
C195 100nF
Close to PIN11,40
C200 4.7uF
C201 100nF
Close to PIN29
radxa
Size A3
Title: Rock 3 Compute Module Plus
REV V1.1
Page Name: Ethernet
Date: Tuesday, November 16, 2021
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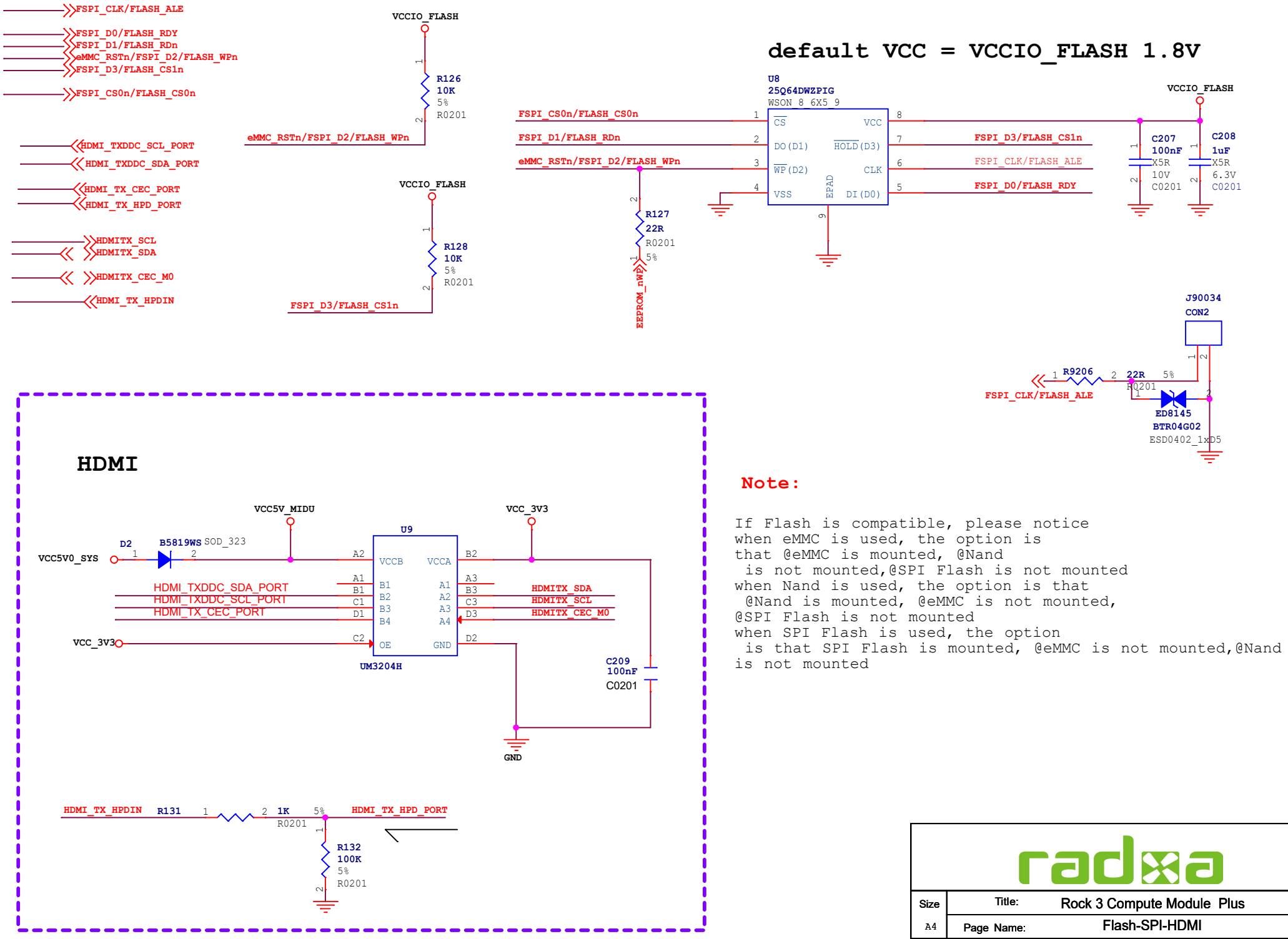
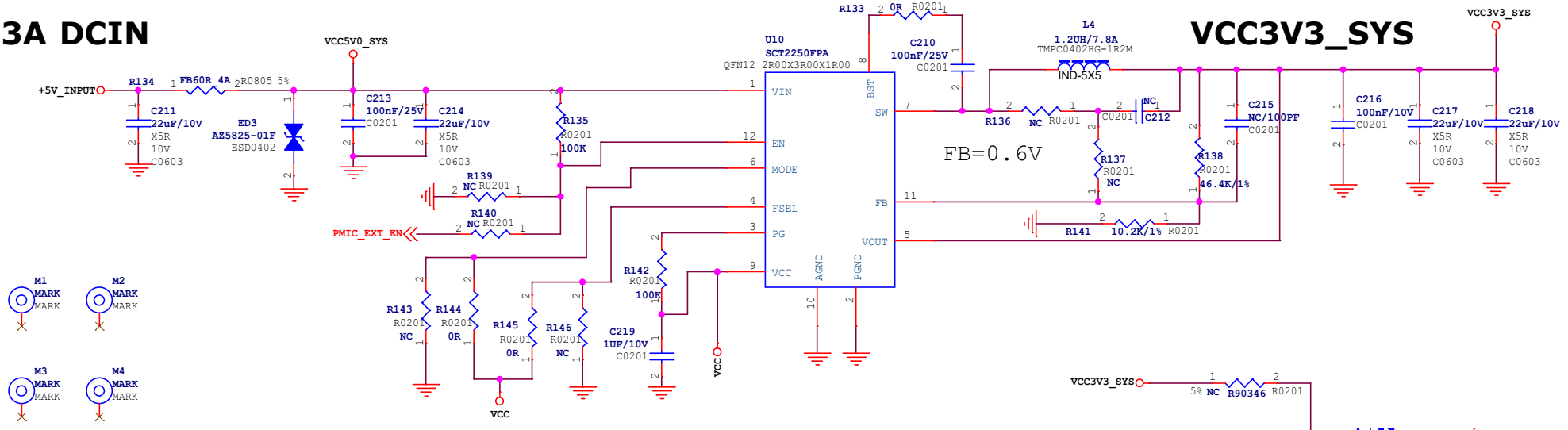


Note:

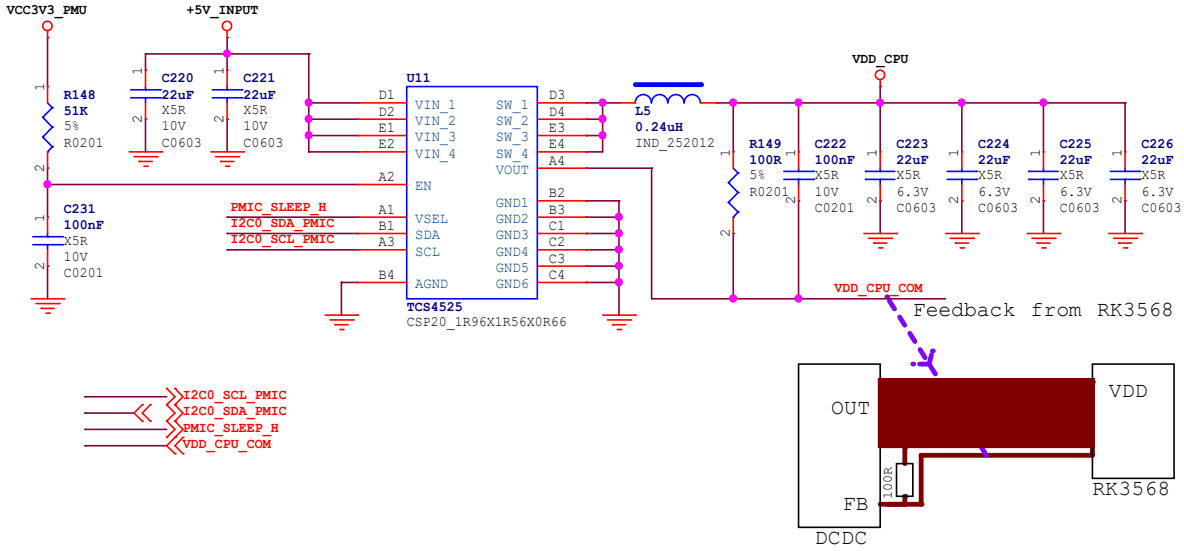
If Flash is compatible, please notice
when eMMC is used, the option is
that @eMMC is mounted, @Nand
is not mounted,@SPI Flash is not mounted
when Nand is used, the option is that
@Nand is mounted, @eMMC is not mounted,
@SPI Flash is not mounted
when SPI Flash is used, the option
is that SPI Flash is mounted, @eMMC is not mounted,@Nand
is not mounted

Size A4	Title: Rock 3 Compute Module Plus Page Name: Flash-SPI-HDMI	REV V1.1
Date: Tuesday, November 16, 2021	Sheet 19 of 25	

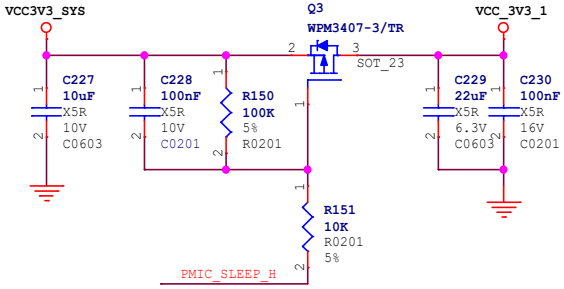
5V/3A DCIN



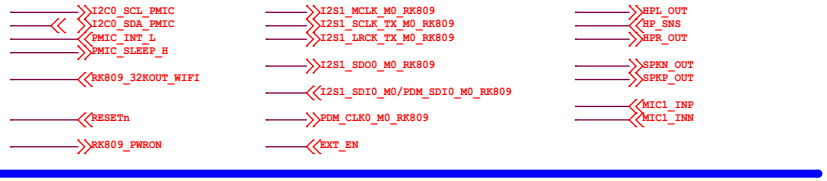
VDD_CPU

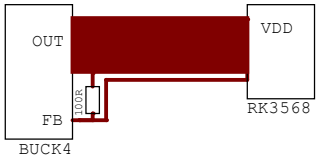


VCC_3V3 (Power OFF under SLEEP)

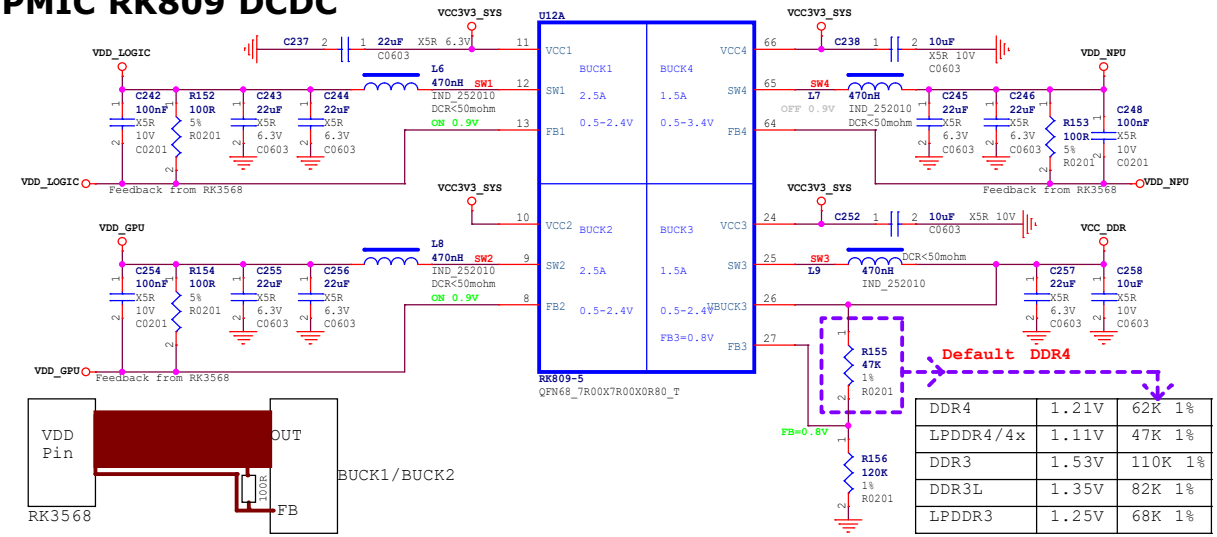


Size: Custom	Title: Rock 3 Compute Module Plus		REV: V1.1
	Page Name: Power_DC IN		
Date: Tuesday, November 16, 2021		Sheet 20 of 25	





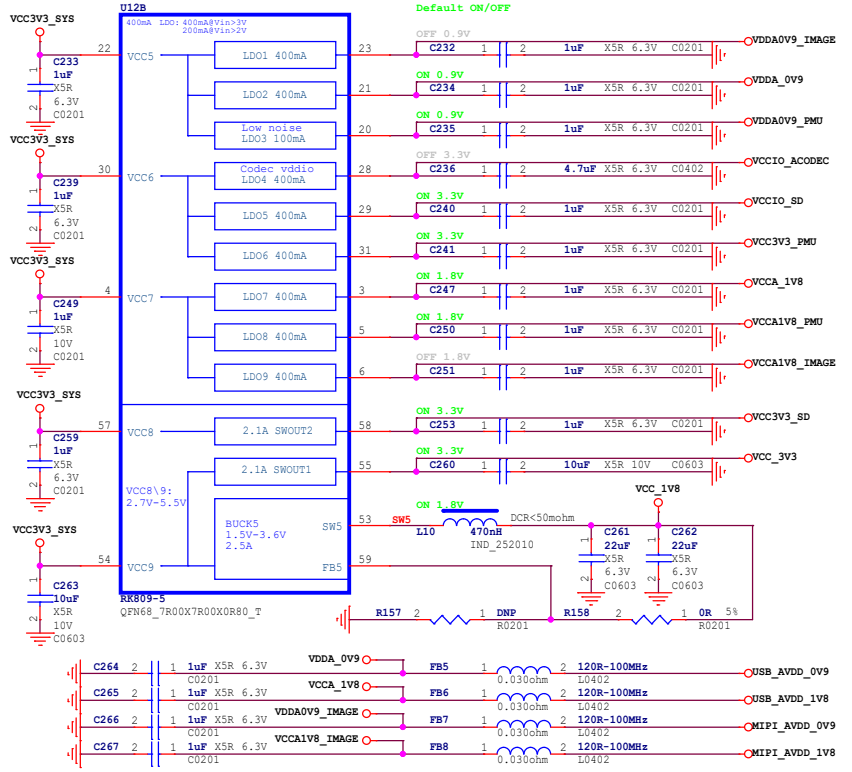
PMIC RK809 DCDC



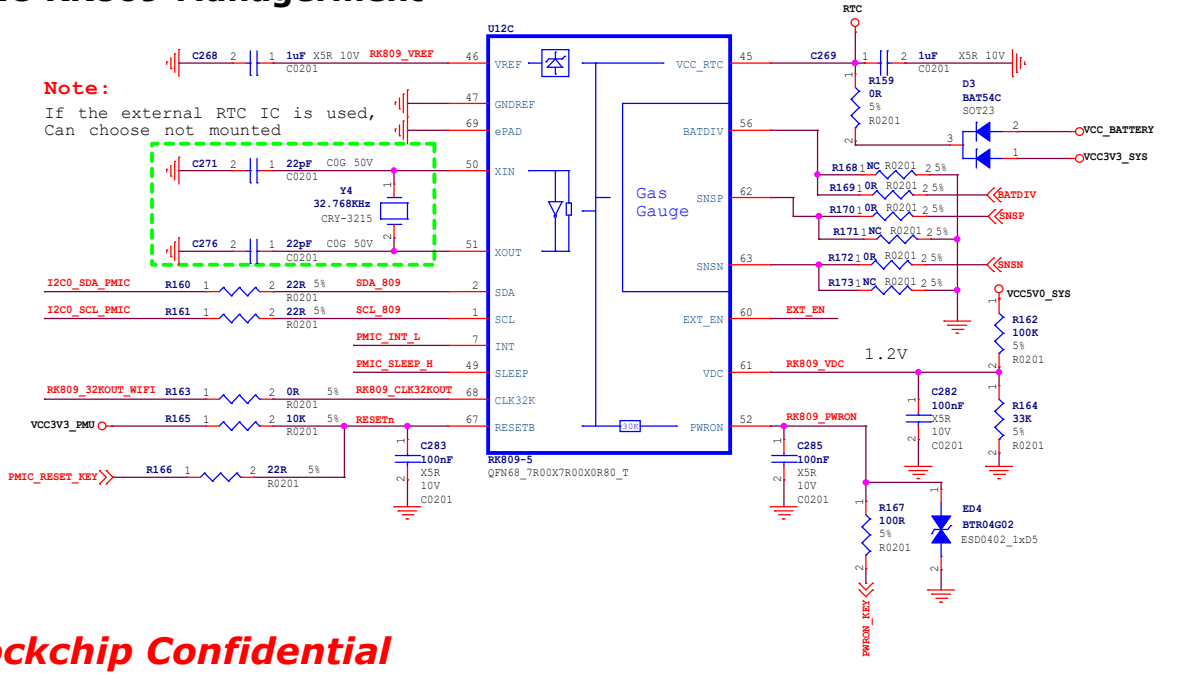
Default DDR4

DDR4	1.21V	62K 1%
LPDDR4/4x	1.11V	47K 1%
DDR3	1.53V	110K 1%
DDR3L	1.35V	82K 1%
LPDDR3	1.25V	68K 1%

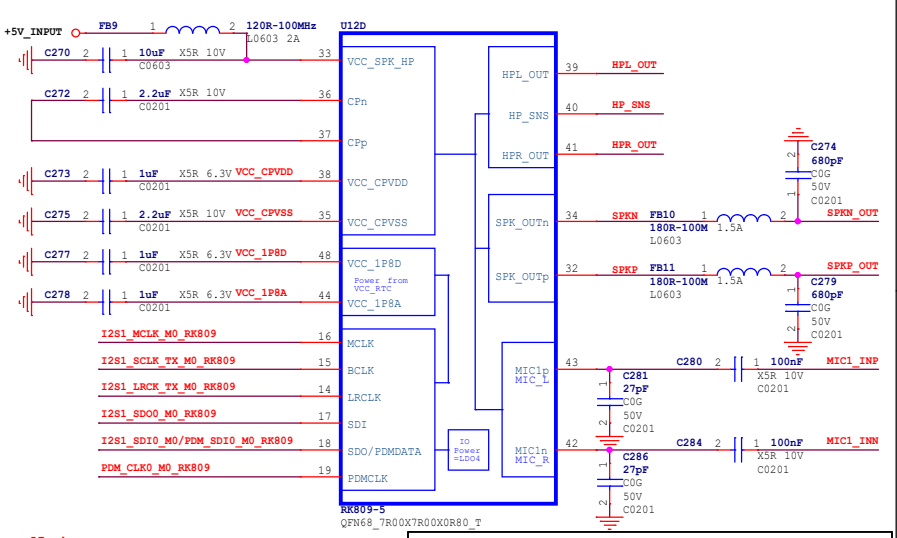
PMIC RK809 LDO



PMIC RK809 Management



PMIC RK809 CODEC



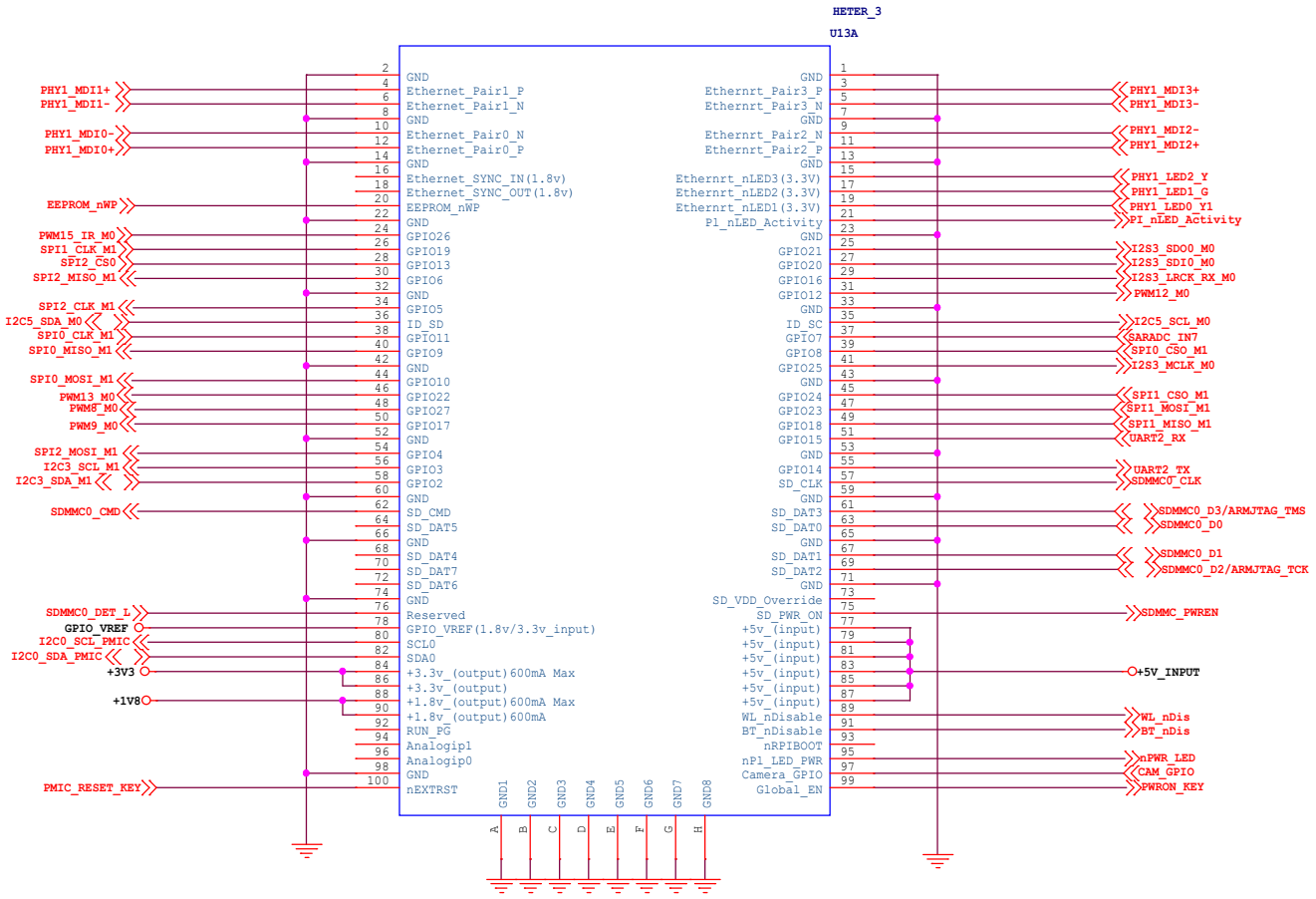
Note:

If RK809-5 codec is not used,
then Pin 14,15,16,17,19,40 Tie VSS
Pin 18,36,37,38,35,39,41,34,32,43,42
Leave floating

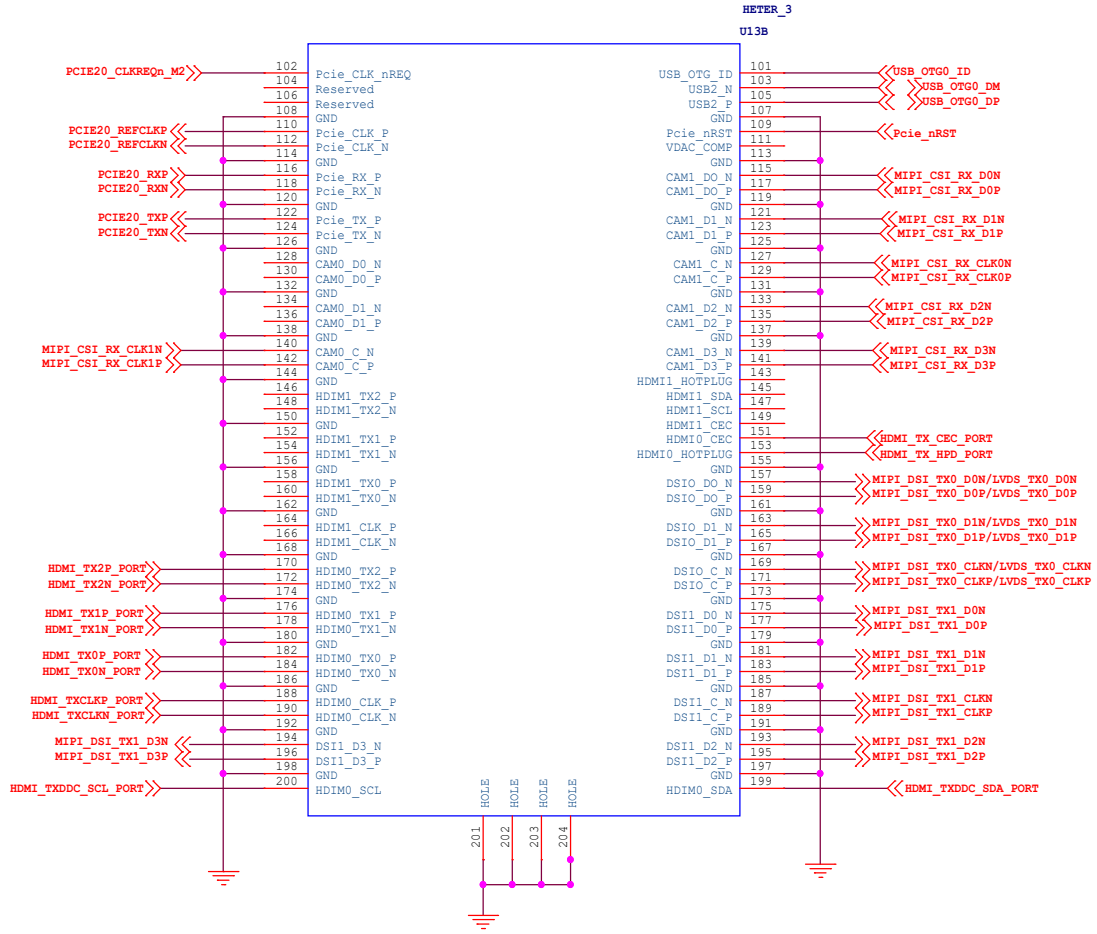
Rockchip Confidential

radxa

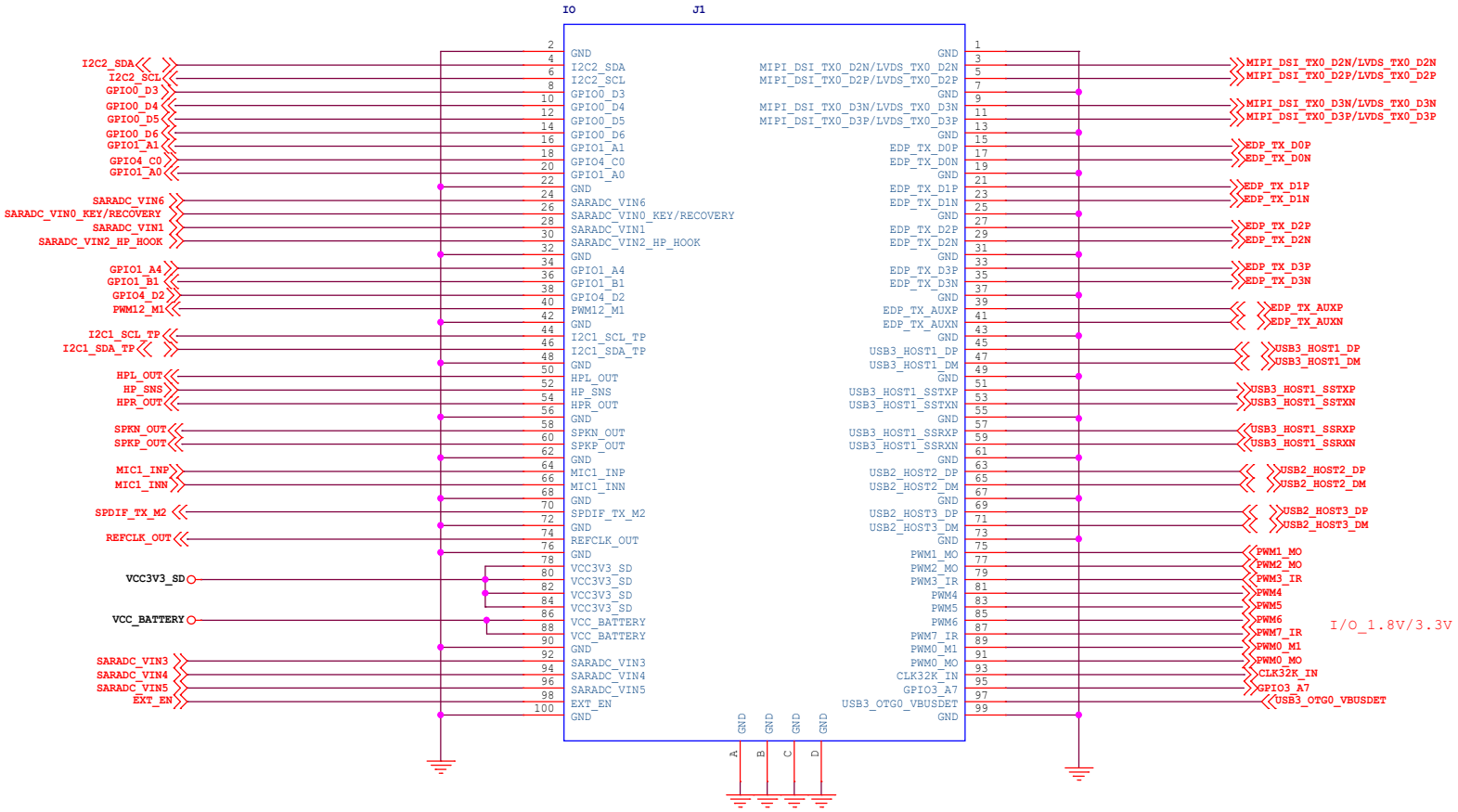
Size A3	Title: Rock 3 Compute Module Plus		REV V1.1
	Page Name: Power_PMIC		
Date: Tuesday, November 16, 2021	Sheet 21 of 25		



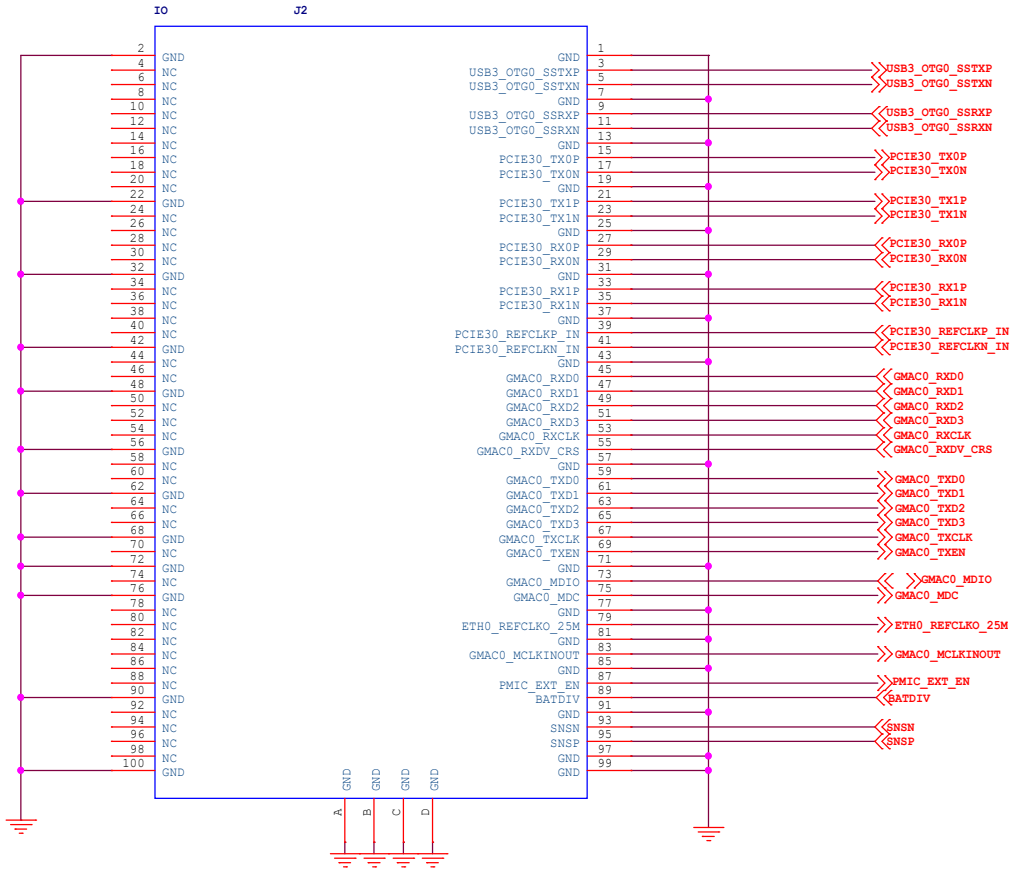
Size: B	Title: Rock 3 Compute Module Plus	REV: V1.1
	Page Name: GPIO+VCC_Connector	
Date: Tuesday, November 16, 2021	Sheet 22 of 25	



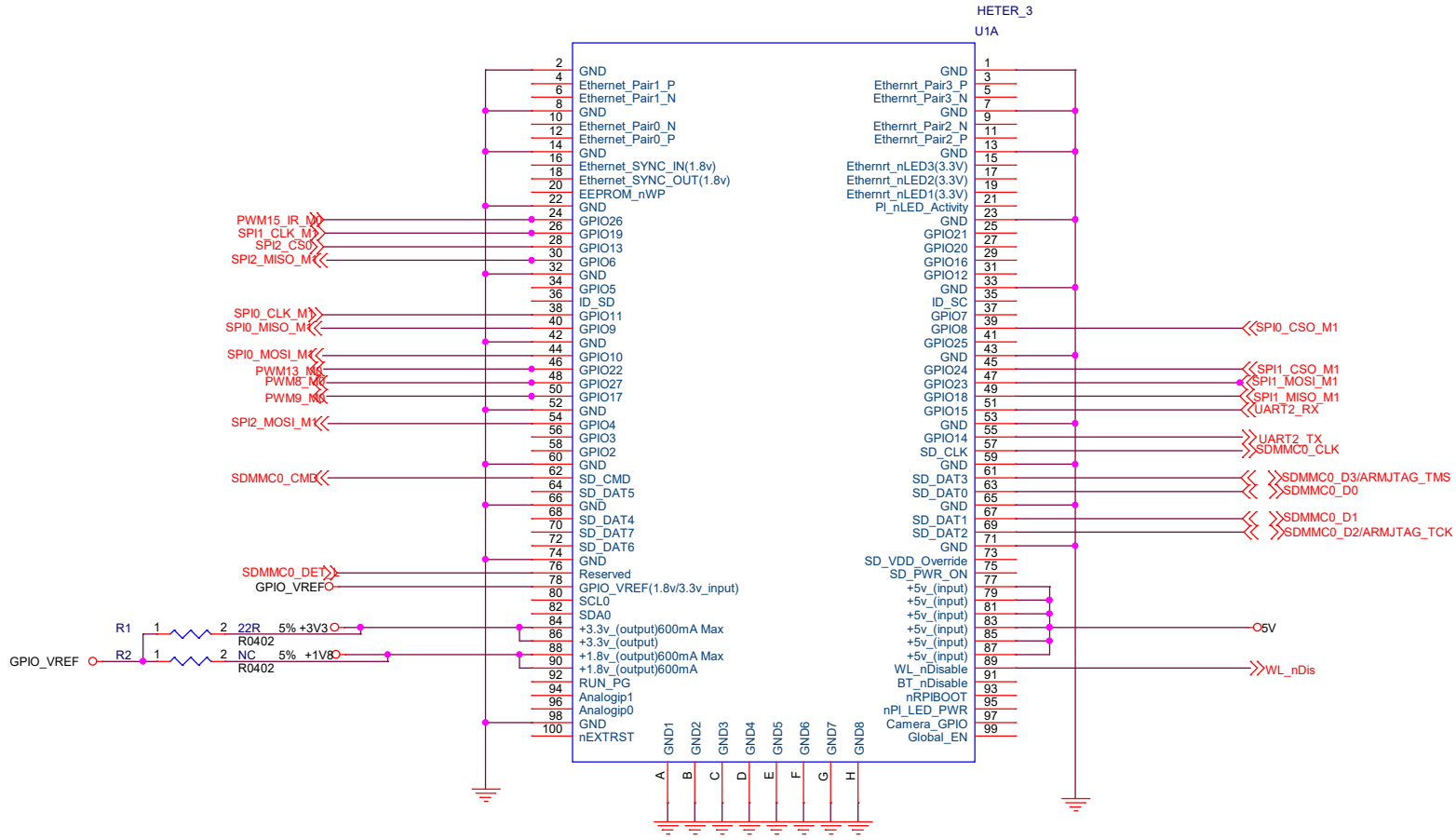
Size: B	Title: Rock 3 Compute Module Plus	REV: V1.1
	Page Name: High Speed Serial_Connector	
Date: Tuesday, November 16, 2021	Sheet 23 of 25	



Size: B	Title: Rock 3 Compute Module Plus	REV: V1.1
	Page Name: IO_Connector	
Date: Tuesday, November 16, 2021	Sheet 24 of 25	

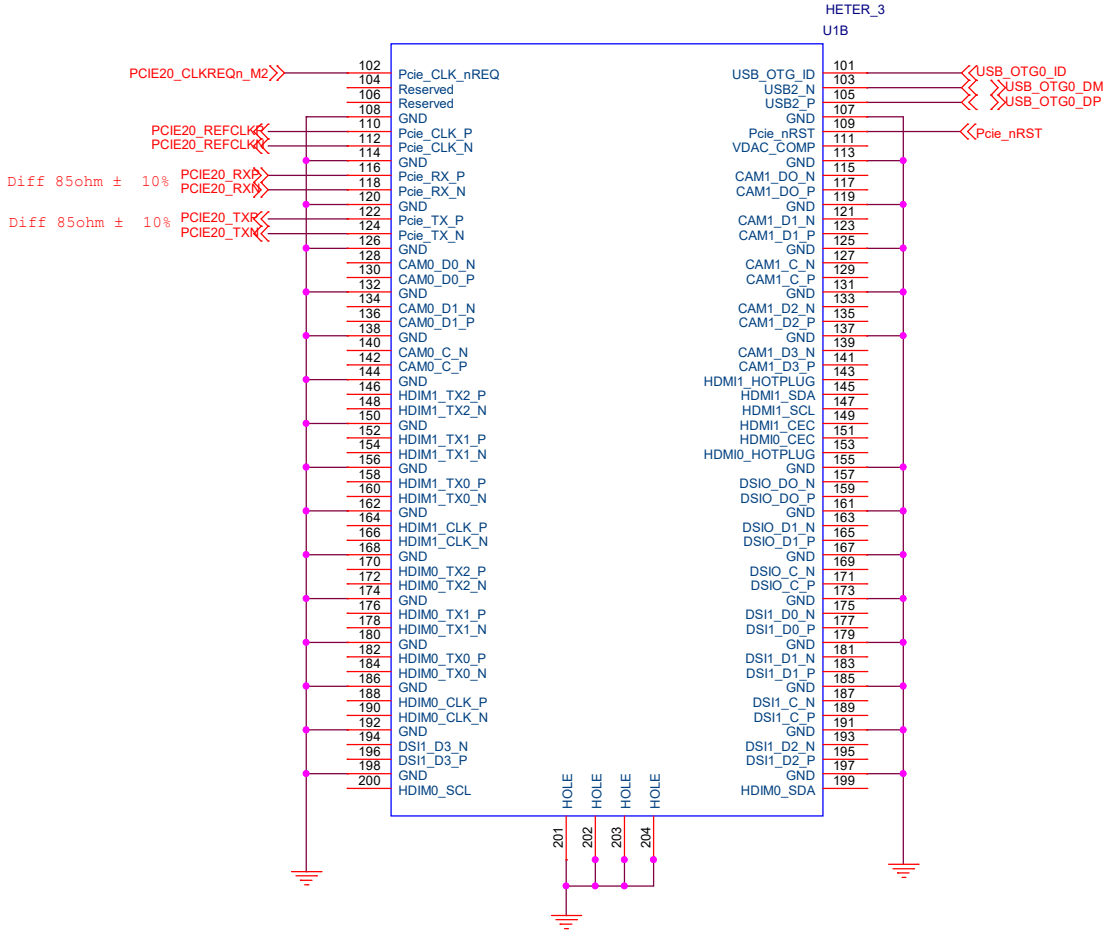


Size: B	Title: Rock 3 Compute Module Plus	REV: V1.1
	Page Name: IO2_Connector	
Date: Tuesday, November 16, 2021	Sheet 25 of 25	

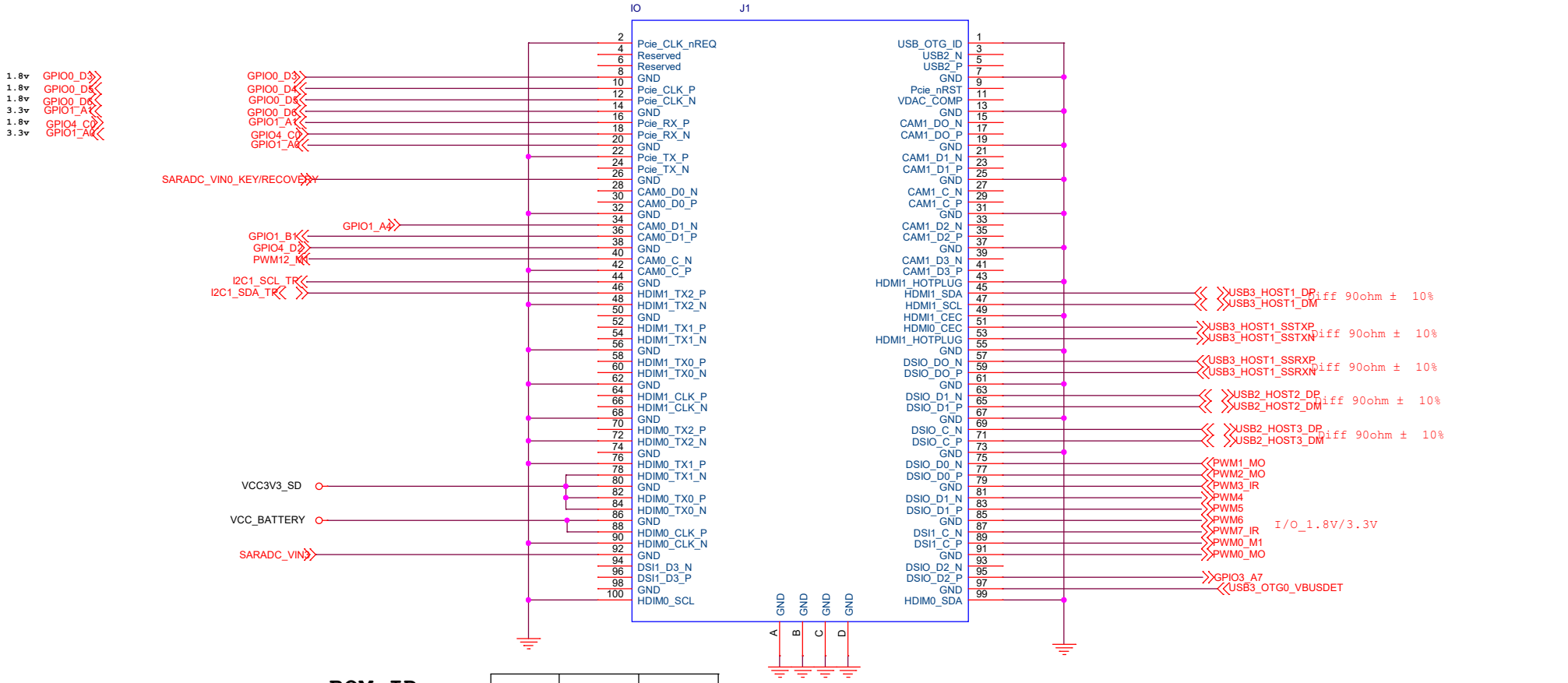


radxa

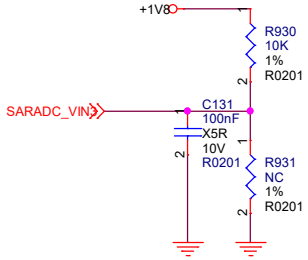
Size	Title:	Radxa_E25	REV
B	Page Name:	GPIO+VCC_Connector	v1.3
Date:	Thursday, January 13, 2022	Sheet 1 of 11	



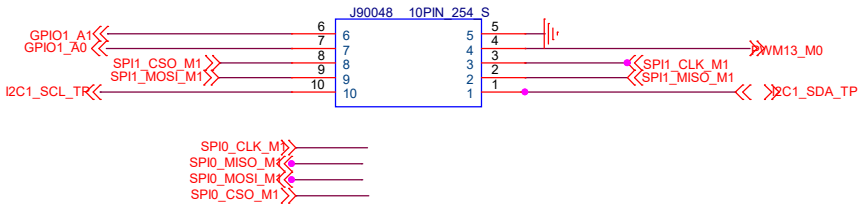
Size	Title: Radxa_E25	REV v1.3
B	Page Name: High Speed Serial_Connector	
Date: Thursday, January 13, 2022	Sheet 2 of 11	



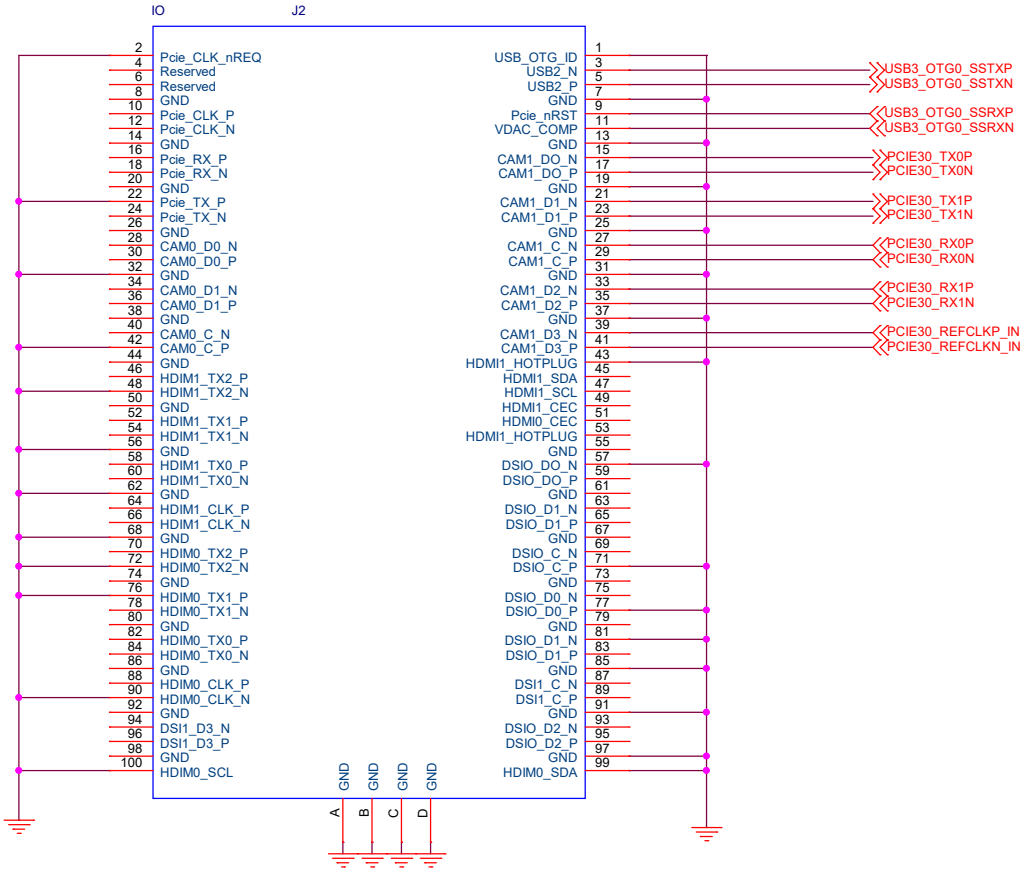
BOM_ID



SARADC_VIN3	Up Resistance	Down Resistance
BOM_ID0	10K	DNP
BOM_ID1	10K	110K
BOM_ID2	20K	100K
BOM_ID3	33K	100K
BOM_ID4	18K	36K
BOM_ID5	36K	51K
BOM_ID6	51K	51K
BOM_ID7	51K	36K
BOM_ID8	36K	18K
BOM_ID9	100K	33K
BOM_ID10	100K	20K
BOM_ID11	110K	10K
BOM_ID12	DNP	10K



Size	Title:	Radxa_E25	REV
	Page Name:	03.IO_Connector	v1.3
Date:	Thursday, January 13, 2022	Sheet 3 of 11	



Size: B	Title: Radxa_E25	REV: v1.3
	Page Name: 04.IO2_Connector	
Date: Thursday, January 13, 2022	Sheet 4 of 11	

RTL8125B(S)_BG 0.95V
RTL8111K 1.0V

For RTL8125B(S)_BG
* Place C3, C4 2.2uF close to AVDD33 pin -- 19, 33
For RTL8111K
* Place C2 0.1uF close to AVDD33 pin -- 19
* Place C4 4.7uF close to AVDD33 pin -- 19

For RTL8125B(S)_BG
L6 =330ohm Bead
For RTL8111K
L6=0R,CS1=NC

20191112
R86 stuff bead

For RTL8125B(S)_BG
* Place C14 to C15 close to DVDD33 pin -- 29, 46
For RTL8111K
* Place C14 close to DVDD33 pin -- 29
* Leave C15 NC

Reserved
RTL8111K 1.0V source @ SWR mode
RTL8125BS 0.95V source

For RTL8111K:
STUFF 0.1uF,UNSTUFF 4.7uF

20191112
Add C75 C76

For RTL8125B(S)_Bg Only
* Place C25 close to AVDD33_XTAL pin -- 34

For RTL8125B(S)_BG
* Place C12 1uF to C13 close to EVDD09 pin -- 37
For RTL8111K
* Place C12 0.1uF to C13 close to EVDD10 pin -- 37

20191112
C913 Unstuff

20191112
C916 stuff 1uF

NC for RTL8111K

For RTL8125B(S)_BG
* Leave R2 NC and connect R3
* Place C17 1uF close to EVDD33 pin -- 43
For RTL8111K
* Leave R3 NC and connect R2
* Place C17 0.1uF close to DVDD10 pin -- 43

For RTL8125B(S)_BG
* Place C9 to C10 10uF close to DVDD09 pin -- 8, 28
* Place C11 2.2uF close to DVDD09 pin -- 47
For RTL8111K
* Place C9 0.1uF close to DVDD10 pin -- 8
* Leave C10 to C11 NC

For RTL8111K only
* Place C16 close to DVDD10 pin -- 40

R9 and R59
for RTL8125B(S)_BG only

For RTL8125B_BG
* Leave R17 to R18 NC
For RTL8125BS
* R17 for Enable SWR
* R18 for Disable SWR
For RTL8111K
* R17 for SWR mode
* R18 for LDO mode

VDD09/VDD10

Reserved
RTL8111K 1.0V source @ LDO mode
RTL8125BS(S) leave R4 and C22 NC

RTL8111K 1.0V source @ SWR mode
RTL8125BS 0.95V source
Remove when NOT using switching regulator

LAN_EXT_CORE

RTL8125B(S)
RTL8125BG
(RTL8111K)

NA

R26 R25 4.7K/5% GPI/GPO
R28 R27 4.7K/5% LANWAKEB
R29 R29 4.7K/5% LED1/EESK/SPISCK

RTL8125B(S)_BG Only
R29 PU for normal application

For RTL8125B(S)_BG & RTL8111K
*, R26 is needed for ensuring IC latch to normal operation mode.

EEPROM Option
For RTL8125B(S)_BG & RTL8111K

TWSI
EEPROM
93C56/66
93C46

For RTL8125B(S)_BG
* R48 for TWSI
R49 for EEROM
For RTL8111K
* Connect R49 and leave R48 NC

TVS for Surge Improvement

ESDLC0545D-HAF
U4
U5

for External Clock Source

Clock Source

must be use SMD type XTAL for RTL8125B(S)

For RTL8125B(S)_BG
* R27 is based on the XTAL drive level spec to choose the appropriate resistor. Do not cascade R25 on CKXTAL1 patch.
For RTL8111K
* R25 is based on the XTAL drive level spec to choose the appropriate resistor. Do not cascade R27 on CKXTAL2 patch.

PCIE 2.0

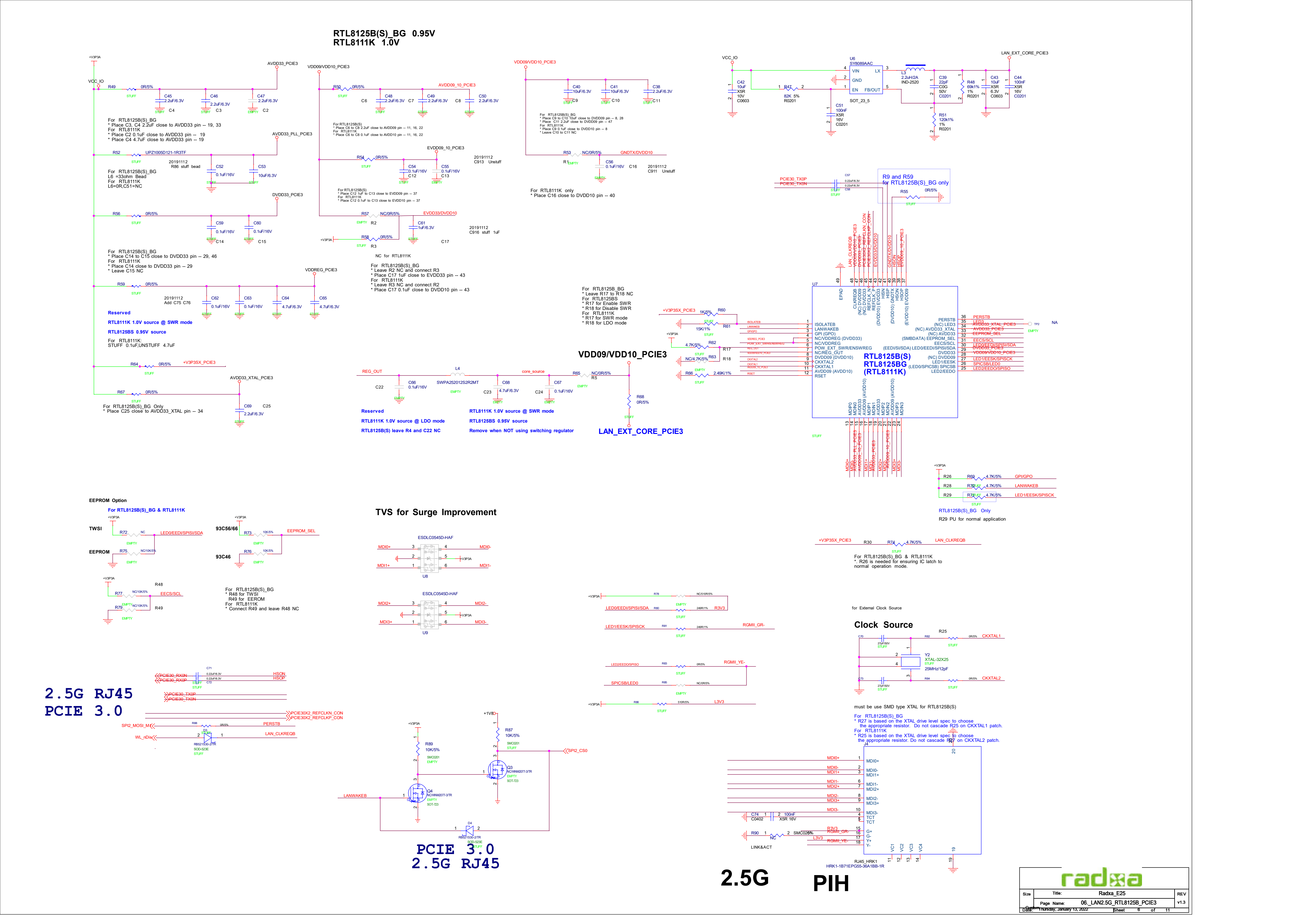
2.5G

PIH

LINK&ACT

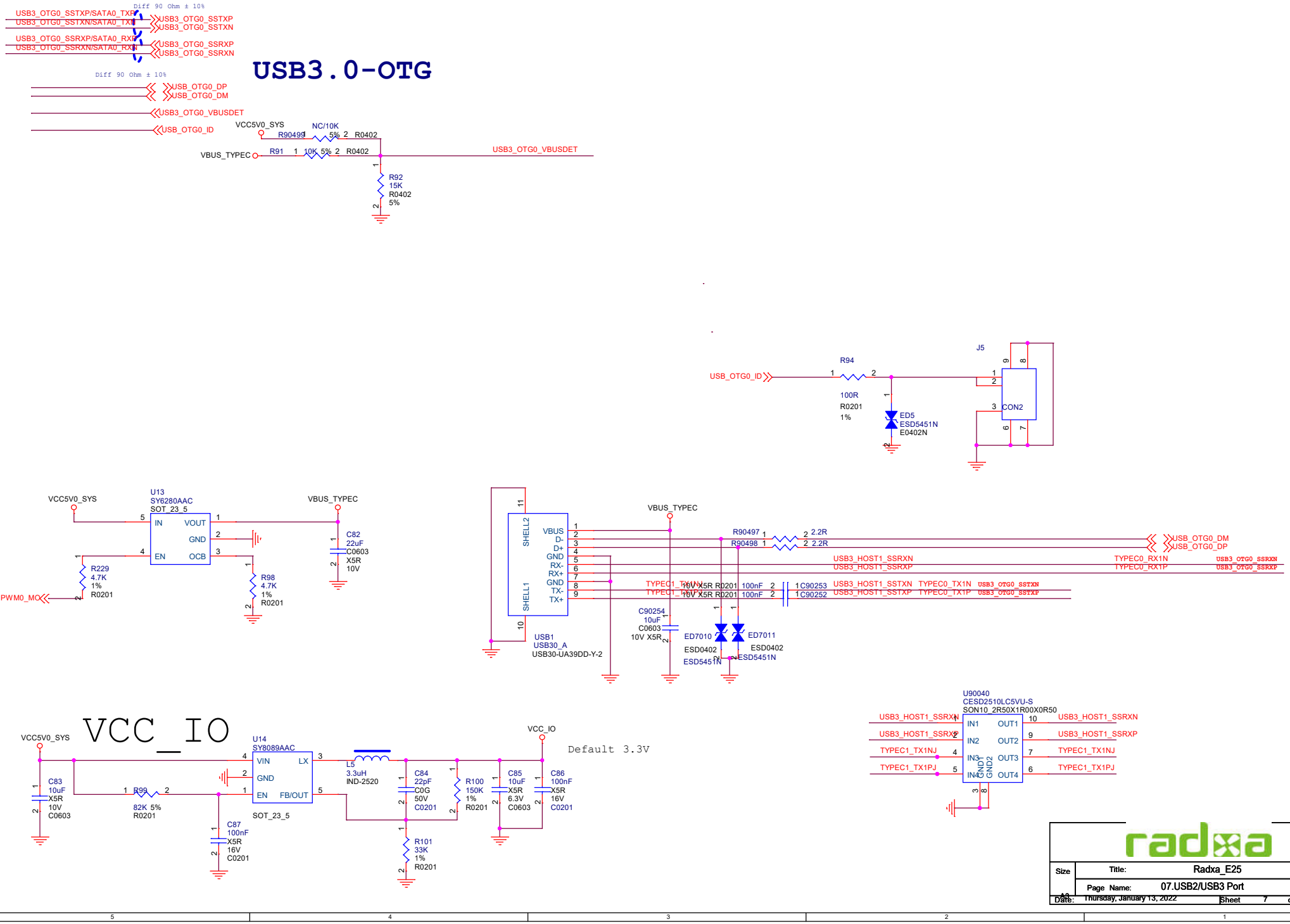
RJ45_HRK1
HRK-1B71EPG55-36A1BB-1R

Size	Title: Radxa_E25		REV
	Page Name: 05_LAN2.5G_RTL8125B_PCIE2		v1.3
Date: Thursday, January 13, 2022	Sheet 5 of 11		



RTL8125B(S)_BG 0.95V
RTL8111K 1.0V
AVDD33_PCIE3
VDD09/VDD10_PCIE3
VDD09/VDD10_PCIE3
VCC_IO
LAN_EXT_CORE_PCIE3
For RTL8125B(S)_BG
* Place C3, C4 2.2uF close to AVDD33 pin -- 19, 33
For RTL8111K
* Place C2 0.1uF close to AVDD33 pin -- 19
* Place C4 4.7uF close to AVDD33 pin -- 19
AVDD33_PLL_PCIE3
For RTL8125B(S)_BG
L6 =33ohm Bead
For RTL8111K
L6=0R,C51=NC
DVDD33_PCIE3
For RTL8125B(S)_BG
* Place C14 to C15 close to DVDD33 pin -- 29, 46
For RTL8111K
* Place C14 close to DVDD33 pin -- 29
* Leave C15 NC
VDDREG_PCIE3
Reserved
RTL8111K 1.0V source @ SWR mode
RTL8125BS 0.95V source
For RTL8111K:
STUFF 0.1uF,UNSTUFF 4.7uF
+V3P3SX_PCIE3
AVDD33_XTAL_PCIE3
For RTL8125B(S)_BG Only
* Place C25 close to AVDD33_XTAL pin -- 34
For RTL8111K only
* Place C16 close to DVDD10 pin -- 40
NC for RTL8111K
For RTL8125B(S)_BG
* Leave R2 NC and connect R3
* Place C17 1uF close to EVDD33 pin -- 43
For RTL8111K
* Leave R3 NC and connect R2
* Place C17 0.1uF close to DVDD10 pin -- 43
For RTL8125B_BG
* Leave R17 to R18 NC
For RTL8125BS
* R17 for Enable SWR
* R18 for Disable SWR
For RTL8111K
* R17 for SWR mode
* R18 for LDO mode
R9 and R59
for RTL8125B(S)_BG only
RTL8125B(S)
RTL8125BG
(RTL8111K)
REG_OUT
core_source
Reserved
RTL8111K 1.0V source @ LDO mode
RTL8125B(S) leave R4 and C22 NC
RTL8111K 1.0V source @ SWR mode
RTL8125BS 0.95V source
Remove when NOT using switching regulator
LAN_EXT_CORE_PCIE3
RTL8125B(S)_BG Only
R29 PU for normal application
For RTL8125B(S)_BG & RTL8111K
*. R26 is needed for ensuring IC latch to normal operation mode.
EEPROM Option
For RTL8125B(S)_BG & RTL8111K
TWSI
EEPROM
93C56/66
93C46
For RTL8125B(S)_BG
* R48 for TWSI
R49 for EEROM
For RTL8111K
* Connect R49 and leave R48 NC
TVS for Surge Improvement
ESDLC0545D-HAF
for External Clock Source
Clock Source
must be use SMD type XTAL for RTL8125B(S)
For RTL8125B(S)_BG
* R27 is based on the XTAL drive level spec to choose the appropriate resistor. Do not cascade R25 on CKXTAL1 patch.
For RTL8111K
* R25 is based on the XTAL drive level spec to choose the appropriate resistor. Do not cascade R27 on CKXTAL2 patch.
2.5G RJ45
PCIE 3.0
PCIE 3.0
2.5G RJ45
RJ45_HRK1
HRK1-1B71EPG55-36A1BB-1R
LINK&ACT
2.5G
PIH
radxa
Title: Radxa_E25
Page Name: 06._LAN2.5G_RTL8125B_PCIE3
REV v1.3
Date: Thursday, January 13, 2022
Sheet 6 of 11

USB3.0-OTG



Size	Title: Radxa_E25	REV v1.3
	Page Name: 07.USB2/USB3 Port	
Date: Thursday, January 13, 2022	Sheet 7 of 11	

SATA

Default

Diff 90 Ohm ± 10%

USB3_HOST1_SSTXP/SATA1_TXP
USB3_HOST1_SSTXN/SATA1_TXN
USB3_HOST1_SSRXP/SATA1_RXP
USB3_HOST1_SSRXN/SATA1_RXN

USB3_HOST1_SSTXP
USB3_HOST1_SSTXN
USB3_HOST1_SSRXP
USB3_HOST1_SSRXN

GPIO0_D4
R102 510R 5% R0402
LED1 LED_RED LED0603 SATA1_ACT_LED

USB2_HOST2_DM
USB2_HOST2_DP
HOST_DM1
HOST_DP1

SATA3.0 Port1 Option

And USB3 HOST1 option, Can support SATA1+USB2 HOST1

USB3_HOST1_SSTXP/SATA1_TXP	SATA1_TXP	C89	2 10nF X7R 10V C0201		SATA1TXP
USB3_HOST1_SSTXN/SATA1_TXN	SATA1_TXN	C88	2 10nF X7R 10V C0201		SATA1TXN
USB3_HOST1_SSRXP/SATA1_RXP	SATA1_RXN	C90	2 10nF X7R 10V C0201	Diff 100 Ohm ± 10%	SATA1RXN
USB3_HOST1_SSRXN/SATA1_RXN	SATA1_RXP	C91	2 10nF X7R 10V C0201		SATA1RXP

NOTES:
1:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.
2:10nF close to connector

KEY B

U90047 M2-KEY-B

PCIE M.2 NGFF B-KEY SOCKET

CONFIG_3	GND13	VBAT1	VCC3V3_PCIE30X1
GND14	USB_D+	VBAT2	VCC3V3_PCIE30X1
USB_D-	GND20	FULL_CARD_PWR_OFF#	4G_PWREN 1.8v
		W_DISABLE1#	4G_DISABLE 3.3v
		LED1#	
CONFIG_0	WoWWAN#	DPR	GND9
U3_TX-	U3_TX+	GND8	U3_RX-
U3_RX+	GND7	PERn0/SATA-B+	PERp0/SATA-B-
GND6	PETn0/SATA-A-	PETp0/SATA-A+	GND5
REFCLKN	REFCLKP	GND4	ANTCTL0
ANTCTL1	LAA_TX_EN	WL_TX_EN	RESET#
CONFIG_1	GND3	GND2	CONFIG_2
GND16	GND15		
I2S_CLK	I2S_TXD	I2S_RXD	W_DISABLE2
I2S_WA	SIM1_RESET	SIM1_CLK	SIM1_DATA
SIM1_PWR	DEVSLP ssd sleep mode		
I2C_SCL	SIM2_DET	SIM2_DATA	SIM2_CLK
SIM2_RESET	SIM2_PWR	PERST#	CLKREQ#
PEWAKE#	RFFE_SCLK	RFFE_SDATA	I2S_MCLK
COEX2	COEX1	SIM1_DET	I2C_SDA
VBAT3	VBAT4	VBAT5	

HOST_DP1
HOST_DM1
1.8v 4G_WAKE_ON_HOST
SATA1RXP
SATA1RXN
SATA1TXN
SATA1TXP
1.8v 4G_RESET

Active high signal used by the platform to put the SSD in Sleep mode

VCC3V3_PCIE30X1
R90518 510R 5% R0402
LED3 LED_RED LED0603 SATA1_ACT_LED

+3V3
R90519 0R R0603 5%
C90283 10uF X5R 10V C0603
C90282 4.7uF/16V C0603
SIM-PWR

1.8v GPIO0_D3 4G_WAKE_ON_HOST
1.8v GPIO0_D5 4G_RESET
1.8v GPIO0_D6 4G_PWREN
3.3v GPIO0_D7 4G_DISABLE
3.3v PWM8_M0 DEVSLP
1.8v GPIO4_C0 W_DISABLE2

SIM1_RESET
SIM1_CLK
SIM1_DATA
SIM1_PWR
R90617 15K
SIM1_DET

R90617 0R SIM-CLK
R90618 0R SIM-DATA
R90619 0R SIM-RESET
R90620 0R SIM-PWR
R90621 0R SIM-DET

U90048 NANO_SIM2

SIM2-CLK
SIM2-DATA
SIM2-RESET
SIM2-PWR
SIM2-DET

R90622 0R SIM-CLK
R90623 0R SIM-DATA
R90624 0R SIM-RESET
R90625 0R SIM-PWR
R90626 0R SIM-DET

ED8124 ESD9B5V
ED8125 ESD9B5V
ED8122 ESD9B5V

SDMMC0_D0
SDMMC0_D1
SDMMC0_D2
SDMMC0_D3
SDMMC0_CMD
SDMMC0_CLK
SDMMC_PWR

[9] SDMMC0_D2/ARMJTAG_TCK
[9] SDMMC0_D3/ARMJTAG_TMS
[9] SDMMC0_CMD
[9] SDMMC0_CLK
[9] SDMMC0_D0
[9] SDMMC0_D1
PWM9_M0

R4200 22R 5% R0201
R4201 22R 5% R0201
R4202 22R 5% R0201
R4203 22R 5% R0201
R4204 22R 5% R0201
R4205 22R 5% R0201

VCC3V3_SD
R90615 10k 5% R0201

D4200 ESD5341N ESD0402
D4201 ESD5341N ESD0402
D4202 ESD5341N ESD0402
D4203 ESD5341N ESD0402
D4204 ESD5341N ESD0402
D4205 ESD5341N ESD0402
D4206 ESD5341N ESD0402

U90049 TFCARD-SOCKET

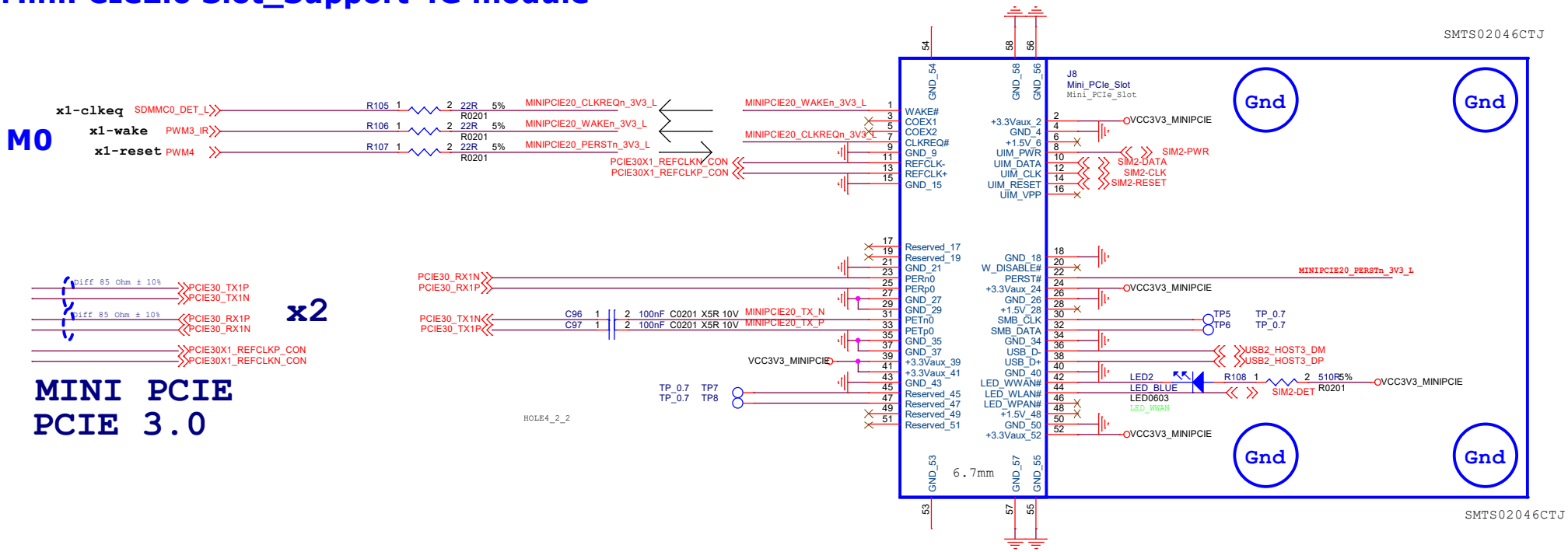
DATA2
CD/DATA3
CMD
VDD
CLK
VSS
DATA0
DATA1
CD

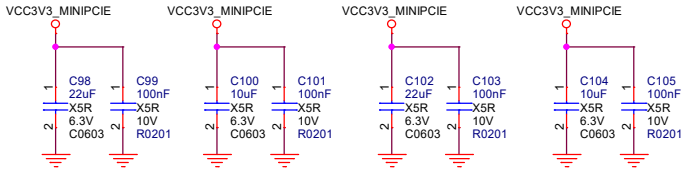
C122 10uF X5R 10V C0603
C123 100nF X5R 10V R0201
R145 10K 5% R0201 DNP

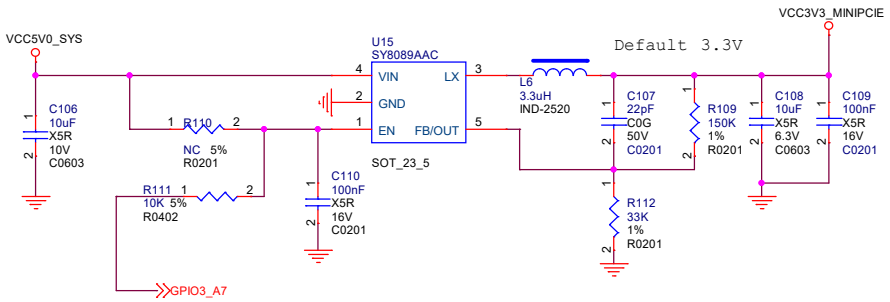
Close to MicroSD Card

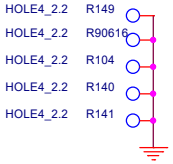
Size	Title: Radxa_E25		REV v1.3
A3	Page Name: 08.KEY-B-4G-sata		
Date: Thursday, January 13, 2022	Sheet 8 of 11		

MiniPCIe2.0 Slot_Support 4G module









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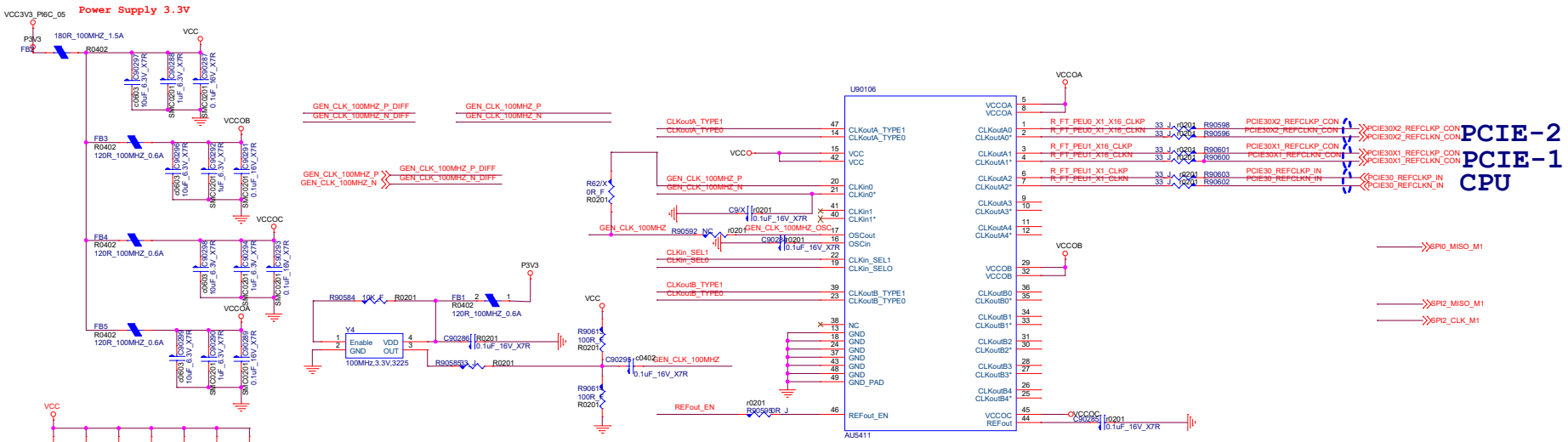
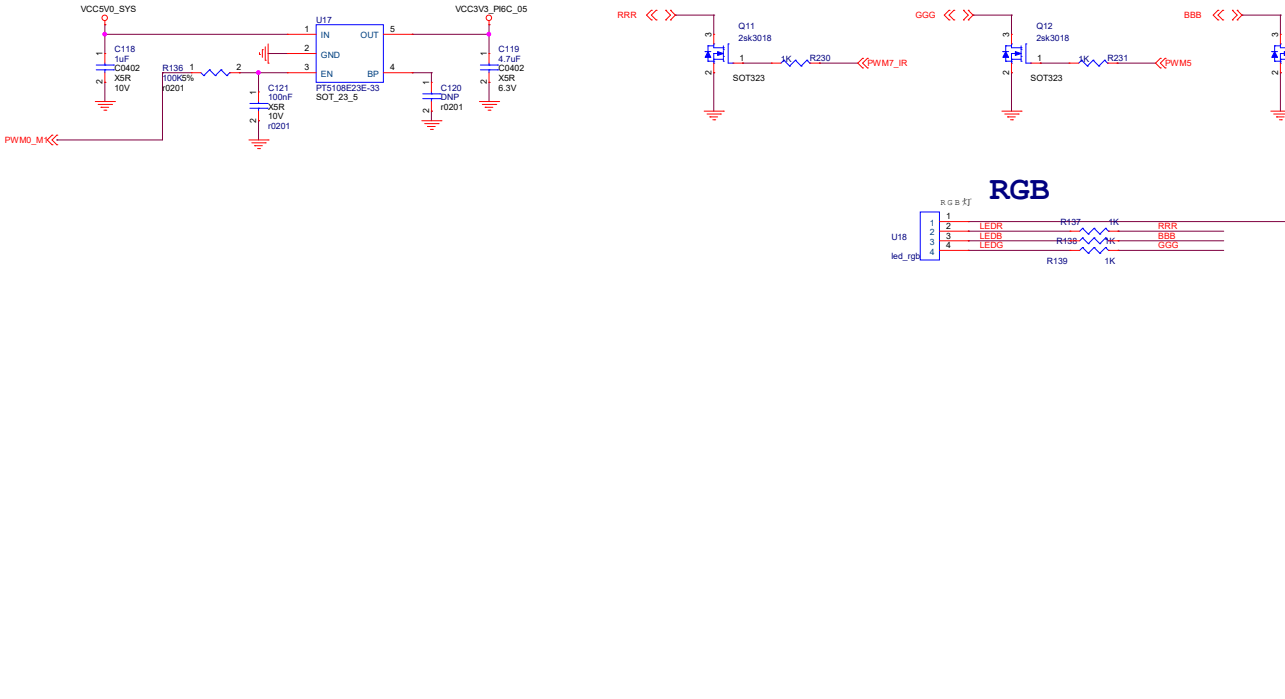
Size	Title: Radxa_E25	REV
A3	Page Name: 09.MiniPCIe	v1.3
Date: Thursday, January 13, 2022	Sheet 9 of 11	

Power Supply 3.3V



Input clock selection		
CLKin_SEL1	CLKin_SEL0	Selected Clock
0	0	CLKin_SEL0
0	1	CLKin_SEL1
1	0	crystal ac
1	1	crystal dc

Programming of Output Driver Type		
Clkoutx-Type1	Clkoutx-Type0	CLK BUFFER TYPE
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	HIZ



RGB

Size	Title: Radxa_E25		REV
A4	Page Name: 10.PCIE-CLK		v1.3
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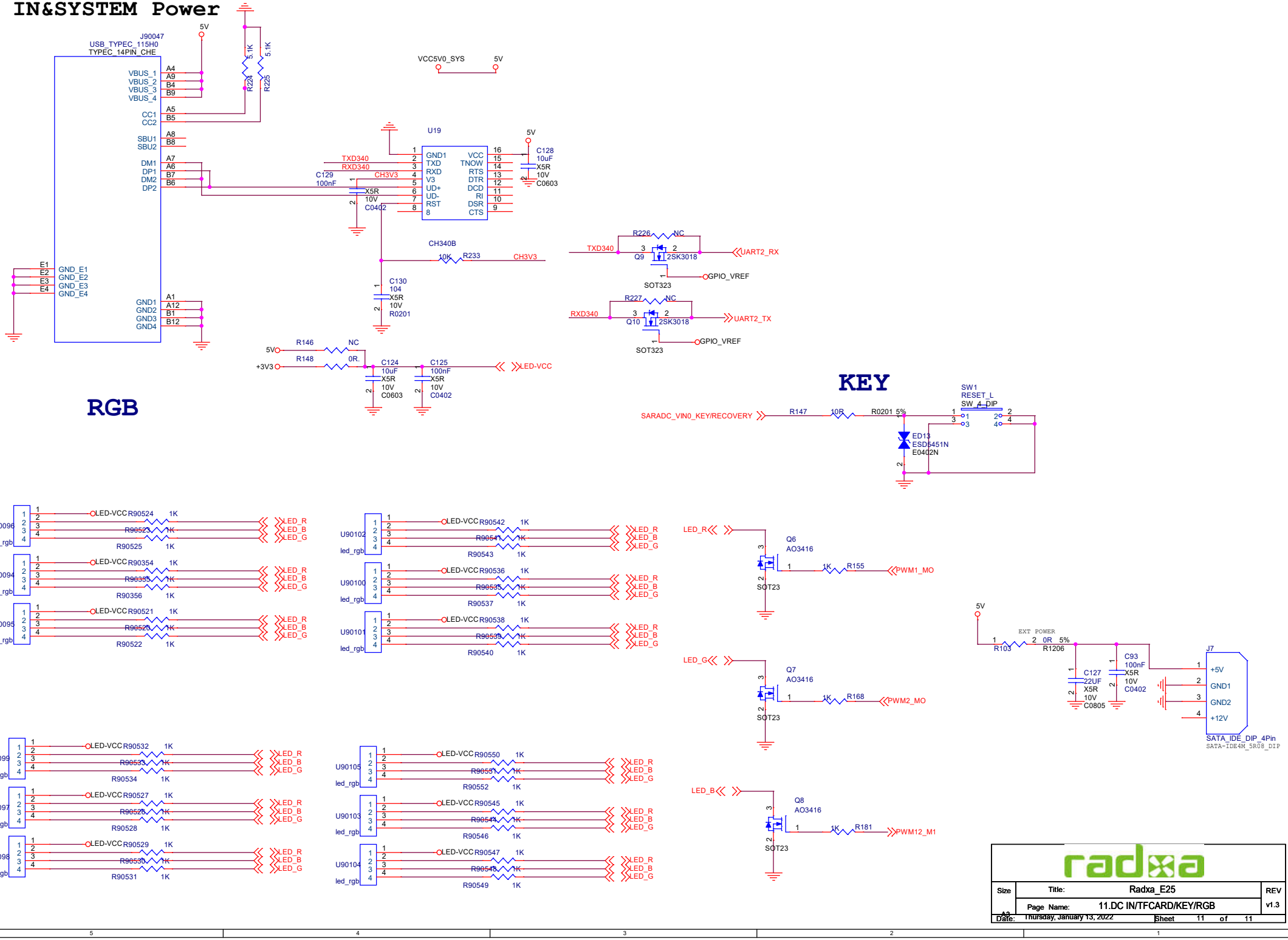
DC IN&SYSTEM Power



Size	Title: Radxa_E25	REV v1.3
A3	Page Name: 11.DC IN/TFCARD/KEY/RGB	
Date: Thursday, January 13, 2022	Sheet 11 of 11	