Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2021-06-01		1:Revision preliminary version	
V1.1	2021-06-29			

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Description

Note

Option

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

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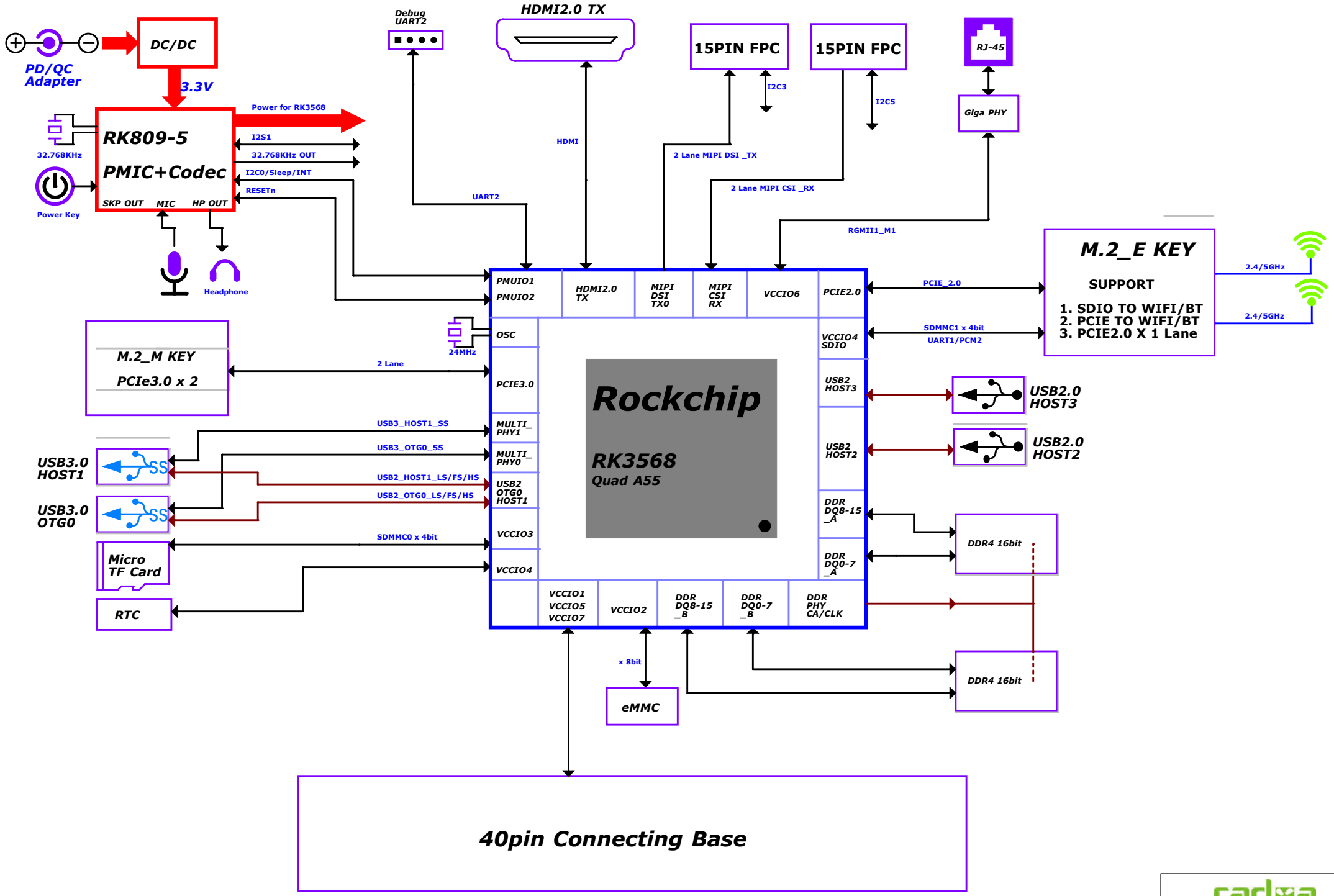
Gong Le Ref Block Diagram



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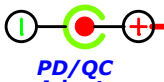
Default Power Diagram



PD/QC Adapter

DC/DC 3000mA Seq:0 Max:

VCC3V3_SYS

RK809-5

Power on Sequence

VCC1	BUCK1 0.5V~2.4V, 2.5A max	Seq:1	VDD_LOGIC Max:	RK3568_Logic
VCC2	BUCK2 0.5V~2.4V, 2.5A max	Seq:2	VDD_GPU Max:	RK3568_GPU
VCC3	BUCK3 0.5V~2.4V, 1.5A max	Seq:3	VCC_DDR Max:	RK3568_DDRC DRAM
VCC4	BUCK4 0.5V~3.4V, 1.5A max	OFF	VDD_NPU Max:	RK3568_NPU
	LDO1 0.6V~3.4V, 400mA max	OFF	VDDA0V9_IMAGE Max:	MIPI_CSI_RX_AVDD_0V9 Max: MIPI_DSI_TX0/LVDS_TX0_AVDD_0V9 Max: MIPI_DSI_TX1_AVDD_0V9 Max: EDP_TX_AVDD_0V9 Max: HDMI_TX_AVDD_0V9 Max:
VCC5	LDO2 0.6V~3.4V, 400mA max	Seq:1	VDDA_0V9 Max:	SYSPLL_AVDD_0V9 Max: USB2_AVDD_0V9 Max: USB3_AVDD_0V9 Max: MULTI_PHY_AVDD_0V9 Max: PCIE30_AVDD_0V9 Max:
	LDO3 0.6V~3.4V, 100mA max	Seq:1	VDDA0V9_PMU Max:	PMU_VDD_LOGIC_0V9 Max: PMUPLL_AVDD_0V9 Max:
	LDO4(Codec VDDIO) 0.6V~3.4V, 400mA max	OFF	VCCIO_ACODEC Max:	VCCIO1--I2S1/PDM MIC/PDM ADC
VCC6	LDO5 0.6V~3.4V, 400mA max	Seq:4	VCCIO_SD Max:	VCCIO3--SDMMC0
	LDO6 0.6V~3.4V, 400mA max	Seq:2	VCC3V3_PMU Max:	PMUIO1/ PMUIO2
	LDO7 0.6V~3.4V, 400mA max	Seq:2	VCCA_1V8 Max:	SYSPLL_AVDD_1V8 Max: USB2_AVDD_1V8 Max: USB3_AVDD_1V8 Max: MULTI_PHY_AVDD_1V8 Max: PCIE30_AVDD_1V8 Max: SARADC_AVDD_1V8 Max:
VCC7	LDO8 0.6V~3.4V, 400mA max	Seq:2	VCCA1V8_PMU Max:	PMUPLL_AVDD_1V8 VCC1V8_DDR
	LDO9 0.6V~3.4V, 400mA max	OFF	VCCA1V8_IMAGE Max:	MIPI_CSI_RX_AVDD_1V8 Max: MIPI_DSI_TX0/LVDS_TX0_AVDD_1V8 Max: MIPI_DSI_TX1_AVDD_1V8 Max: EDP_TX_AVDD_1V8 Max: HDMI_TX_AVDD_1V8 Max: VCC18_LCD(Option) Max:
VCC8	Switch2 2.1 A max, Rdson=100mΩ	Seq:4	VCC3V3_SD Max:	Micro SD Card
	Switch1 2.1 A max, Rdson=90mΩ	Seq:4	VCC_3V3 Max:	USB3_AVDD_3V3 Max: USB2_AVDD_3V3 Max: VCCIO5,VCCIO7 Max: eMMC_VCC / Nand_VCC Max: VCC3V3_PHY0/1/2 Max: VCC3V3_TP Max: IR Receiver Max: UART Device Max: RS485 Device Max: CAN IC Max:
VCC9	BUCK5: 1.5V~3.6V, 2.5 A max	Seq:2	VCC_1V8 Max:	OTP_VCC18 Max: VCCIO2(Default) --eMMC/Nand IO Max: VCCIO4(Default) Max: VCCIO6(Default) Max: GiGa PHY0/1 IO-Option Max: WIFI/BT IO Max:
VCC_RTC				

VCC5V0_SYS

EXT DC/DC ,5A Seq:2A VDD_CPU Max: RK3568_CPU

EXT LDO ,0.3A Seq:2A VCC2V5_DDR Max: DDR4 DRAM

VCC3V3_SYS

- Mos-->LCD Panel Max:
- Mos-->VCC3V3_VGA Max:
- Mos-->RK628D Max:
- WIFI/BT VBAT Max:
- LDO-->Camera 1.2V Max:
- LDO-->Camera 1.8V Max:
- RTC IC Max:

MOS OFF

- PCIe Slot Max:
- SATA Max:

DC/DC 3000mA Seq:0 VCC5V0_USB Max:

- SATA Max:
- USB HOST Max:

DC/DC 3000mA Seq:0 VCC5V0_SYS Max:

- RK809_SPK_PA Max:
- MOS → VCC5V0_VGA Max:
- LDO → VCC3V3_PI6C Max:
- LDO → Camera 2.8V Max:
- DDR VTT Max:
- LCM Backlight Max:
- MOS → VCC5V_HDMI_TX Max:
- CAN transceiver IC Max:
- EXT SPK PA Max:

DC/DC 3000mA VCC3V3_PCIE Max:

DC/DC 3000mA VCC3V3_MINIPCIE Max:

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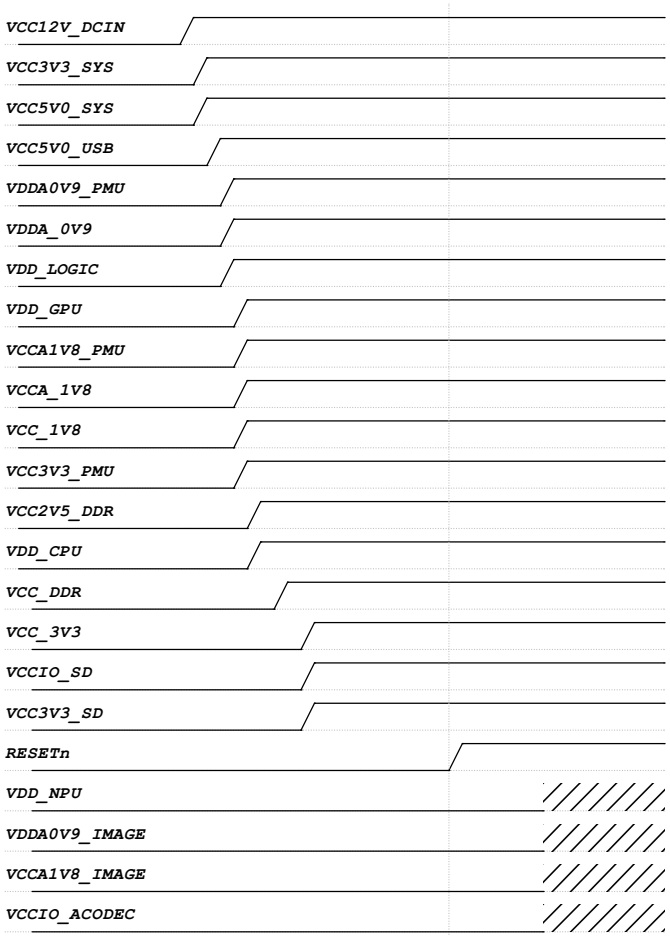
Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC3V3_SYS	RK809_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	0.9V	TBD	TBD
VCC3V3_SYS	RK809_BUCK2	2.5A	VDD_GPU	Slot:2	0.9V	ON	DVFS	TBD	TBD
VCC3V3_SYS	RK809_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	1.2V (DDR4)	TBD	TBD
VCC3V3_SYS	RK809_BUCK4	1.5A	VDD_NPU	N/A	0V	OFF	DVFS	TBD	TBD
VCC3V3_SYS	RK809_LDO1	0.4A	VDDA0V9_IMAGE	N/A	0V	OFF	0.9V	TBD	TBD
	RK809_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	0.9V	TBD	TBD
	RK809_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	0.9V	TBD	TBD
VCC3V3_SYS	RK809_LDO4	0.4A	VCCIO_ACODEC	N/A	0V	OFF	3.3V	TBD	TBD
	RK809_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	3.3V or 1.8V (SD2.0=3.3V,SD3.0=1.8V)	TBD	TBD
	RK809_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	3.3V	TBD	TBD
VCC3V3_SYS	RK809_LDO7	0.4A	VCCA_1V8	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_LDO8	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_LDO9	0.4A	VCCA1V8_IMAGE	N/A	0V	OFF	1.8V	TBD	TBD
VCC3V3_SYS	RK809_SW2 100mohm	2.1A	VCC3V3_SD	Slot:4	3.3V	ON	3.3V	TBD	TBD
VCC3V3_SYS	RK809_SW1 90mohm	2.1A	VCC_3V3	Slot:4	3.3V	ON	3.3V	TBD	TBD
	RK809_BUCK5	2.5A	VCC_1V8	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_RESETn			Slot:4+5					
VCC12V_DCIN	EXT BUCK	3.0A	VCC3V3_SYS	Slot:0	3.3V	ON	3.3V	TBD	TBD
VCC12V_DCIN	EXT BUCK	3.0A	VCC5V0_SYS	Slot:0	5.0V	ON	5.0V	TBD	TBD
VCC5V0_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	DVFS	TBD	TBD
VCC3V3_SYS	EXT LDO	0.3A	VCC2V5_DDR	Slot:2A	2.5V	ON	2.5V	TBD	TBD

Default IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage		Actual assigned IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	Pin Y20	✓	✗	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	Pin W19	✓	✓	VCC3V3_PMU	VCC3V3_PMU	3.3V	
VCCIO1	Pin H17	✓	✓	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	Pin H18	✓	✓	VCCIO_FLASH	VCC_1V8	1.8V	PIN "FLASH_VOL_SEL" must be logic High if VCCIO_FLASH=3.3V,FLASH_VOL_SEL must be logic low
VCCIO3	Pin L22	✓	✓	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	Pin J21	✓	✓	VCCIO4	VCC_1V8	1.8V	
VCCIO5	Pin V10 Pin V11	✓	✓	VCCIO5	VCC_3V3	3.3V	
VCCIO6	Pin R9 Pin U9	✓	✓	VCCIO6	VCC_1V8	1.8V	
VCCIO7	Pin V12	✓	✓	VCCIO7	VCC_3V3	3.3V	

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

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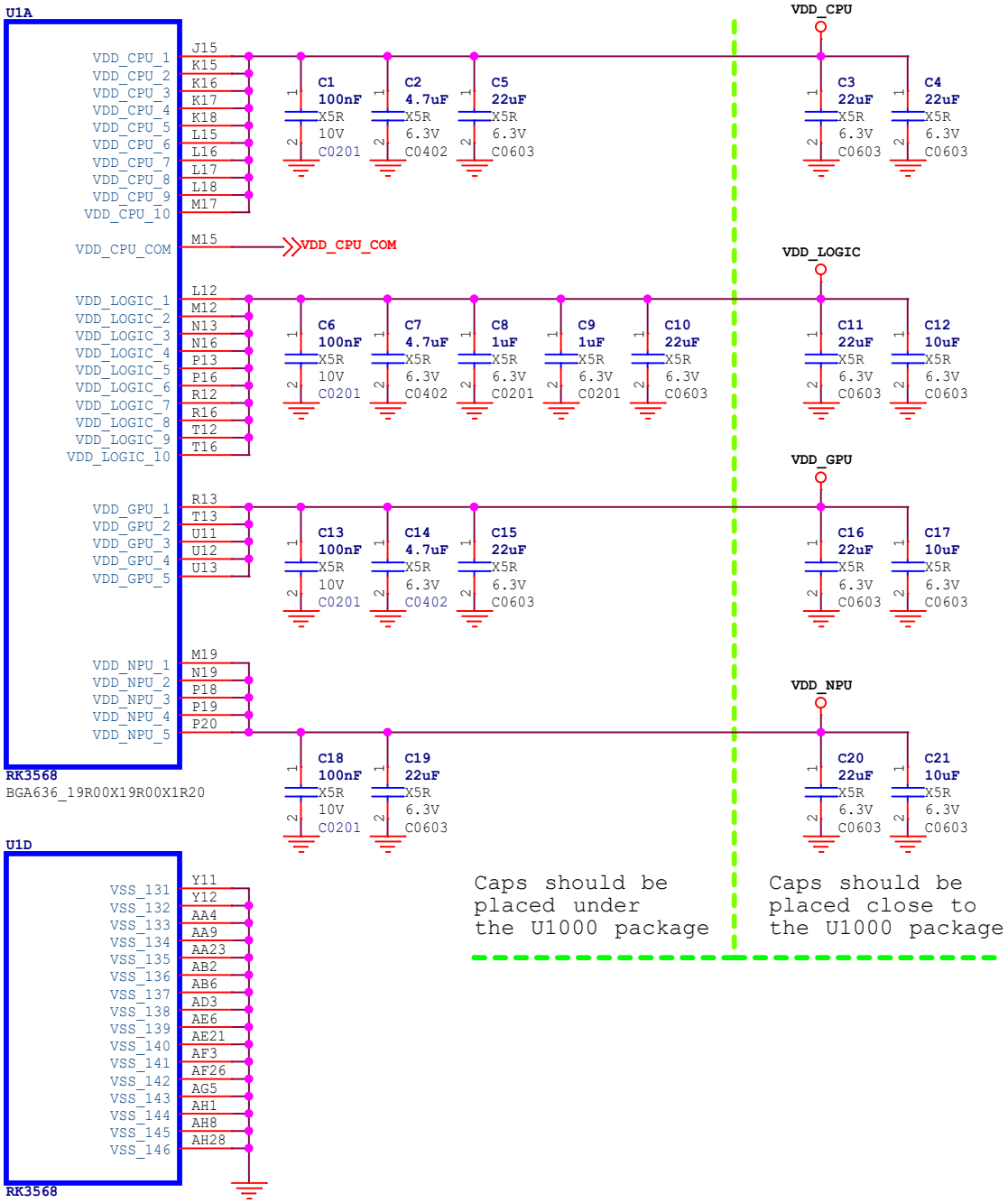
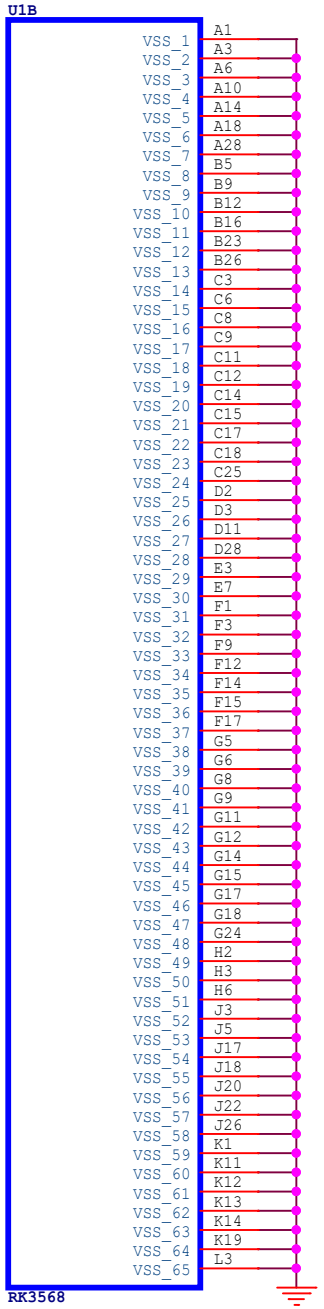
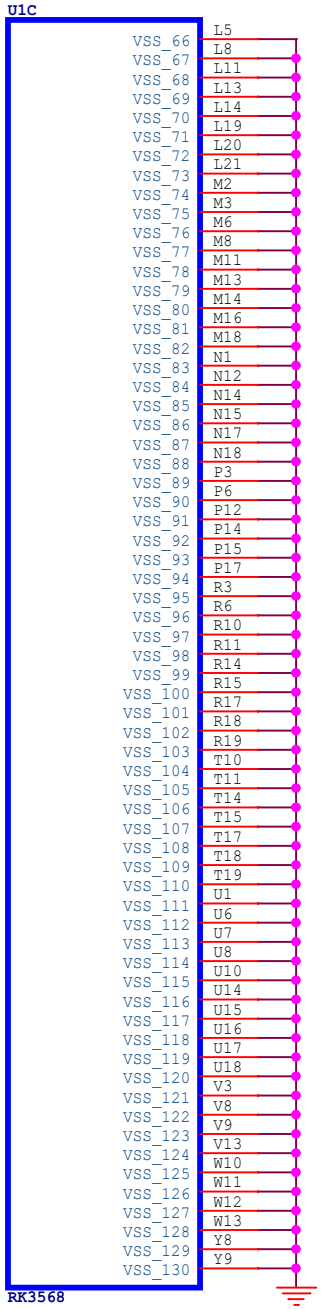
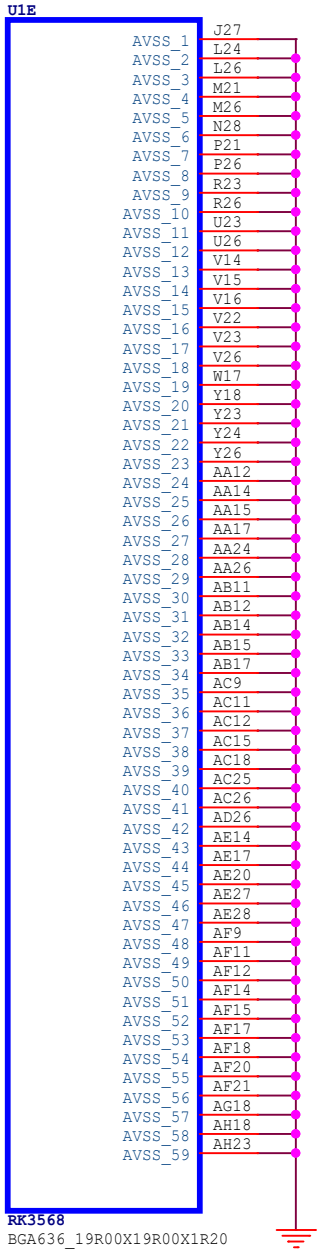
RK3568_ABCDE (Power&Gnd)









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RK3568_F (DDR PHY)

U1F

DDR4	LPDDR4	DDR3	LPDDR3
DDR_DQ0_A	DDR4_DQL0_A	LPDDR4_DQ0_A	DDR3_DQ0	LPDDR3_DQ15
DDR_DQ1_A	DDR4_DQL2_A	LPDDR4_DQ1_A	DDR3_DQ1	LPDDR3_DQ14
DDR_DQ2_A	DDR4_DQL4_A	LPDDR4_DQ2_A	DDR3_DQ2	LPDDR3_DQ10
DDR_DQ3_A	DDR4_DQL6_A	LPDDR4_DQ3_A	DDR3_DQ3	LPDDR3_DQ9
DDR_DQ4_A	DDR4_DQL7_A	LPDDR4_DQ4_A	DDR3_DQ4	LPDDR3_DQ13
DDR_DQ5_A	DDR4_DQL5_A	LPDDR4_DQ5_A	DDR3_DQ5	LPDDR3_DQ12
DDR_DQ6_A	DDR4_DQL3_A	LPDDR4_DQ6_A	DDR3_DQ6	LPDDR3_DQ8
DDR_DQ7_A	DDR4_DQL1_A	LPDDR4_DQ7_A	DDR3_DQ7	LPDDR3_DQ11
DDR_DM0_A	DDR4_DML_A	LPDDR4_DM0_A	DDR3_DM0	LPDDR3_DM1
DDR_DQS0P_A	DDR4_DQSL_P_A	LPDDR4_DQS0P_A	DDR3_DQS0P	LPDDR3_DQS1P
DDR_DQS0N_A	DDR4_DQSL_N_A	LPDDR4_DQS0N_A	DDR3_DQS0N	LPDDR3_DQS1N
DDR_DQ8_A	DDR4_DQU3_A	LPDDR4_DQ8_A	DDR3_DQ8	LPDDR3_DQ25
DDR_DQ9_A	DDR4_DQU1_A	LPDDR4_DQ9_A	DDR3_DQ9	LPDDR3_DQ24
DDR_DQ10_A	DDR4_DQU7_A	LPDDR4_DQ10_A	DDR3_DQ10	LPDDR3_DQ28
DDR_DQ11_A	DDR4_DQU5_A	LPDDR4_DQ11_A	DDR3_DQ11	LPDDR3_DQ29
DDR_DQ12_A	DDR4_DQU2_A	LPDDR4_DQ12_A	DDR3_DQ12	LPDDR3_DQ26
DDR_DQ13_A	DDR4_DQU4_A	LPDDR4_DQ13_A	DDR3_DQ13	LPDDR3_DQ31
DDR_DQ14_A	DDR4_DQU6_A	LPDDR4_DQ14_A	DDR3_DQ14	LPDDR3_DQ30
DDR_DQ15_A	DDR4_DQU0_A	LPDDR4_DQ15_A	DDR3_DQ15	LPDDR3_DQ27
DDR_DM1_A	DDR4_DMU_A	LPDDR4_DM1_A	DDR3_DM1	LPDDR3_DM3
DDR_DQS1P_A	DDR4_DQSU_P_A	LPDDR4_DQS1P_A	DDR3_DQS1P	LPDDR3_DQS3P
DDR_DQS1N_A	DDR4_DQSU_N_A	LPDDR4_DQS1N_A	DDR3_DQS1N	LPDDR3_DQS3N
DDR_DQ0_B	DDR4_DQU7_B	LPDDR4_DQ0_B	DDR3_DQ16	LPDDR3_DQ1
DDR_DQ1_B	DDR4_DQU5_B	LPDDR4_DQ1_B	DDR3_DQ17	LPDDR3_DQ5
DDR_DQ2_B	DDR4_DQU3_B	LPDDR4_DQ2_B	DDR3_DQ18	LPDDR3_DQ6
DDR_DQ3_B	DDR4_DQU1_B	LPDDR4_DQ3_B	DDR3_DQ19	LPDDR3_DQ4
DDR_DQ4_B	DDR4_DQU0_B	LPDDR4_DQ4_B	DDR3_DQ20	LPDDR3_DQ2
DDR_DQ5_B	DDR4_DQU6_B	LPDDR4_DQ5_B	DDR3_DQ21	LPDDR3_DQ3
DDR_DQ6_B	DDR4_DQU4_B	LPDDR4_DQ6_B	DDR3_DQ22	LPDDR3_DQ7
DDR_DQ7_B	DDR4_DQU2_B	LPDDR4_DQ7_B	DDR3_DQ23	LPDDR3_DQ0
DDR_DM0_B	DDR4_DMU_B	LPDDR4_DM0_B	DDR3_DM2	LPDDR3_DM0
DDR_DQS0P_B	DDR4_DQSU_P_B	LPDDR4_DQS0P_B	DDR3_DQS2P	LPDDR3_DQS0P
DDR_DQS0N_B	DDR4_DQSU_N_B	LPDDR4_DQS0N_B	DDR3_DQS2N	LPDDR3_DQS0N
DDR_DQ8_B	DDR4_DQL0_B	LPDDR4_DQ8_B	DDR3_DQ24	LPDDR3_DQ18
DDR_DQ9_B	DDR4_DQL2_B	LPDDR4_DQ9_B	DDR3_DQ25	LPDDR3_DQ19
DDR_DQ10_B	DDR4_DQL4_B	LPDDR4_DQ10_B	DDR3_DQ26	LPDDR3_DQ22
DDR_DQ11_B	DDR4_DQL6_B	LPDDR4_DQ11_B	DDR3_DQ27	LPDDR3_DQ23
DDR_DQ12_B	DDR4_DQL7_B	LPDDR4_DQ12_B	DDR3_DQ28	LPDDR3_DQ16
DDR_DQ13_B	DDR4_DQL5_B	LPDDR4_DQ13_B	DDR3_DQ29	LPDDR3_DQ17
DDR_DQ14_B	DDR4_DQL1_B	LPDDR4_DQ14_B	DDR3_DQ30	LPDDR3_DQ20
DDR_DQ15_B	DDR4_DQL3_B	LPDDR4_DQ15_B	DDR3_DQ31	LPDDR3_DQ21
DDR_DM1_B	DDR4_DML_B	LPDDR4_DM1_B	DDR3_DM3	LPDDR3_DM2
DDR_DQS1P_B	DDR4_DQSL_P_B	LPDDR4_DQS1P_B	DDR3_DQS3P	LPDDR3_DQS2P
DDR_DQS1N_B	DDR4_DQSL_N_B	LPDDR4_DQS1N_B	DDR3_DQS3N	LPDDR3_DQS2N
DDR_ECC_DQ0	DDR4_ECC_DQ7	--	DDR3_ECC_DQ0	
DDR_ECC_DQ1	DDR4_ECC_DQ0	--	DDR3_ECC_DQ1	
DDR_ECC_DQ2	DDR4_ECC_DQ2	--	DDR3_ECC_DQ2	
DDR_ECC_DQ3	DDR4_ECC_DQ1	--	DDR3_ECC_DQ3	
DDR_ECC_DQ4	DDR4_ECC_DQ6	--	DDR3_ECC_DQ4	
DDR_ECC_DQ5	DDR4_ECC_DQ4	--	DDR3_ECC_DQ5	
DDR_ECC_DQ6	DDR4_ECC_DQ3	--	DDR3_ECC_DQ6	
DDR_ECC_DQ7	DDR4_ECC_DQ5	--	DDR3_ECC_DQ7	
DDR_ECC_DM	DDR4_ECC_DM	--	DDR3_ECC_DM	
DDR_ECC_DQS_P	DDR4_ECC_DQS_P	--	DDR3_ECC_DQS_P	
DDR_ECC_DQS_N	DDR4_ECC_DQS_N	--	DDR3_ECC_DQS_N	

DDR4	LPDDR4	DDR3	LPDDR3
DDR4_A0	LPDDR4_CLKP_B	DDR3_A9	---	AC0
DDR4_A1	---	DDR3_A2	---	AC1
DDR4_A2	LPDDR4_A1_A	DDR3_A4	LPDDR3_A6	AC2
DDR4_A3	LPDDR4_CKE1_A	DDR3_A3	---	AC3
DDR4_A4	LPDDR4_A3_B	DDR3_BA1	LPDDR3_A3	AC4
DDR4_A5	LPDDR4_A5_B	DDR3_A11	LPDDR3_A2	AC5
DDR4_A6	LPDDR4_A1_B	DDR3_A13	LPDDR3_A1	AC6
DDR4_A7	LPDDR4_ODT0_CA_B	DDR3_A8	---	AC7
DDR4_A8	LPDDR4_ODT0_CA_A	DDR3_A6	LPDDR3_A9	AC8
DDR4_A9	LPDDR4_CLKN_B	DDR3_A5	---	AC9
DDR4_A10	LPDDR4_CKE0_B	DDR3_A10	---	AC10
DDR4_A11	LPDDR4_A0_A	DDR3_A7	LPDDR3_A8	AC11
DDR4_A12	LPDDR4_A3_A	DDR3_BA2	---	AC12
DDR4_A13	LPDDR4_A0_B	DDR3_A14	LPDDR3_A0	AC13
DDR4_A14_WEn	LPDDR4_A4_A	DDR3_A15	LPDDR3_A5	AC14
DDR4_A15_CASn	LPDDR4_A2_A	DDR3_A0	---	AC15
DDR4_A16_RASn	LPDDR4_A5_A	DDR3_RASn	LPDDR3_A7	AC16
DDR4_ACTn	LPDDR4_CKE1_B	DDR3_CASn	---	AC17
DDR4_BA0	LPDDR4_A2_B	DDR3_A1	---	AC18
DDR4_BA1	LPDDR4_A4_B	DDR3_A12	LPDDR3_A4	AC19
DDR4_BG0	LPDDR4_ODT1_CA_B	DDR3_WEn	---	AC20
DDR4_BG1	LPDDR4_ODT1_CA_A	DDR3_BA0	---	AC21
DDR4_CKE	LPDDR4_CKE0_A	DDR3_CKE	LPDDR3_CKE	AC22
DDR4_CLKP	LPDDR4_CLKP_A	DDR3_CLKP	LPDDR3_CLKP	AC23
DDR4_CLKN	LPDDR4_CLKN_A	DDR3_CLKN	LPDDR3_CLKN	AC24
DDR4_CS0n	LPDDR4_CS0n_A	DDR3_ODT1	LPDDR3_ODT0	AC25
DDR4_CS1n	LPDDR4_CS1n_A	DDR3_CS1n	LPDDR3_ODT1	AC26
DDR4_ODT0	LPDDR4_CS1n_B	DDR3_ODT0	LPDDR3_CS1n	AC27
DDR4_ODT1	LPDDR4_CS0n_B	DDR3_CS0n	LPDDR3_CS0n	AC28
DDR4_RESETn	LPDDR4_RESETn	DDR3_RESETn	---	AC29

Note: Sequences can not be swap

Note:
Except DDR3, other DQ sequences can not be swap

DDR_RZQ

DDR_VREFOUT

DDR3L	=1.35V
DDR3	=1.5V
DDR4	=1.2V
LPDDR3	=1.2V
LPDDR4	=1.1V
LPDDR4x	=1.1V

DDRPHY_VDDQ_1 … DDRPHY_VDDQ_8

DDR3L	=1.35V
DDR3	=1.5V
DDR4	=1.2V
LPDDR3	=1.2V
LPDDR4	=1.1V
LPDDR4x	=0.6V

DDRPHY_VDDQL_1 … DDRPHY_VDDQL_6

DDR_AVSS

RK3568
BGA636_19R00X19R00X1R20

For DDR4/DDR3/LPDDR3 mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_RZQ pin and VSS pin

For LPDDR4/LPDDR4x mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_RZQ pin and DDRPHY_VDDQ pin

DDR_RZQ R1 120R 1% R0201 VCC_DDR

LPDDR4/LPDDR4x

VCC_DDR

C22 100nF X5R 10V C0201
C23 100nF X5R 10V C0201
C24 4.7uF X5R 6.3V C0402
C25 4.7uF X5R 6.3V C0402
C26 10uF X5R 6.3V C0603

VCC0V6_DDR

C27 100nF X5R 10V C0201
C28 100nF X5R 10V C0201
C29 4.7uF X5R 6.3V C0402
C30 4.7uF X5R 6.3V C0402
C31 4.7uF X5R 6.3V C0402

Caps should be placed under the U1000 package

Size	Title:	Gong Le	REV
A3	Page Name:	RK3568_DDR PHY	V1.1
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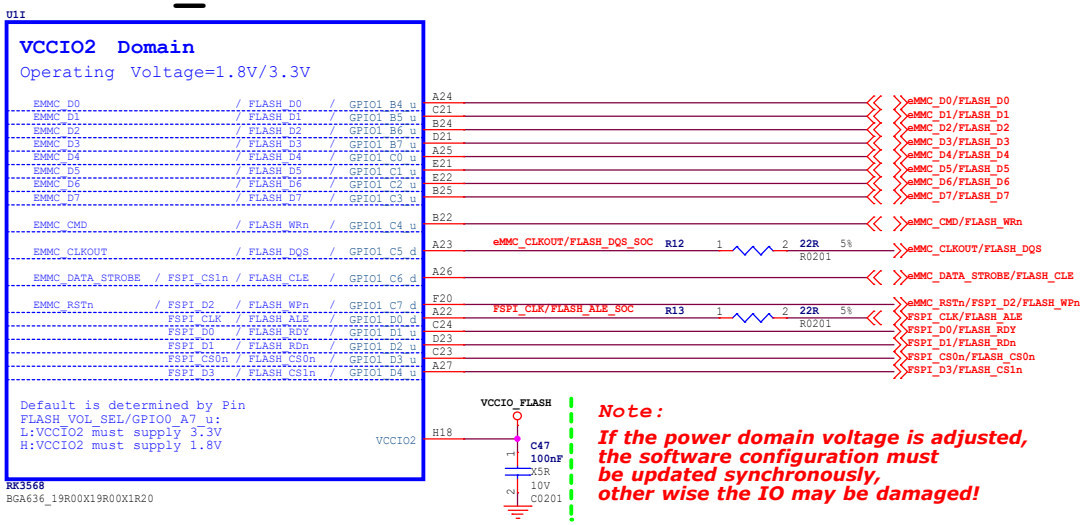
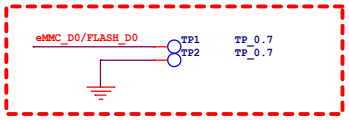
RK3568_I(VCCIO2 Domain)



Note:

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

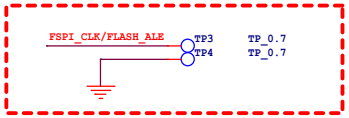


Note:

For eMMC or Nand Flash:
If eMMC_D0/FLASH_D0=0V at after power on and reset, then system will enter into Maskrom mode.

Layout note:

Test point must be placed on the line, and no branch can be added



Note:

For SPI Flash:
If FSPI_CLK=0V at after power on and reset, then system will enter into Maskrom mode.

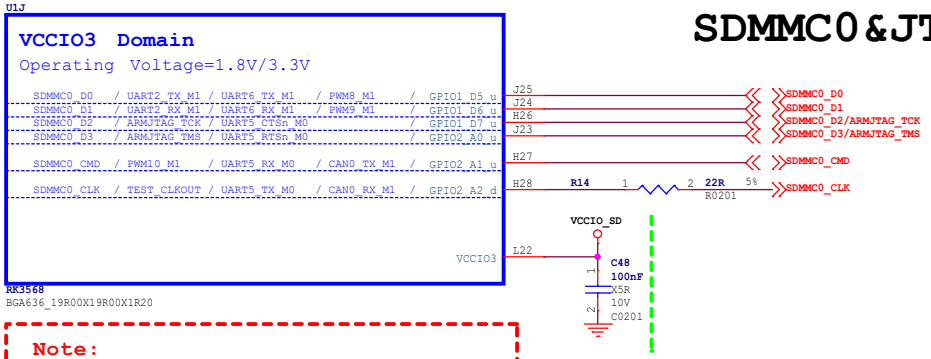
Note:
Reserve TestPoint for put the system into Maskrom mode to update the firmware When writing mismatched firmware or other conditions result in boot failure, use this test point

Except in this case, please use Recovery Key
Put the system into loader mode to update the firmware

RK3568_J(VCCIO3 Domain)

Default

SDMMC0&JTAG



Note:

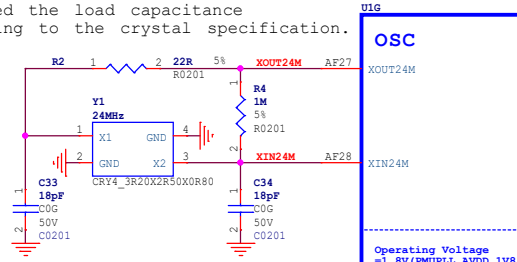
Caps of between dashed green lines and U1000 should be placed under the U1000 package

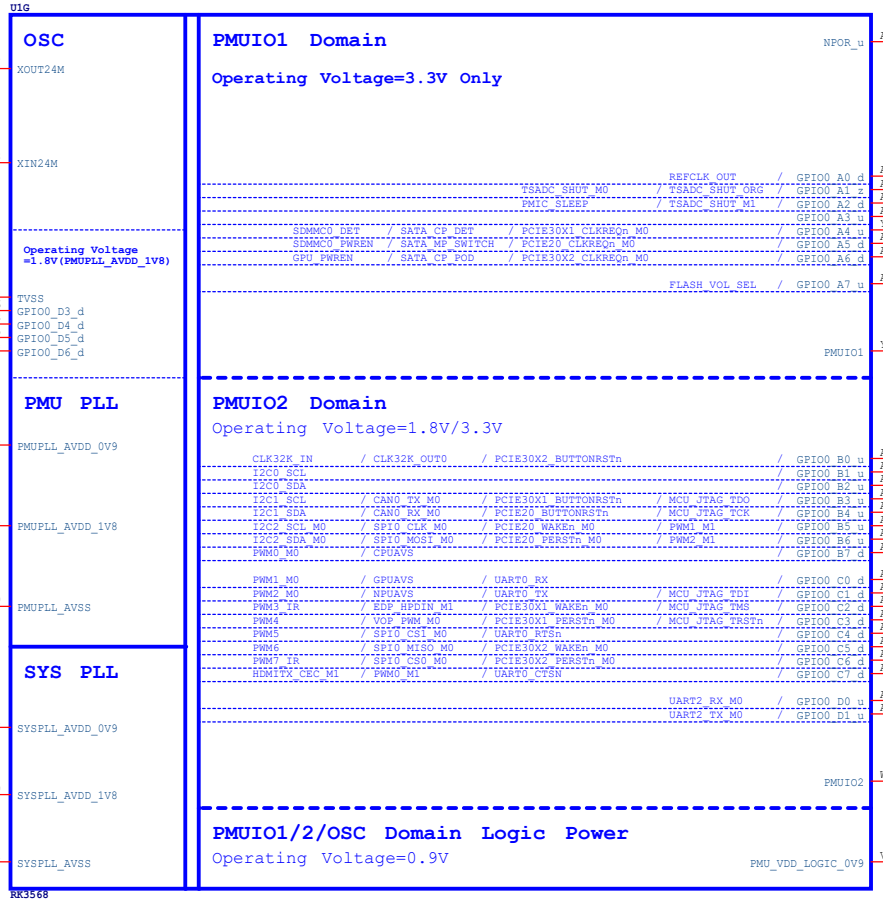
Size A3	Title: Gong Le	REV V1.1
	Page Name: RK3568_Flash/SD Controller	
Date: Wednesday, July 28, 2021	Sheet 08 of 32	

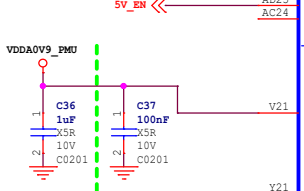
RK3568_G(OSC/PLL/PMUIO1/2)

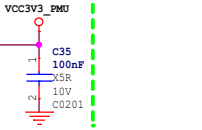
Note:

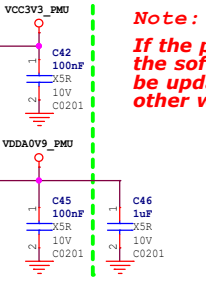
Adjusted the load capacitance according to the crystal specification.

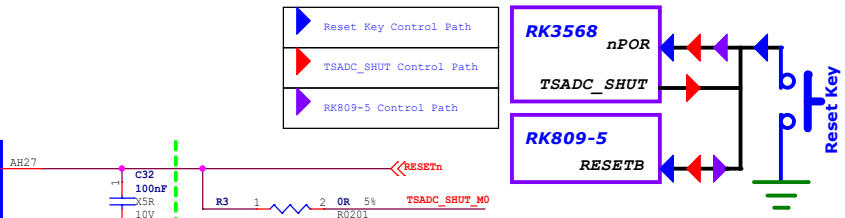


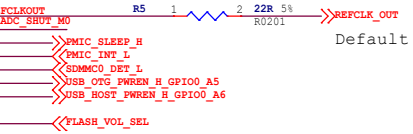




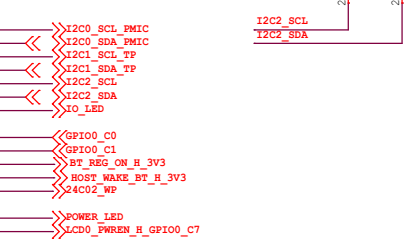


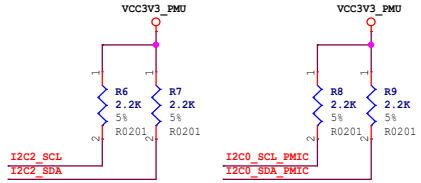


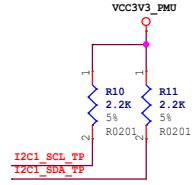




Default:24MHz

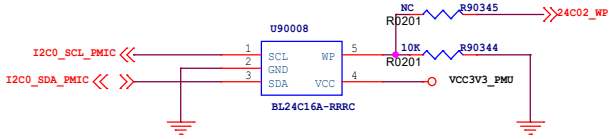






Note:

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!



Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Size	Title:	Gong Le	REV
A3	Page Name:	RK3568_OSC/PLL/PMUIO	V1.1
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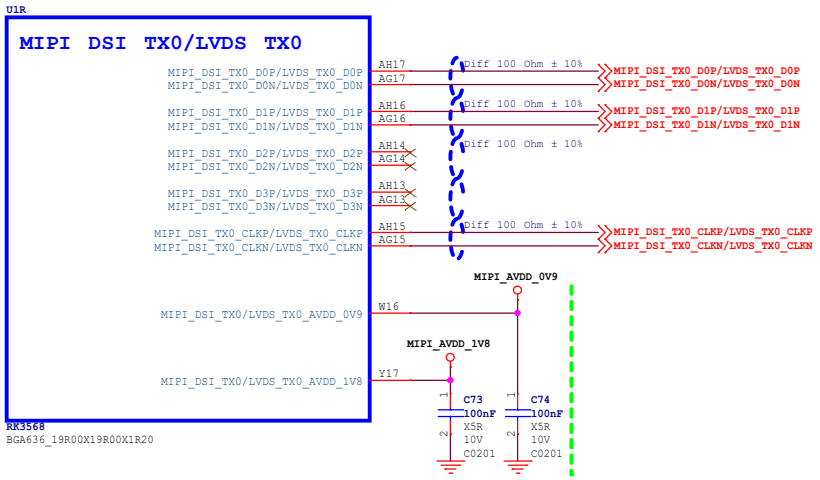
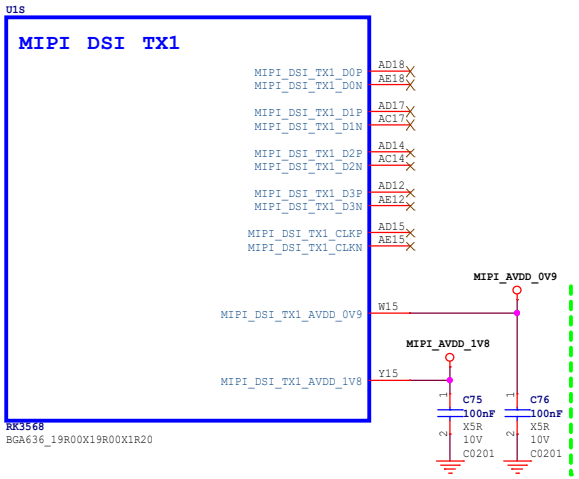
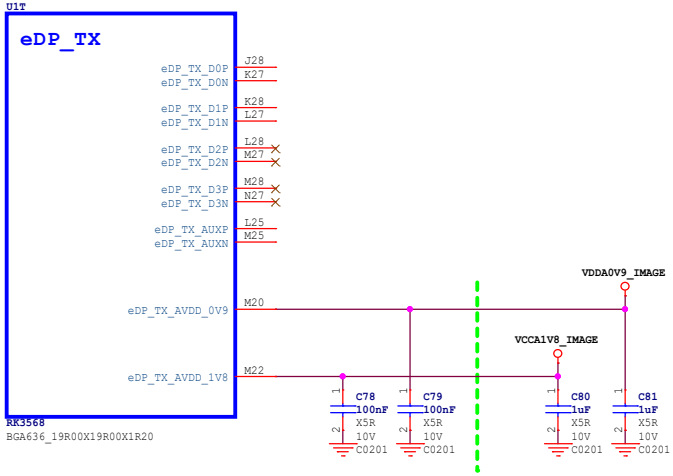
RK3568_R(MIPI_DSI_TX0/LVDS_TX0)



RK3568_S(MIPI_DSI_TX1)

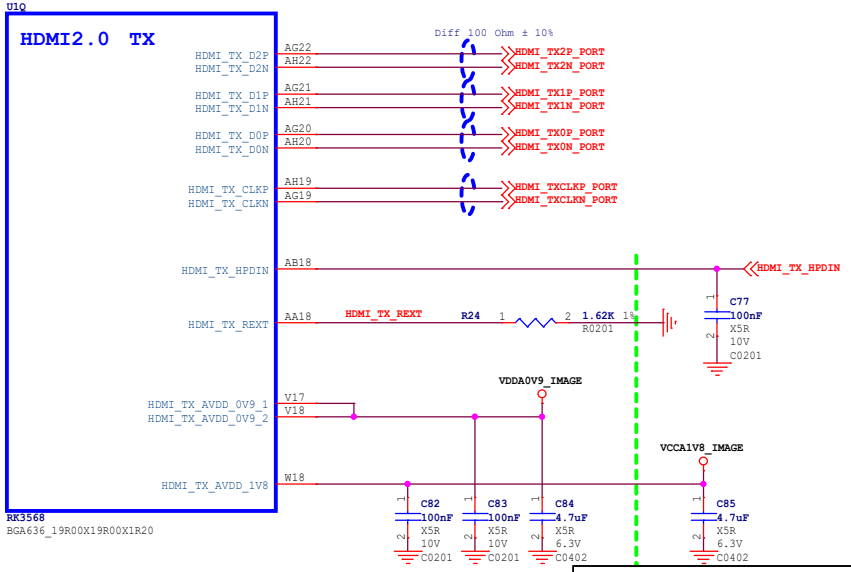


RK3568_T(eDP TX)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3568_Q(HDMI2.0 TX)



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Size	Title:	Gong Le	REV
A3	Page Name:	RK3568_VO Interface_1	V1.1
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RK3568_L(VCCIO5 Domain)

U1L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC_D0	VOP_BT656_D0_M0	SPI0_MISO_M1	PCIE20_CLKREQn_M1	I2S1_MCLK_M2	GPIO2_D0_d
LCDC_D1	VOP_BT656_D1_M0	SPI0_MOSI_M1	PCIE20_WAKEn_M1	I2S1_SCLK_TX_M2	GPIO2_D1_d
LCDC_D2	VOP_BT656_D2_M0	SPI0_CS0_M1	PCIE30X1_CLKREQn_M1	I2S1_LRCK_TX_M2	GPIO2_D2_d
LCDC_D3	VOP_BT656_D3_M0	SPI0_CLK_M1	PCIE30X1_WAKEn_M1	I2S1_SDI0_M2	GPIO2_D3_d
LCDC_D4	VOP_BT656_D4_M0	SPI2_CS1_M1	PCIE30X2_CLKREQn_M1	I2S1_SDI1_M2	GPIO2_D4_d
LCDC_D5	VOP_BT656_D5_M0	SPI2_CS0_M1	PCIE30X2_WAKEn_M1	I2S1_SDI2_M2	GPIO2_D5_d
LCDC_D6	VOP_BT656_D6_M0	SPI2_MOSI_M1	PCIE30X2_PERSTn_M1	I2S1_SDI3_M2	GPIO2_D6_d
LCDC_D7	VOP_BT656_D7_M0	SPI2_MISO_M1	UART8_TX_M1	I2S1_SDO0_M2	GPIO2_D7_d
LCDC_CLK	VOP_BT656_CLK_M0	SPI2_CLK_M1	UART8_RX_M1	I2S1_SDO1_M2	GPIO3_A0_d
LCDC_D8	VOP_BT1120_D0	SPI1_CS0_M1	PCIE30X1_PERSTn_M1	SDMMC2_D0_M1	GPIO3_A1_d
LCDC_D9	VOP_BT1120_D1	GMAC1_TXD2_M0	I2S3_MCLK_M0	SDMMC2_D1_M1	GPIO3_A2_d
LCDC_D10	VOP_BT1120_D2	GMAC1_TXD3_M0	I2S3_SCLK_M0	SDMMC2_D2_M1	GPIO3_A3_d
LCDC_D11	VOP_BT1120_D3	GMAC1_RXD2_M0	I2S3_LRCK_M0	SDMMC2_D3_M1	GPIO3_A4_d
LCDC_D12	VOP_BT1120_D4	GMAC1_RXD3_M0	I2S3_SDO_M0	SDMMC2_CMD_M1	GPIO3_A5_d
LCDC_D13	VOP_BT1120_CLK	GMAC1_TXCLK_M0	I2S3_SDI_M0	SDMMC2_CLK_M1	GPIO3_A6_d
LCDC_D14	VOP_BT1120_D5	GMAC1_RXCLK_M0		SDMMC2_DET_M1	GPIO3_A7_d
LCDC_D15	VOP_BT1120_D6	ETH1_REFCLKO_25M_M0		SDMMC2_PWREN_M1	GPIO3_B0_d
LCDC_D16	VOP_BT1120_D7	GMAC1_RXD0_M0	UART4_RX_M1	PWM8_M0	GPIO3_B1_d
LCDC_D17	VOP_BT1120_D8	GMAC1_RXD1_M0	UART4_TX_M1	PWM9_M0	GPIO3_B2_d
LCDC_D18	VOP_BT1120_D9	GMAC1_RXDV_CRS_M0	I2C5_SCL_M0	PDM_SDI0_M2	GPIO3_B3_d
LCDC_D19	VOP_BT1120_D10	GMAC1_RXER_M0	I2C5_SDA_M0	PDM_SDI1_M2	GPIO3_B4_d
LCDC_D20	VOP_BT1120_D11	GMAC1_TXD0_M0	I2C3_SCL_M1	PWM10_M0	GPIO3_B5_d
LCDC_D21	VOP_BT1120_D12	GMAC1_TXD1_M0	I2C3_SDA_M1	PWM11_IR_M0	GPIO3_B6_d
LCDC_D22	PWM12_M0	GMAC1_TXEN_M0	UART3_TX_M1	PDM_SDI2_M2	GPIO3_B7_d
LCDC_D23	PWM13_M0	GMAC1_MCLKINOUT_M0	UART3_RX_M1	PDM_SDI3_M2	GPIO3_C0_d
LCDC_HSYNC	VOP_BT1120_D13	SPI1_MOSI_M1	PCIE20_PERSTn_M1	I2S1_SDO2_M2	GPIO3_C1_d
LCDC_VSYNC	VOP_BT1120_D14	SPI1_MISO_M1	UART5_TX_M1	I2S1_SDO3_M2	GPIO3_C2_d
LCDC_DEN	VOP_BT1120_D15	SPI1_CLK_M1	UART5_RX_M1	I2S1_SCLK_RX_M2	GPIO3_C3_d
PWM14_M0	VOP_PWM_M1	GMAC1_MDC_M0	UART7_TX_M1	PDM_CLK1_M2	GPIO3_C4_d
PWM15_IR_M0	SPDIF_TX_M1	GMAC1_MDIO_M0	UART7_RX_M1	I2S1_LRCK_RX_M2	GPIO3_C5_d

VCCIO5_1
VCCIO5_2

RK3568
BGA636_19R00X19R00X1R20

AG6 PCIE20_CLKREQn_M1
AD7 PCIE20_WAKEn_M1
AC8 HP_DET_L_GPIO2_D2
AC7
AF5 PCIE30X2_CLKREQn_M1
AF6 PCIE30X2_WAKEn_M1
AD6 PCIE30X2_PERSTn_M1
AH5 GPIO2_D7
AH4 GPIO3_A0
AB8 GPIO3_A1
AE5 GPIO3_A2
AG4 GPIO3_A3
AF4 GPIO3_A4
AH3 GPIO3_A5
AG3 GPIO3_A6
AH2 GMAC1_INT/PMEB_GPIO3_A7
AG2 GMAC1_RSTn_GPIO3_B0
AG1 PWM_FAN
AF2 GPIO3_B2
AF1 I2C5_SCL_M0
AE1 I2C5_SDA_M0
AE2 I2C3_SCL_M1
AE3 I2C3_SDA_M1
AD4 GPIO3_B7
AD2 GPIO3_C0
AD1 PCIE20_PERSTn_M1
AA7 GPIO3_C2
AC4 GPIO3_C3
AC3 GPIO3_C4
AC2 GPIO3_C5

V10
V11

VCC_3V3
C86 100nF X5R 10V C0201

VCC_3V3
R25 10K 5% R0201
od
GMAC1_INT/PMEB_GPIO3_A7

VCC_3V3
R26 2.2K 5% R0201
R27 2.2K 5% R0201
I2C5_SCL_M0
I2C5_SDA_M0

VCC_3V3
R28 2.2K 5% R0201
R29 2.2K 5% R0201
I2C3_SCL_M1
I2C3_SDA_M1

Note:
If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

radxa

Size	Title:	Gong Le	REV
A4	Page Name:	RK3568_VO Interface_2	V1.1
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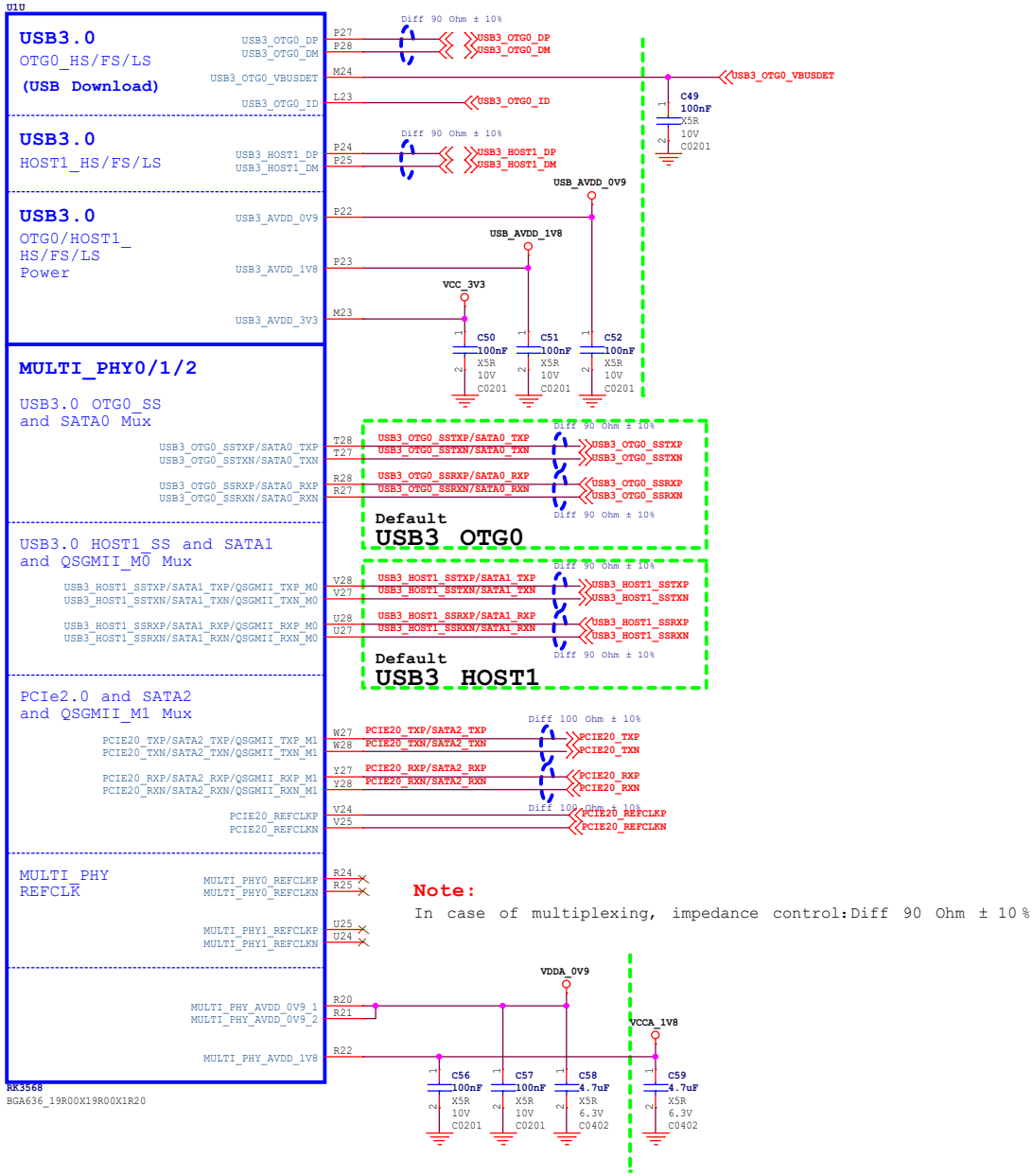
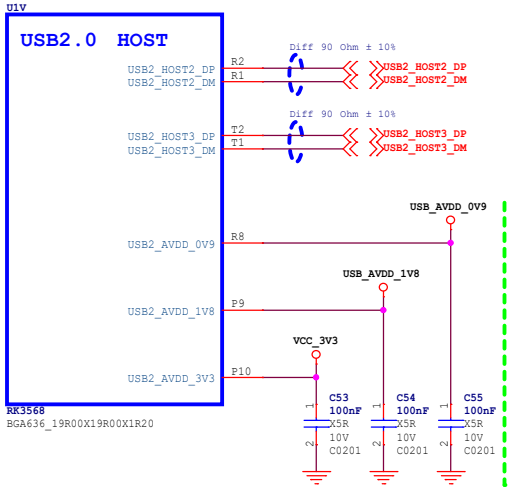
RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)

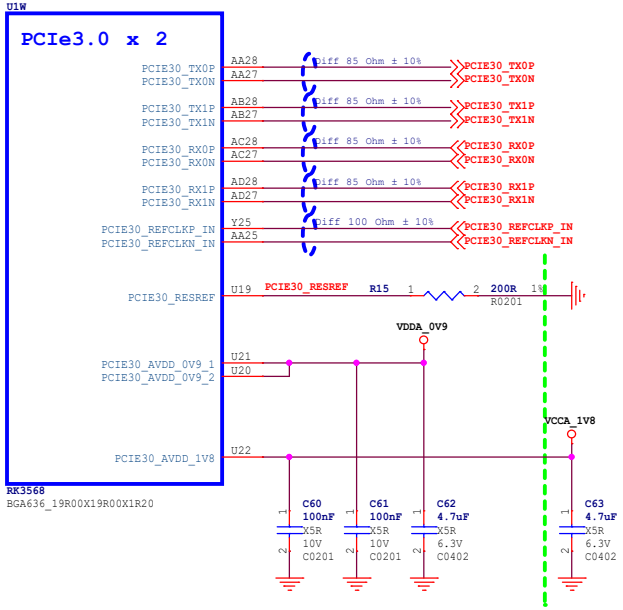


Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3568_V(USB2.0 HOST)



RK3568_W(PCIe3.0 x2)



Size	Title:	Gong Le	REV
A3	Page Name:	RK3568_USB/PCIe/SATA PHY	V1.1
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RK3568_H(VCCIO1 Domain)

U1H

VCCIO1 Domain

Operating Voltage=1.8V/3.3V

I2C3_SDA_M0	/ UART3_RX_M0	/ CAN1_RX_M0		/ AUDIOPWM_LOUT_P	/ ACODEC_ADC_DATA	/	GPIO1_A0_u
I2C3_SCL_M0	/ UART3_TX_M0	/ CAN1_TX_M0		/ AUDIOPWM_LOUT_N	/ ACODEC_ADC_CLK	/	GPIO1_A1_u
I2S1_MCLK_M0	/ UART3_RTSn_M0	/ SCR_CLK	/ PCIE30X1_PERSTn_M2			/	GPIO1_A2_d
I2S1_SCLK_TX_M0	/ UART3_CTSn_M0	/ SCR_IO	/ PCIE30X1_WAKEn_M2		/ ACODEC_DAC_CLK	/	GPIO1_A3_d
I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0		/ SPDIF_TX_M0		/	GPIO1_A4_d
I2S1_LRCK_TX_M0	/ UART4_RTSn_M0	/ SCR_RST	/ PCIE30X1_CLKREQn_M2		/ ACODEC_DAC_SYNC	/	GPIO1_A5_d
I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0		/ AUDIOPWM_ROUT_P		/	GPIO1_A6_d
I2S1_SDO0_M0	/ UART4_CTSn_M0	/ SCR_DET		/ AUDIOPWM_ROUT_N	/ ACODEC_DAC_DATAL	/	GPIO1_A7_d
I2S1_SDO1_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0	/ PCIE20_CLKREQn_M2		/ ACODEC_DAC_DATAR	/	GPIO1_B0_d
I2S1_SDO2_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0	/ PCIE20_WAKEn_M2		/ ACODEC_ADC_SYNC	/	GPIO1_B1_d
I2S1_SDO3_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0	/ PCIE20_PERSTn_M2			/	GPIO1_B2_d
	I2S1_SDI0_M0	/ PDM_SDI0_M0				/	GPIO1_B3_d

VCCIO1

RK3568

BGA636_19R00X19R00X1R20

D18 — GPIO1_A0
E18 — GPIO1_A1
A19 — I2S1_MCLK_M0_RK809
B19 — I2S1_SCLK_TX_M0_RK809
F18
A20 — I2S1_LRCK_TX_M0_RK809
C20 — PDM_CLK0_M0_RK809
B20 — I2S1_SDO0_M0_RK809
D20
E20 — MIPI_CAM0_PDN_L_GPIO1_B1
A21
B21 — I2S1_SDI0_M0/PDM_SDI0_M0_RK809

VCCIO_ACODEC

H17

C87
100nF
X5R
10V
C0201

Default 3.3V

Note:

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

radxa

Size	Title:	Gong Le	REV
A4	Page Name:	RK3568_Audio Interface	V1.1
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RK3568_K(VCCIO4 Domain)

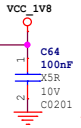
U1K

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

SDMMC1_D0	/ GMAC0_RXD2	/ UART6_RX_M0	/ GPIO2_A3_u	E27
SDMMC1_D1	/ GMAC0_RXD3	/ UART6_TX_M0	/ GPIO2_A4_u	E28
SDMMC1_D2	/ GMAC0_RXCLK	/ UART7_RX_M0	/ GPIO2_A5_u	B28
SDMMC1_D3	/ GMAC0_TXD2	/ UART7_TX_M0	/ GPIO2_A6_u	C27
SDMMC1_CMD	/ GMAC0_TXD3	/ UART9_RX_M0	/ GPIO2_A7_u	C28
SDMMC1_CLK	/ GMAC0_TXCLK	/ UART9_TX_M0	/ GPIO2_B0_d	D27 → WIFI_LED
SDMMC1_PWREN	/ I2C4_SDA_M1	/ UART8_RTSn_M0 / CAN2_RX_M1	/ GPIO2_B1_d	D26 → I2C4_SDA_M1
SDMMC1_DET	/ I2C4_SCL_M1	/ UART8_CTSn_M0 / CAN2_TX_M1	/ GPIO2_B2_u	E25 → I2C4_SCL_M1
	GMAC0_TXD0	/ UART1_RX_M0	/ GPIO2_B3_u	F28 → UART1_RX_M0
	GMAC0_TXD1	/ UART1_TX_M0	/ GPIO2_B4_u	G27 → UART1_TX_M0
	GMAC0_TXEN	/ UART1_RTSn_M0 / SPI1_CLK_M0	/ GPIO2_B5_u	G28 → UART1_RTS_M0
	GMAC0_RXD0	/ UART1_CTSn_M0 / SPI1_MISO_M0	/ GPIO2_B6_u	F27 → UART1_CTS_M0
I2S2_SCLK_RX_M0	/ GMAC0_RXD1	/ UART6_RTSn_M0 / SPI1_MOSI_M0	/ GPIO2_B7_d	H25
I2S2_LRCK_RX_M0	/ GMAC0_RXDV_CRS	/ UART6_CTSn_M0 / SPI1_CS0_M0	/ GPIO2_C0_d	F24
I2S2_MCLK_M0	/ ETH0_REFCLKO_25M	/ UART7_RTSn_M0 / SPI2_CLK_M0	/ GPIO2_C1_d	G23
I2S2_SCLK_TX_M0	/ GMAC0_MCLKINOUT	/ UART7_CTSn_M0 / SPI2_MISO_M0	/ GPIO2_C2_d	F25 → SOC_PCM_CLK
I2S2_LRCK_TX_M0	/ GMAC0_MDC	/ UART9_RTSn_M0 / SPI2_MOSI_M0	/ GPIO2_C3_d	H24 → SOC_PCM_SYNC
I2S2_SDO_M0	/ GMAC0_MDIO	/ UART9_CTSn_M0 / SPI2_CS0_M0	/ GPIO2_C4_d	H23 → SOC_PCM_OUT
I2S2_SDI_M0	/ GMAC0_RXER	/ UART8_TX_M0 / SPI2_CS1_M0	/ GPIO2_C5_d	F26 → SOC_PCM_IN
CLK32K_OUT1		/ UART8_RX_M0 / SPI1_CS1_M0	/ GPIO2_C6_d	E26
			VCCIO4	J21

RK3568
BGA636_19R00X19R00X1R20



RGMII0

Note:
If Ethernet PHY uses other models, please note whether the default pull-up and pull-down of GPIO affect Ethernet PHY function

At present, TXEN will be affected if it defaults to high level need to add a 4.7K resistance to ground

Note:
According to the actual choice of mounted Cannot be mounted at the same time
Default:1.8V
Select the voltage according to the application

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

RK3568_N(VCCIO7 Domain)

Note:
When use HDMI, HDMITX_SCL/SDA cannot be shared with other devices

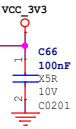
U1N

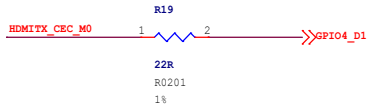
VCCIO7 Domain

Operating Voltage=1.8V/3.3V

PWM14_M1	/ SPI3_CLK_M1 / CAN1_RX_M1	/ PCIE30X2_CLKREQn_M2 / I2S3_MCLK_M1	/ GPIO4_C2_d	AF8 → GPIO4_C2
PWM15_IR_M1	/ SPI3_MOSI_M1 / CAN1_TX_M1	/ PCIE30X2_WAKEn_M2 / I2S3_SCLK_M1	/ GPIO4_C3_d	AA11 → GPIO4_C3
EDP_HPDIN_M0	/ SPDIF_TX_M2 / SATA2_ACT_LED	/ PCIE30X2_PERSTn_M2 / I2S3_LRCK_M1	/ GPIO4_C4_d	AH7
PWM12_M1	/ SPI3_MISO_M1 / SATA1_ACT_LED	/ UART9_TX_M1 / I2S3_SDO_M1	/ GPIO4_C5_d	AD8 → GPIO4_C5
PWM13_M1	/ SPI3_CS0_M1 / SATA0_ACT_LED	/ UART9_RX_M1 / I2S3_SDI_M1	/ GPIO4_C6_d	AE8 → GPIO4_C6
HDMITX_SCL	/ I2C5_SCL_M1		/ GPIO4_C7_u	AG8 → HDMITX_SCL
HDMITX_SDA	/ I2C5_SDA_M1		/ GPIO4_D0_u	AG7 → HDMITX_SDA
HDMITX_CEC_M0	/ SPI3_CS1_M1		/ GPIO4_D1_u	AH6 → HDMITX_CEC_M0
			GPIO4_D2_d	AB9 → CAMERAB_PDN_L_GPIO4_D2 [26]
			VCCIO7	V12

RK3568
BGA636_19R00X19R00X1R20





Note:
If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

RK3568_O(SARADC/OTP)

U1O

SARADC

Recovery/ SARADC_VIN0	B27	SARADC_VIN0_KEY/RECOVERY — C65 1nF X5R 50V C0201
SARADC_VIN1	C26	SARADC_VIN1
SARADC_VIN2	D24	SARADC_VIN2_HP_HOOK
SARADC_VIN3	E23	SARADC_VIN3
SARADC_VIN4	G21	ADC_IN4 [26]
SARADC_VIN5	F22	SARADC_VIN5
SARADC_VIN6	G20	
SARADC_VIN7	F21	
SARADC_AVDD_1V8	H22	VCCA_1V8 — C67 100nF X5R 10V C0201

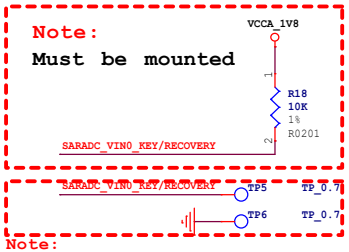
OTP

OTP_VCC18	H20	VCC_1V8 — C68 100nF X5R 10V C0201

RK3568
BGA636_19R00X19R00X1R20

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Note:
Must be mounted



Note:
If there is no Key requirement, two test points must be reserved to facilitate firmware update

It is suggested to reserve a Key to facilitate the development debug

If SARADC_VIN0=0V at after power on and reset, then system will enter into loader mode.

SARADC_VIN0_KEY/RECOVERY

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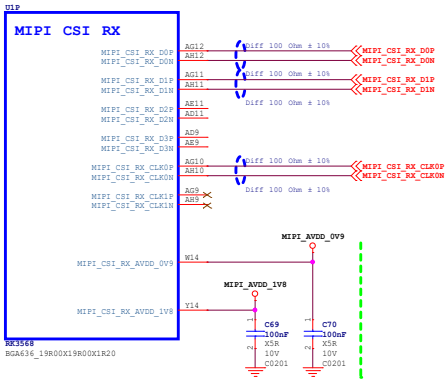
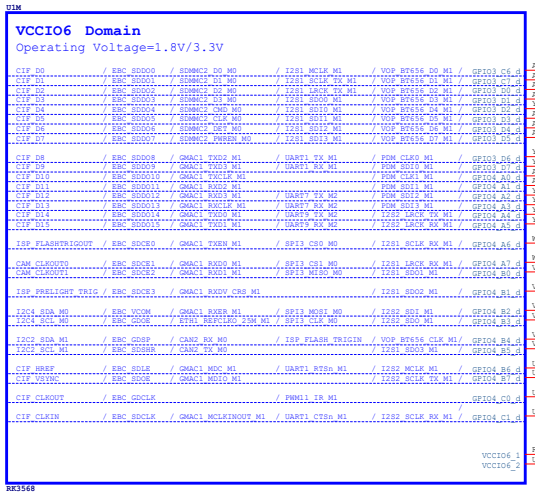
Size	Title:	Gong Le	REV
A3	Page Name:	RK3568_SARADC/GPIO	V1.1
Date:	Wednesday, July 28, 2021	Sheet 14 of 32	

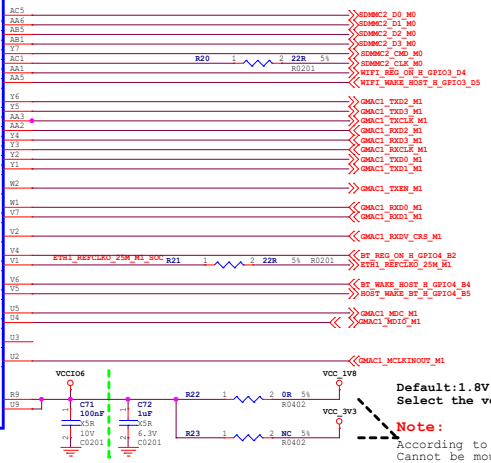
RK3568_P(MIPI_CSI_RX)



Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0
		MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

RK3568_M(VCCIO6 Domain)





Default:1.8V
Select the voltage according to the application

Note:
According to the actual choice of mounted
Cannot be mounted at the same time

Note:
If the power domain voltage is adjusted,
the software configuration must
be updated synchronously,
other wise the IO may be damaged!

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Note:
Camera MCLK can select the following clock:
1:CAM_CLKOUT0
2:CAM_CLKOUT1
3:CIF_CLKOUT
4:REFCLK_OUT

Attention to the voltage matching

Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

BT1120 16bit Mode:
Default: D0-D7 <--> Y0-Y7 , D8-D15 <--> C0-C7
Swap ON: D0-D7 <--> C0-C7 , D8-D15 <--> Y0-Y7

GMAC	Direction	GEPHY	GMAC	Direction	FEPHY
GMACx_TXD0	------->	PHYx_TXD0	GMACx_TXD0	------->	PHYx_TXD0
GMACx_TXD1	------->	PHYx_TXD1	GMACx_TXD1	------->	PHYx_TXD1
GMACx_TXD2	------->	PHYx_TXD2			
GMACx_TXD3	------->	PHYx_TXD3			
GMACx_TXEN	------->	PHYx_TXEN	GMACx_TXEN	------->	PHYx_TXEN
GMACx_TXCLK	------->	PHYx_TXCLK			
GMACx_RXD0	<-------	PHYx_RXD0	GMACx_RXD0	<-------	PHYx_RXD0
GMACx_RXD1	<-------	PHYx_RXD1	GMACx_RXD1	<-------	PHYx_RXD1
GMACx_RXD2	<-------	PHYx_RXD2			
GMACx_RXD3	<-------	PHYx_RXD3			
GMACx_RXDV	<-------	PHYx_RXDV	GMACx_RXDV	<-------	PHYx_RXDV
GMACx_RXCLK	<-------	PHYx_RXCLK			
GMACx_RXER			GMACx_RXER	<-------	PHYx_RXER
GMACx_MDC	------->	PHYx_MDC	GMACx_MDC	------->	PHYx_MDC
GMACx_MDIO	<------->	PHYx_MDIO	GMACx_MDIO	<------->	PHYx_MDIO
ETHx_REFCLKO_25M	------->	PHYx_XTALIN			
GMACx_MCLKINOUT	<-------	PHYx_CLKOUT125(Option)	GMACx_MCLKINOUT	------->	PHYx_XTALIN/REFCLK
GPIO	------->	PHYx_RSTn	GPIO	------->	PHYx_RSTn
GPIO	<-------	PHYx_INT/PMEB	GPIO	<-------	PHYx_INT/PMEB

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A2	Page Name:	RK3568_VI Interface	V1.1
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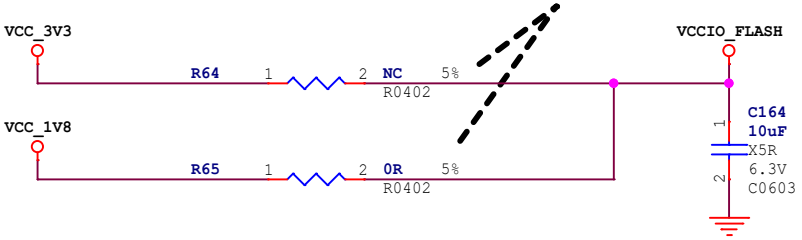
FLASH_VOL_SEL

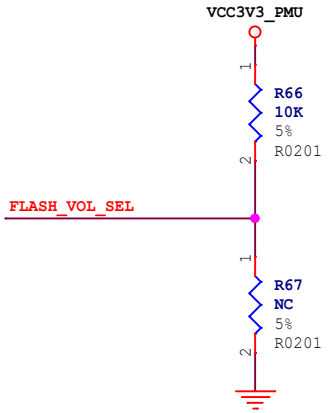
Flash Power Manage

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Optional 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 1.8V, Optional 3.3V	FLASH_VOL_SEL --> Logic=H(Default)

Note:

According to the actual choice of mounted
Cannot be mounted at the same time

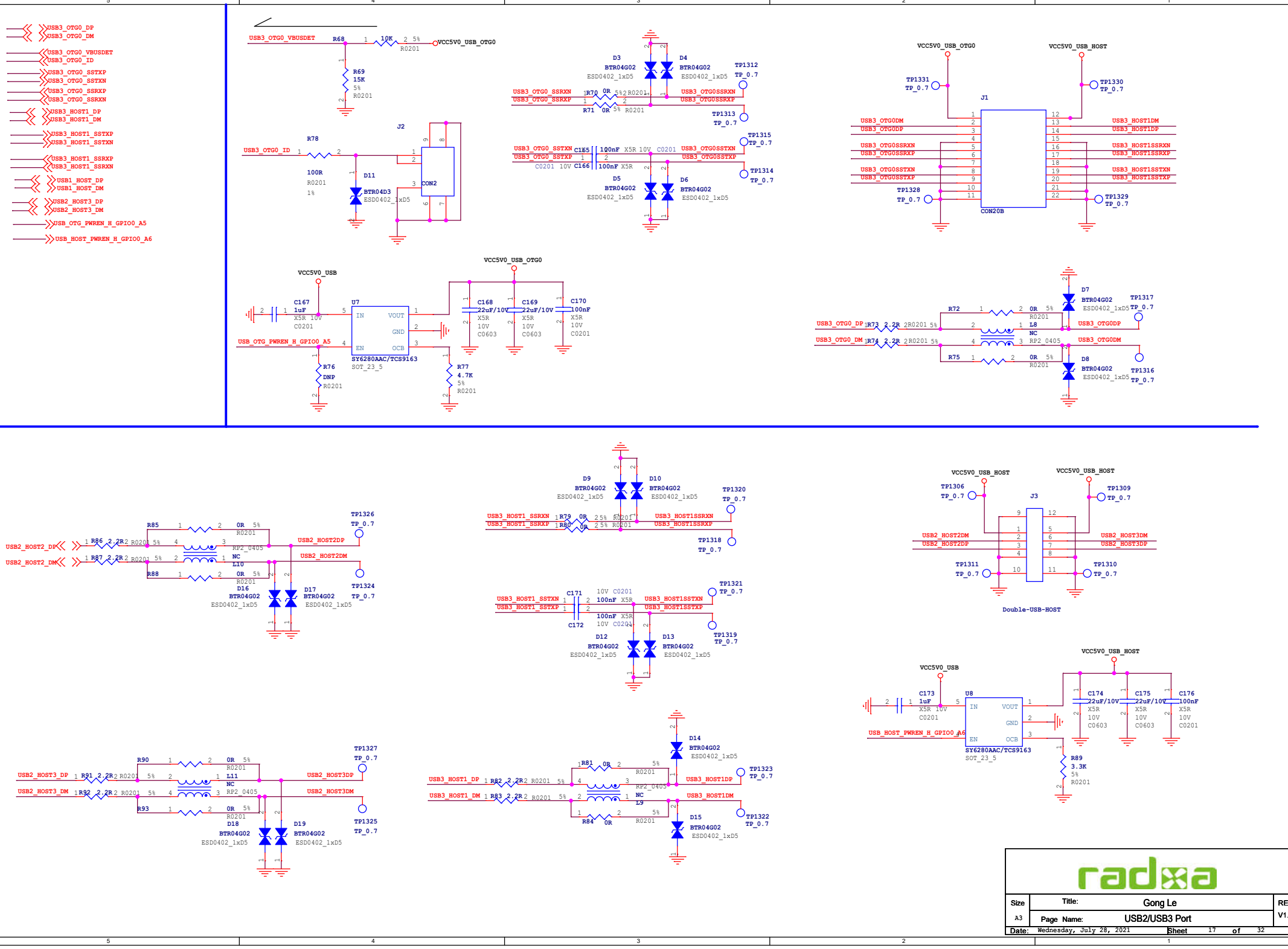




Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L:3.3V IO driven
Logic=H:1.8V IO driven

radxa

Size	Title:	Gong Le	REV
A4	Page Name:	Flash Power Manage	V1.1
Date:	Wednesday, July 28, 2021	Sheet 16 of 32	


USB3_OTG0_DP
USB3_OTG0_DM
USB3_OTG0_VBUSDET
USB3_OTG0_ID
USB3_OTG0_SSTXP
USB3_OTG0_SSTXN
USB3_OTG0_SSRXP
USB3_OTG0_SSRXN
USB3_HOST1_DP
USB3_HOST1_DM
USB3_HOST1_SSTXP
USB3_HOST1_SSTXN
USB3_HOST1_SSRXP
USB3_HOST1_SSRXN
USB1_HOST_DP
USB1_HOST_DM
USB2_HOST3_DP
USB2_HOST3_DM
USB_OTG_PWREN_H_GPIO0_A5
USB_HOST_PWREN_H_GPIO0_A6
USB3_OTG0_VBUSDET
R68
10K
R0201
VCC5V0_USB_OTG0
R69
15K
R78
USB3_OTG0_ID
100R
D11
BTR04D3
ESD0402_1xD5
J2
CON2
D3
D4
BTR04G02
TP1312
TP1313
TP1315
TP1314
R70
R71
C165
C166
100nF
C0201
D5
D6
TP1331
TP1330
J1
CON20B
TP1328
TP1329
USB3_OTG0DM
USB3_OTG0DP
USB3_OTG0SSRXN
USB3_OTG0SSRXP
USB3_OTG0SSTXN
USB3_OTG0SSTXP
USB3_HOST1DM
USB3_HOST1DP
USB3_HOST1SSRXN
USB3_HOST1SSRXP
USB3_HOST1SSTXN
USB3_HOST1SSTXP
VCC5V0_USB
C167
1uF
C0201
U7
SY6280AAC/TCS9163
SOT_23_5
C168
22uF/10V
C0603
C169
C170
100nF
R76
DNP
R77
4.7K
D7
D8
TP1317
TP1316
R72
R73
R74
R75
2.2R
RP2_0405
L8
NC
0R
D9
D10
TP1320
TP1318
R79
R80
TP1306
TP1309
TP1311
TP1310
J3
Double-USB-HOST
C171
C172
TP1321
TP1319
D12
D13
R85
R86
R87
R88
L10
D16
D17
TP1326
TP1324
USB2_HOST2_DP
USB2_HOST2_DM
USB2_HOST2DP
USB2_HOST2DM
R90
R91
R92
R93
L11
D18
D19
TP1327
TP1325
USB2_HOST3_DP
USB2_HOST3_DM
USB2_HOST3DP
USB2_HOST3DM
D14
D15
R81
R82
R83
R84
L9
TP1323
TP1322
USB3_HOST1_DP
USB3_HOST1_DM
USB3_HOST1DP
USB3_HOST1DM
C173
C174
C175
C176
R89
3.3K
USB_HOST_PWREN_H_GPIO0_A6
radxa
Size
A3
Title:
Gong Le
REV
V1.1
Page Name:
USB2/USB3 Port
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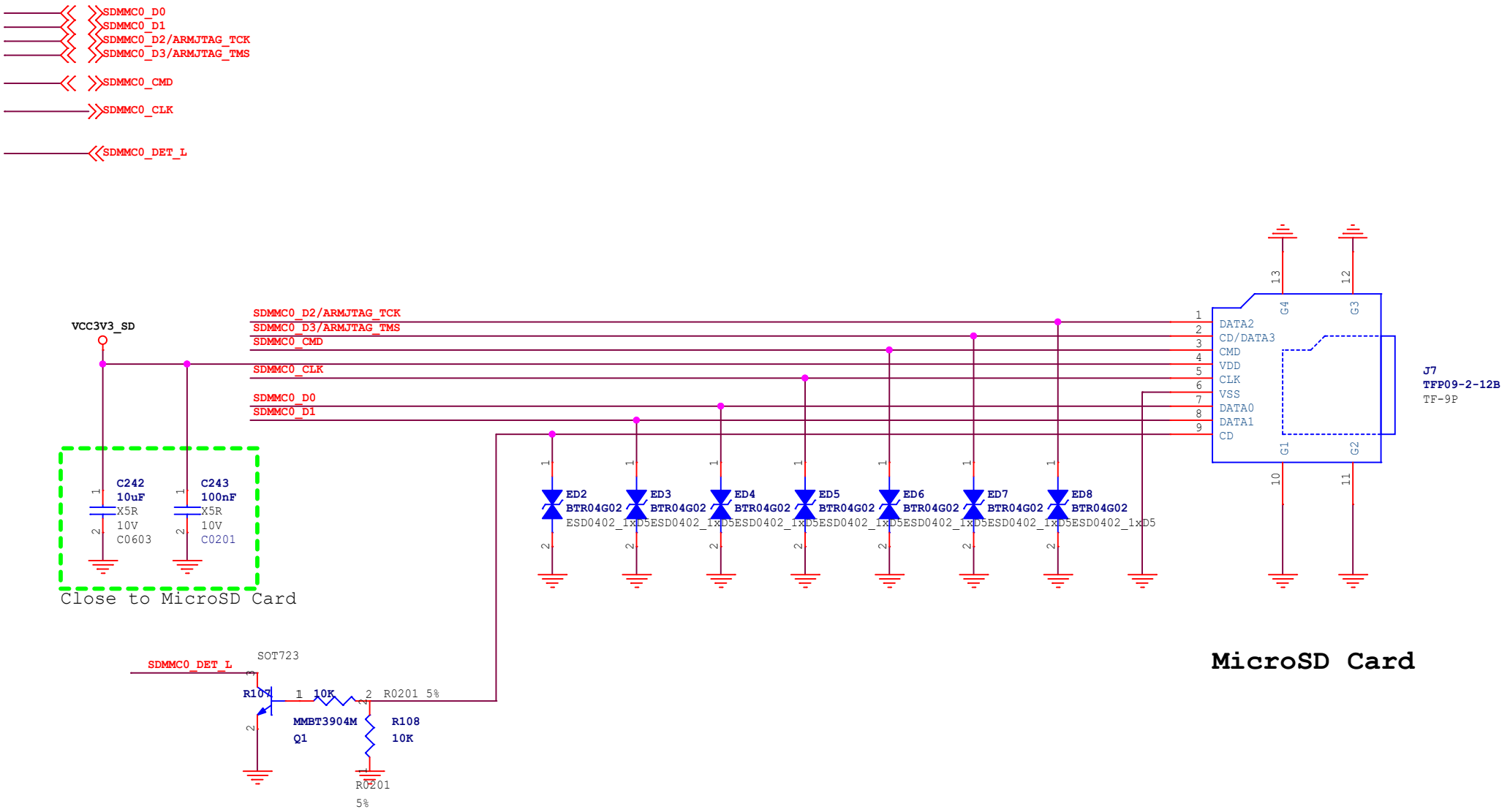
of
32

MicroSD Card



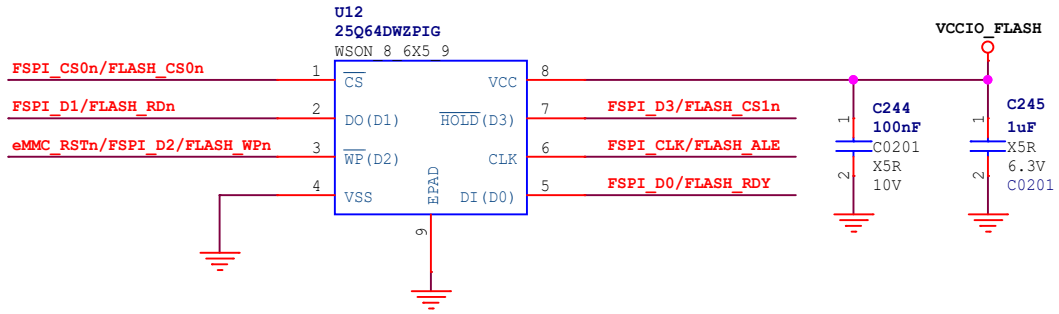
Size: A4	Title: Gong Le		REV: V1.1
	Page Name: MicroSD Card		
Date: Wednesday, July 28, 2021	Sheet 18 of 32		

SPI Flash

FSPI_CLK/FLASH_ALE

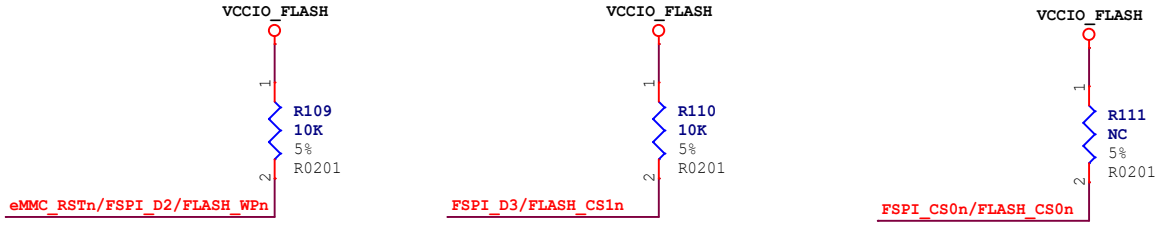
FSPI_D0/FLASH_RDY
FSPI_D1/FLASH_RDn
eMMC_RSTn/FSPI_D2/FLASH_WPn
FSPI_D3/FLASH_CS1n

FSPI_CS0n/FLASH_CS0n



Note:
Default: 1.8V

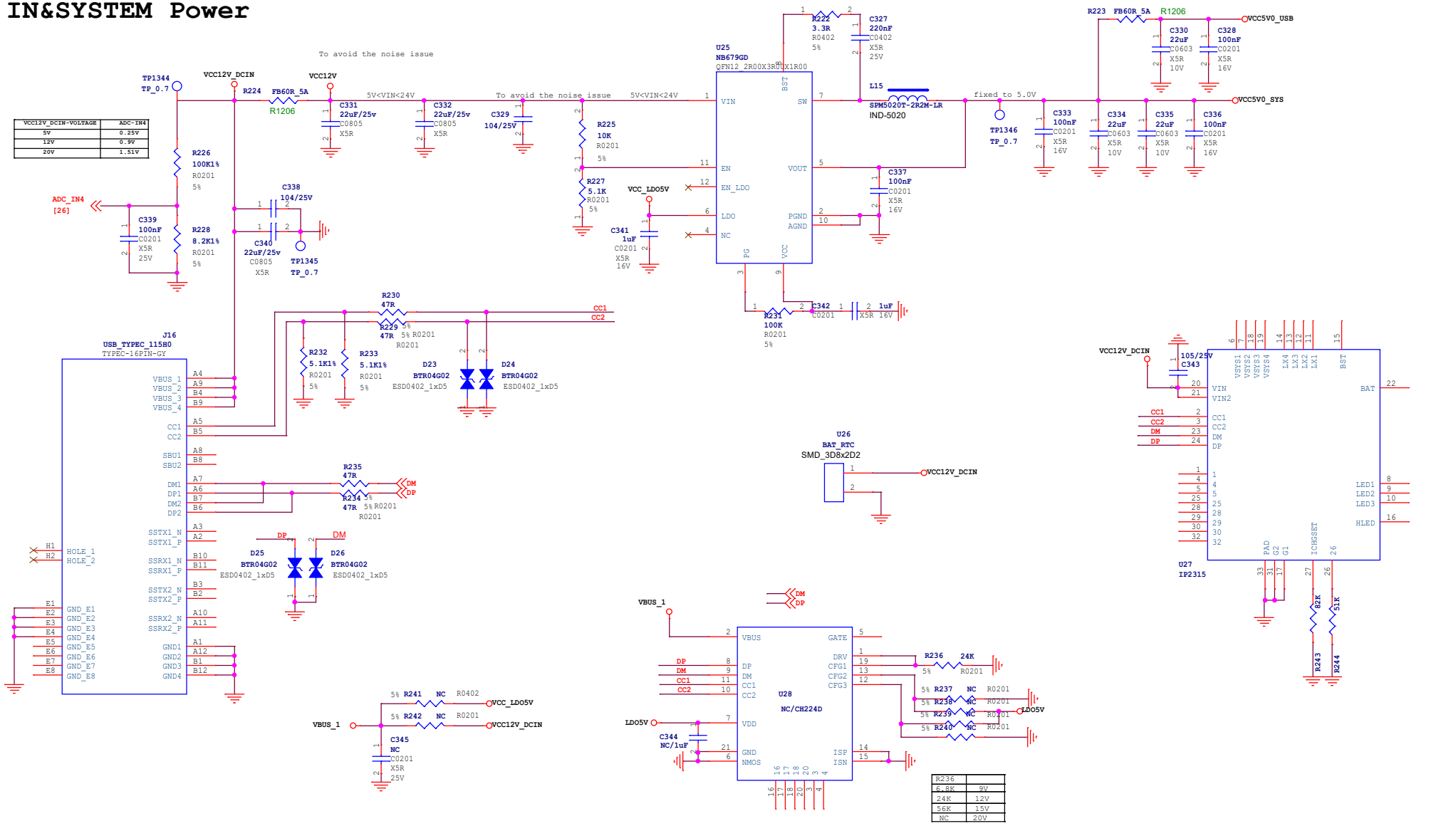
Support:
1bit SPI NOR or SPI NAND
4bit SPI NOR or SPI NAND



Note:
If Flash is compatible, please notice
when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted,@SPI Flash is not mounted
when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted,@SPI Flash is not mounted
when SPI Flash is used, the option is that SPI Flash is mounted, @eMMC is not mounted,@Nand is not mounted

Size	Title:	Gong Le	REV
A4	Page Name:	SPI FLASH(Option)	V1.1
Date:	Wednesday, July 28, 2021	Sheet 19 of 32	

DC IN&SYSTEM Power



VCC12V_DCIN-VOLTAGE	ADC-IN4
5V	0.25V
12V	0.9V
20V	1.51V

R236	
6.8K	9V
24K	12V
56K	15V
NC	20V

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Size	Title:	Gong Le	REV
A3	Page Name:	Power-DC IN	V1.1
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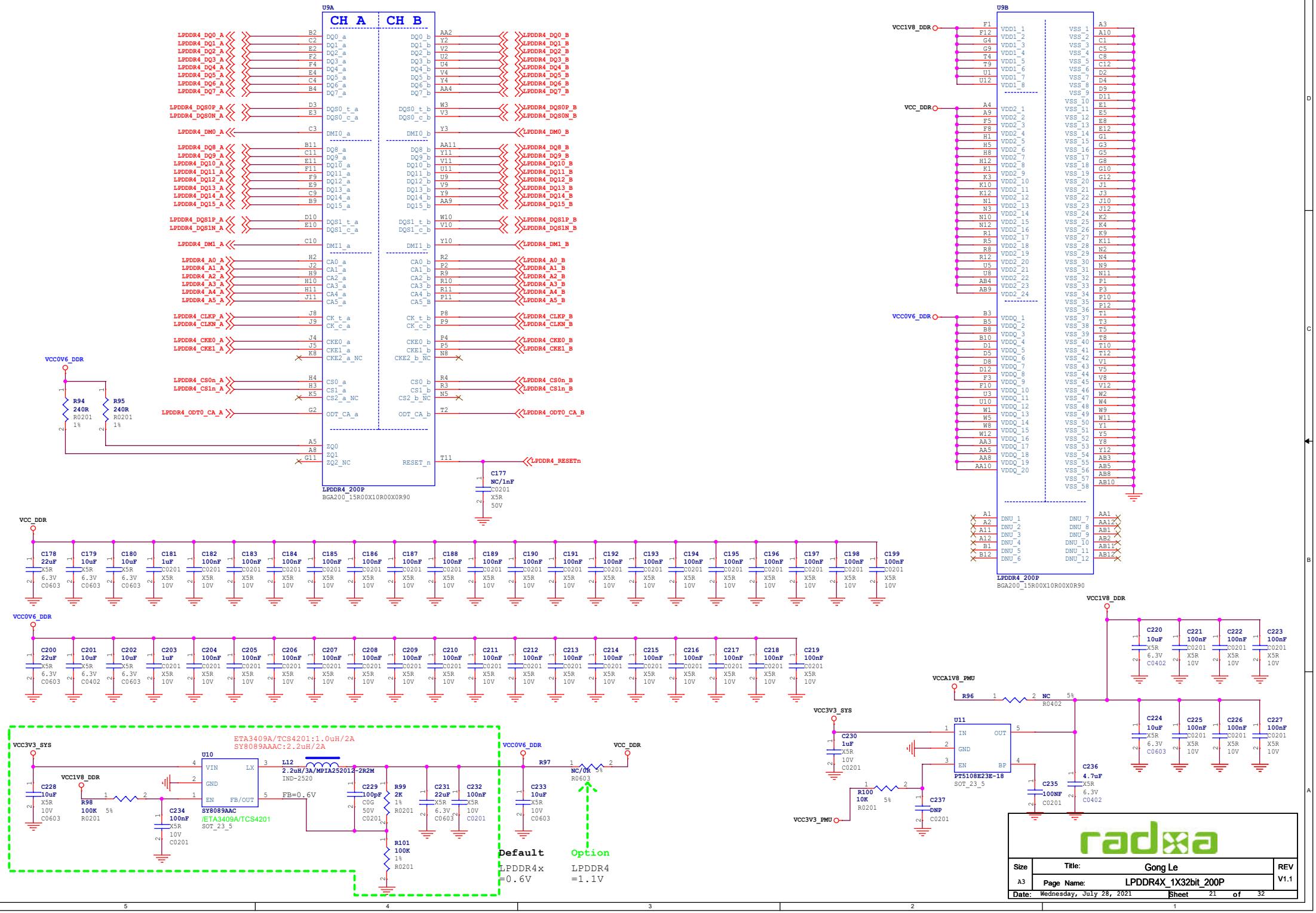
U9A
CH A
CH B
LPDDR4_200P
BGA200_15R00X10R00X0R90
U9B
LPDDR4_200P
BGA200_15R00X10R00X0R90
VCC1V8_DDR
VCC_DDR
VCC0V6_DDR
R94 240R R0201 1%
R95 240R R0201 1%
C177 NC/1nF C0201 X5R 50V
LPDDR4_RESETn
VCC3V3_SYS
VCC1V8_PMU
VCC3V3_PMU
U10
SY8089AAC
/ETA3409A/TCS4201
SOT_23_5
ETA3409A/TCS4201:1.0uH/2A
SY8089AAAC:2.2uH/2A
L12 2.2uH/3A/MPIA252012-2R2M IND-2520
FB=0.6V
R97 NC/0R R0603
U11
PTS108E23E-18
SOT_23_5
R96 NC R0402
R100 10K R0201
C237 DNP C0201
Default
LPDDR4x
=0.6V
Option
LPDDR4
=1.1V
Size A3
Title: Gong Le
Page Name: LPDDR4X_1X32bit_200P
REV V1.1
Date: Wednesday, July 28, 2021
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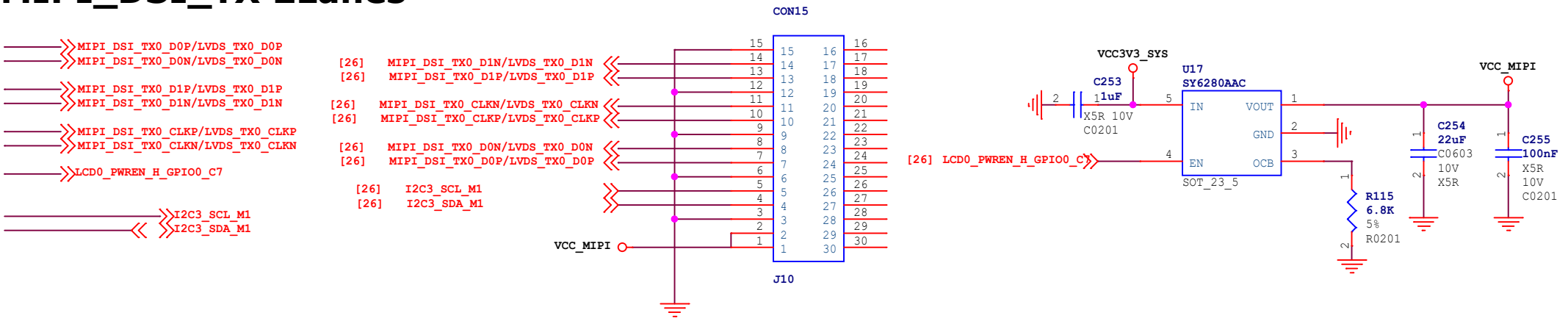
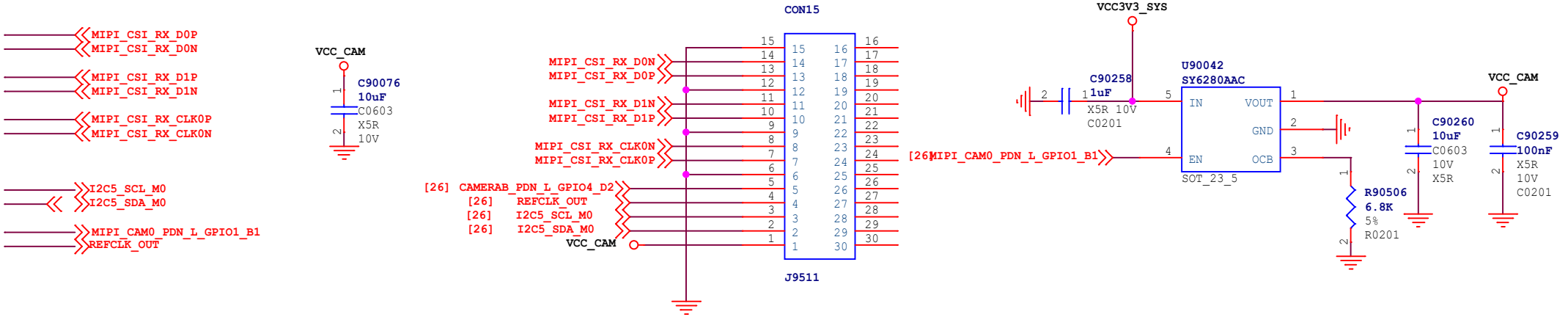
MIPI_DSI_TX 2Lanes



MIPI_CSI_RX 2Lanes



Size A4	Title: Gong Le		REV V1.1
	Page Name: MIPI_DSI_CSI		
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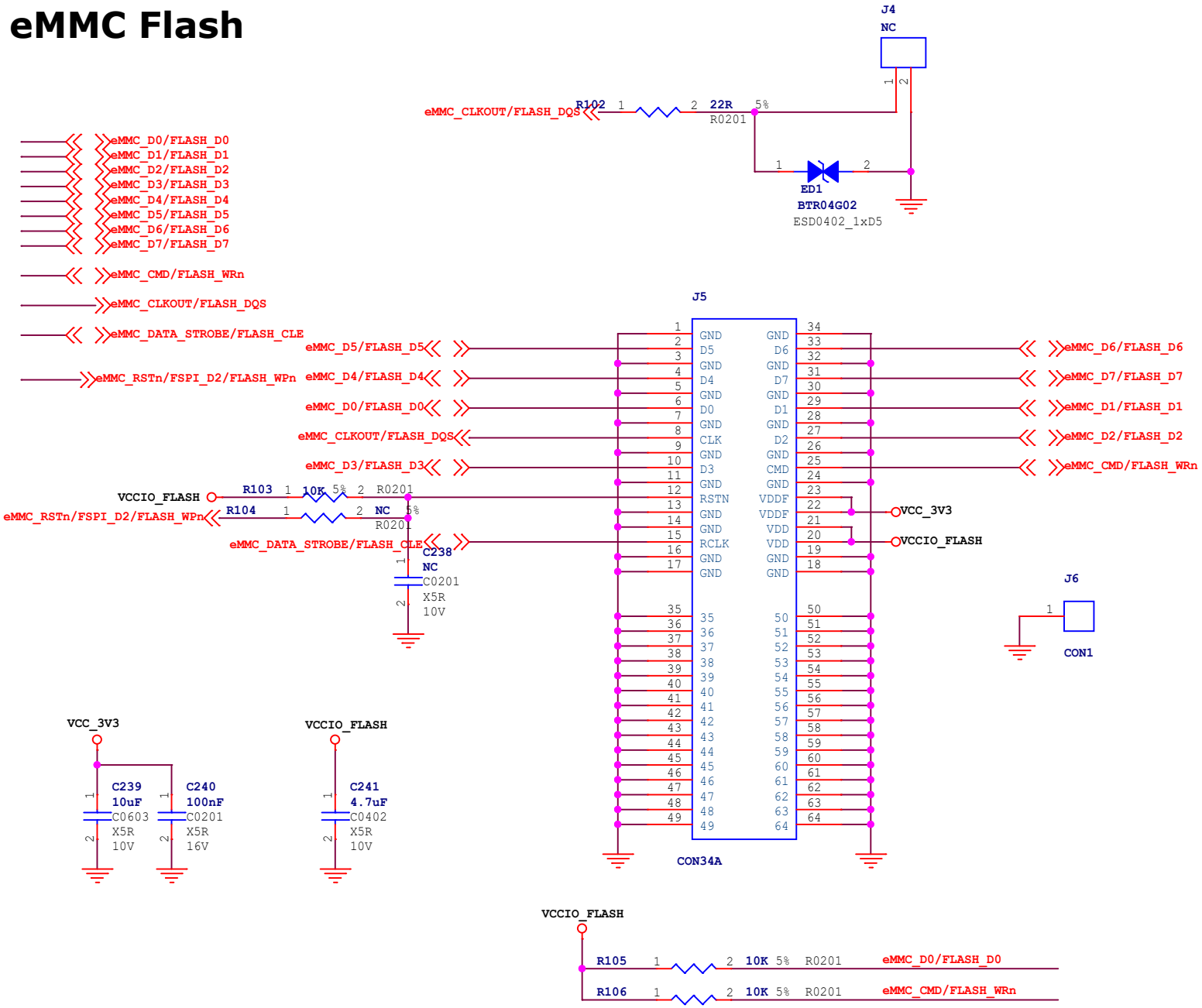
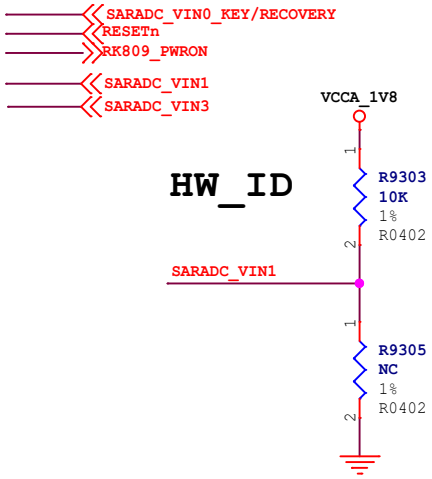
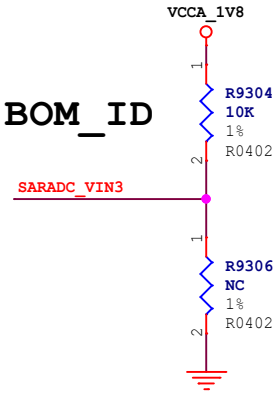
eMMC Flash



Size	Title:	Gong Le	REV
A4	Page Name:	eMMC Flash	V1.1
Date:	Wednesday, July 28, 2021	Sheet 23 of 32	

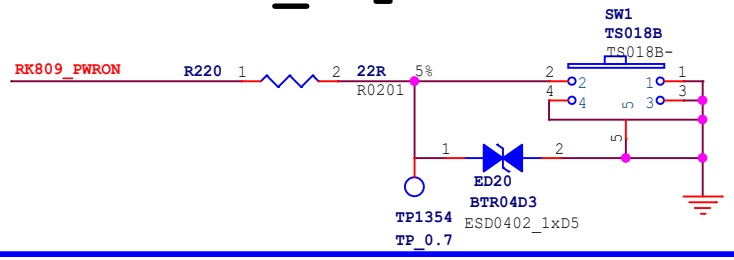


SARADC_VIN1	Up Resistance	Down Resistance
HW_ID0	10K	DNP
HW_ID1	10K	110K
HW_ID2	20K	100K
HW_ID3	33K	100K
HW_ID4	18K	36K
HW_ID5	36K	51K
HW_ID6	51K	51K
HW_ID7	51K	36K
HW_ID8	36K	18K
HW_ID9	100K	33K
HW_ID10	100K	20K
HW_ID11	110K	10K
HW_ID12	DNP	10K

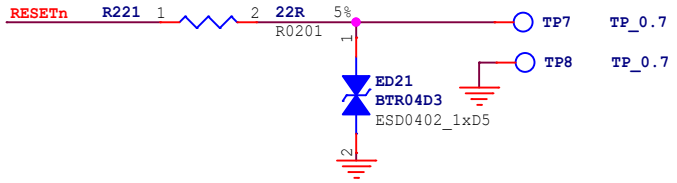


SARADC_VIN3	Up Resistance	Down Resistance
BOM_ID0	10K	DNP
BOM_ID1	10K	110K
BOM_ID2	20K	100K
BOM_ID3	33K	100K
BOM_ID4	18K	36K
BOM_ID5	36K	51K
BOM_ID6	51K	51K
BOM_ID7	51K	36K
BOM_ID8	36K	18K
BOM_ID9	100K	33K
BOM_ID10	100K	20K
BOM_ID11	110K	10K
BOM_ID12	DNP	10K

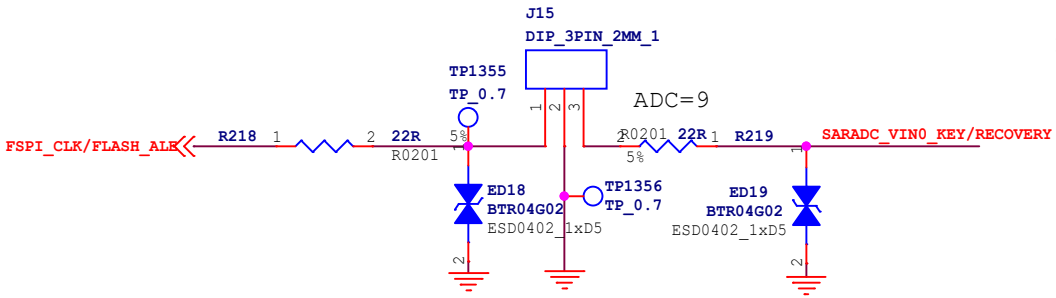
PowerOn/OFF_Key



Reset_Key



RECOVERY



Note:

If there is no Key requirement,
It is suggested to reserve a
SW9200 Key to facilitate the
development debug

RECOVERY_Key function:
If SARADC_VIN0=0V
at after power on and reset,
then system will
enter into loader mode.

Size	Title:	Gong Le	REV
A4	Page Name:	SARADC_KEY	V1.1
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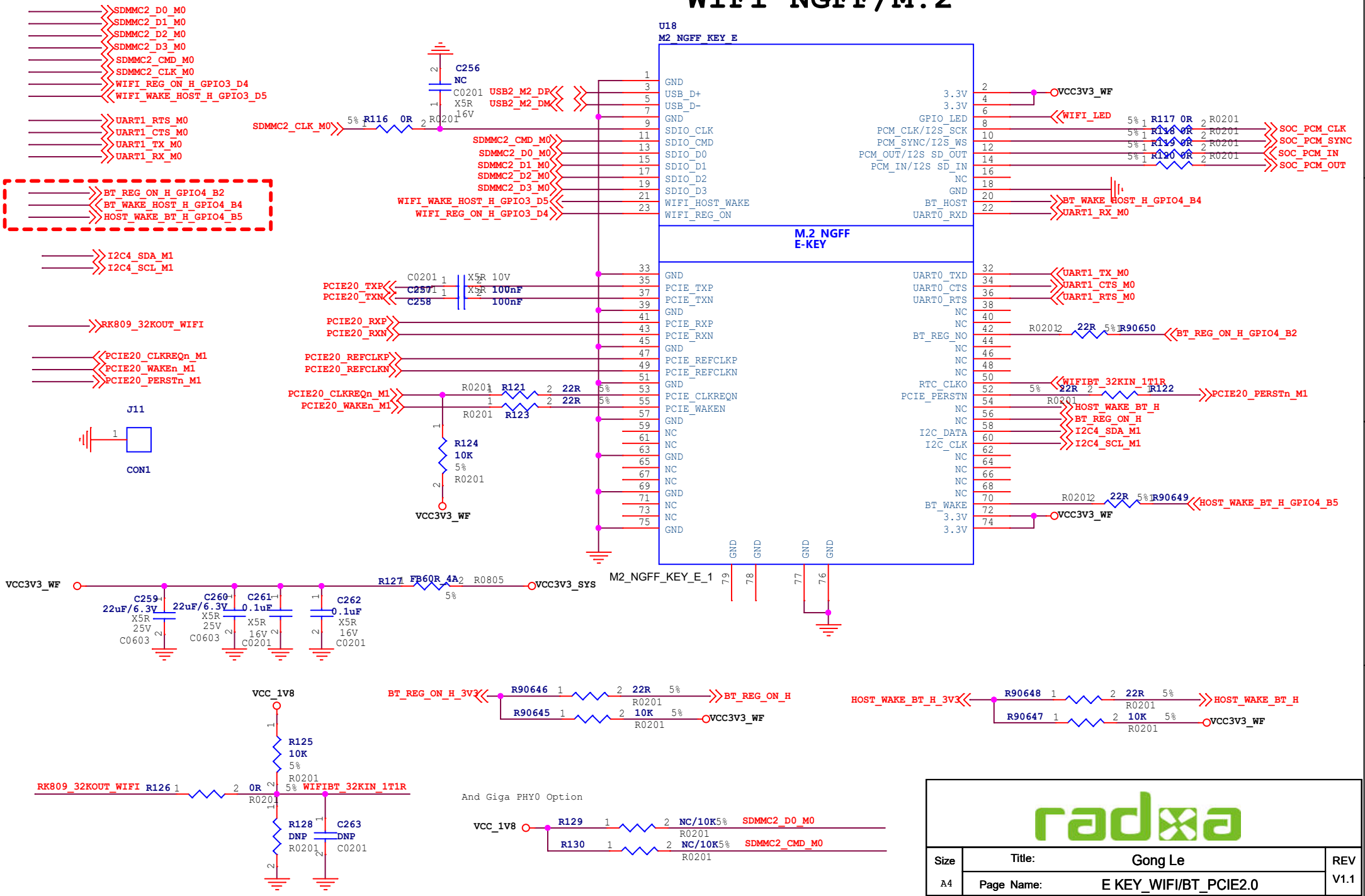
SDIO WIFI/BT MODULE

WIFI NGFF/M.2



Size	Title:	Gong Le	REV
A4	Page Name:	E KEY_WIFI/BT_PCIE2.0	V1.1
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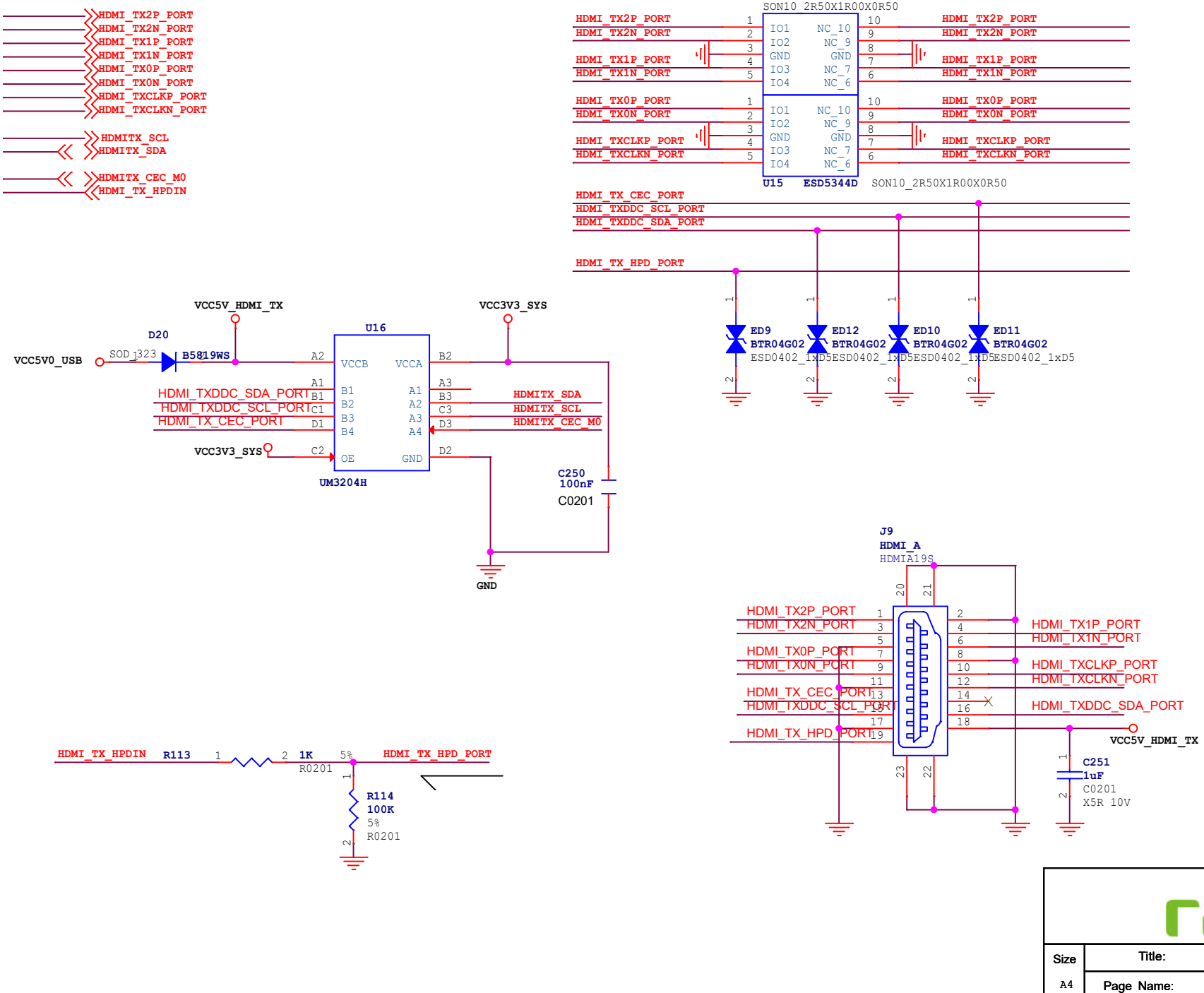
HDMI2.0 TX

Cj<=0.4pF



Size	Title:	Gong Le	REV
A4	Page Name:	HDMI	V1.1
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Giga PHY1

GMAC1_TXD0_M1
GMAC1_TXD1_M1
GMAC1_TXD2_M1
GMAC1_TXD3_M1
GMAC1_TXEN_M1
GMAC1_TXCLK_M1
GMAC1_RXD0_M1
GMAC1_RXD1_M1
GMAC1_RXD2_M1
GMAC1_RXD3_M1
GMAC1_RXDV_CRS_M1
GMAC1_RXCLK_M1
ETH1_REFCLKO_25M_M1
GMAC1_MCLKINOUT_M1
GMAC1_MDC_M1
GMAC1_MDIO_M1
GMAC1_RSTn_GPIO3_B0
GMAC1_INT/PMEB_GPIO3_A7

Y4 25MHz CRY4_3R20X2R50X0R80
R131 22R 5% R0201
C264 8.2pF C0G 50V C0201
C265 8.2pF C0G 50V C0201
R132 NC 5% R0201
R133 NC R0201 5%
PHY1_XTALOUT
PHY1_XTALIN
ETH1_REFCLKO_25M_M1
R134 NC R0201 5%
C266 DNP C0201

GMAC1_MCLKINOUT_M1
R135 33R 5% R0201
R136 120R 5% R0201
PHY1_CLKOUT125
3.3Vpp
MAC <----- PHY

MDI0+ MDI0- FB6 BCMEF122P900H GMDG-6PIN_ESD
MDI1+ MDI1- FB7 BCMEF122P900H GMDG-6PIN_ESD
MDI2+ MDI2- FB8 BCMEF122P900H GMDG-6PIN_ESD
MDI3+ MDI3- FB9 BCMEF122P900H GMDG-6PIN_ESD
TP1332 TP_0.7 PHY1_MDI0+ PHY1_MDI0-
TP1333 TP_0.7 PHY1_MDI1+ PHY1_MDI1-
TP1334 TP_0.7 TP1335 TP_0.7 PHY1_MDI2+ PHY1_MDI2-
TP1336 TP_0.7 TP1337 TP_0.7 PHY1_MDI3+ PHY1_MDI3-
TP1338 TP_0.7 TP1339 TP_0.7

J12
PHY1_MDI0+ PHY1_MDI0- PHY1_MDI1+ PHY1_MDI1- PHY1_MDI2+ PHY1_MDI2- PHY1_MDI3+ PHY1_MDI3-
MDI0+ MDI0- MDI1+ MDI1- MDI2+ MDI2- MDI3+ MDI3- TCT TCT1
C267 C0201 100nF X5R 16V
PHY1_LED_G+ PHY1_G_LED- PHY1_Y_LED+ PHY1_Y_LED-
G+ G- Y+ Y-
VC1 VC2 VC3 VC4
J13 TP1342 TP_0.7 TP1343 TP_0.7 HR911130C RJ45_HRK1
TP1340 TP_0.7 TP1341 TP_0.7 CON4A
TR0 TR1 TR2 TR3

VDD10_PHY1
R142 2.49K 1% R0201
VCC3V3_PHY1
RSET1
PHY1_XTALOUT1
PHY1_XTALIN
PHY1_CLKOUT125
PHY1_LED2/CFG_LDO1
PHY1_LED1/CFG_LDO0
PHY1_LED0/CFG_EXT
R150 0R 5% R0201 GMAC1_INT/PMEB_GPIO3_A7

U19
E_Pad
AVDD33 RSET AVDD10 XTAL_OUT/EXT_CLK XTAL_IN CLKOUT LED2/CFG_LDO1 LED1/CFG_LDO0 LED0/CFG_EXT INTB/PMEB
MDI0+ MDI0- MDI1+ MDI1- MDI2+ MDI2- MDI3+ MDI3-
MDI[0]+ MDI[0]- AVDD10 MDI[1]+ MDI[1]- MDI[2]+ MDI[2]- AVDD10 MDI[3]+ MDI[3]-
REG_OUT DVDD33 DVDD_RG RXC/PHYAD1 RXCTL/PHYAD2 RXD0/RXDLY RXD1/TXDLY RXD2/PLLOFF RXD3/PHYAD0 DVDD10
PHY1_REG_OUT VCC3V3_PHY1 VCCIO_PHY1 PHY1_RXCLK/PHYAD1 GMAC1_RXDV_CRS_M1 GMAC1_RXD0_M1 GMAC1_RXD1_M1 GMAC1_RXD2_M1 GMAC1_RXD3_M1 VDD10_PHY1
AVDD33 PHYRSTB MDC MDIO TXD3 TXD2 TXD1 TXD0 TXCTL TXC
PHY1_RSTn GMAC1_MDC_M1 GMAC1_MDIO_M1 GMAC1_TXD3_M1 GMAC1_TXD2_M1 GMAC1_TXD1_M1 GMAC1_TXD0_M1 GMAC1_TXCLK_M1

RTL8211F-CG
QFN40_5R00X5R00X0R90_T
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial

VCC3V3_PHY1
R167 NC/10K 5% R0201
GMAC1_RSTn_GPIO3_B0
R168 0R 5% R0201
PHYRSTB is 3.3V IO
R169 1.8K 5% R0201 VCCIO_PHY1
C284 100nF X5R 10V C0201

GMAC1_TXCLK
R170 22R 5% R0201 GMAC1_TXCLK_M1
C290 DNP C0201
PHY1_RXCLK/PHYAD1
R171 22R 5% R0201 GMAC1_RXCLK_M1
C291 DNP C0201
Close to PHY

R137 4.7K 5% R0201 PHY1_LED0/CFG_EXT
R138 NC/4.7K 5% R0201 VCC3V3_PHY1
R139 NC/4.7K 5% R0201 PHY1_LED2/CFG_LDO1
R140 4.7K 5% R0201
R141 4.7K 5% R0201 PHY1_LED1/CFG_LDO0
VCC_PHY0_IO Voltage Config

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V	1'b1	2'b00	
External 1.8V	1'b1	2'b10	
Internal 1.8V(default)	1'b0	2'b10	

R143 0R 5% R0201 PHY1_LED2/CFG_LDO1
R147 NC 5% R0201
R151 NC 5% R0201 PHY1_LED0/CFG_EXT
Reserve for EMI.
C270 1000pF C0G 50V C0201
R144 NC 5% R0201
R145 510R 5% R0201 PHY1_Y_LED+
VCC3V3_PHY1
R153 NC 5% R0201
PHY1_LED_G+
C271 1000pF 50V C0G C0201
R154 NC 5% R0201
R155 0R 5% R0201
R158 510R 5% R0201 PHY1_G_LED-
PHY1_LED1/CFG_LDO0
C272 1000pF C0G 50V C0201
Reserve for EMI.

R149 4.7K 5% R0201 PHY1_RXCLK/PHYAD1
R146 4.7K 5% R0201 VCCIO_PHY1
R148 NC/4.7K 5% R0201
R152 4.7K 5% R0201 GMAC1_RXDV_CRS_M1
PHY Address Config

PHY Address	PHYAD[2:0]
1 (default)	3'b001

R156 4.7K 5% R0201 GMAC1_RXD0_M1
R157 NC/4.7K 5% R0201 VCCIO_PHY1
Pull-up for additional 2ns delay to RXC for data latching

R159 4.7K 5% R0201 GMAC1_RXD1_M1
R160 NC/4.7K 5% R0201 VCCIO_PHY1
Pull-up for additional 2ns delay to TXC for data latching

R162 NC/4.7K 5% R0201
R163 4.7K 5% R0201 VCCIO_PHY1
GMAC1_RXD2_M1
Pull-up to disable PLL @ ALDPS mode(Low power mode)

PHY1_REG_OUT
L13 2.2uH IND_252010
C277 4.7uF X5R 10V C0402
C278 100nF X5R 10V C0201
Close to PIN30
VDD10_PHY1
R165 0R R0603 5%
Close to PIN21
C279 100nF X5R 10V C0201
C285 100nF X5R 10V C0201
C286 100nF X5R 10V C0201
C287 100nF X5R 10V C0201
Close to PIN3,8,38
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial

Note:
According to the actual choice of mounted Cannot be mounted at the same time

VCC_1V8
R161 0R 5% R0402
VCCIO_PHY1
VCC_3V3
R164 NC 5% R0402
C273 1uF 6.3V X5R C0201
C274 4.7uF 6.3V X5R C0402
C275 1uF 6.3V X5R C0201
C276 100nF X5R 10V C0201
Close to PIN28

VCC_3V3
R166 0R 5% R0402
VCC3V3_PHY1
C280 4.7uF X5R 6.3V C0402
C281 100nF X5R 10V C0201
C283 100nF X5R 10V C0201
Close to PIN11,40
C288 4.7uF X5R 6.3V C0402
C289 100nF X5R 10V C0201
Close to PIN29

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Size	Title:	Gong Le	REV
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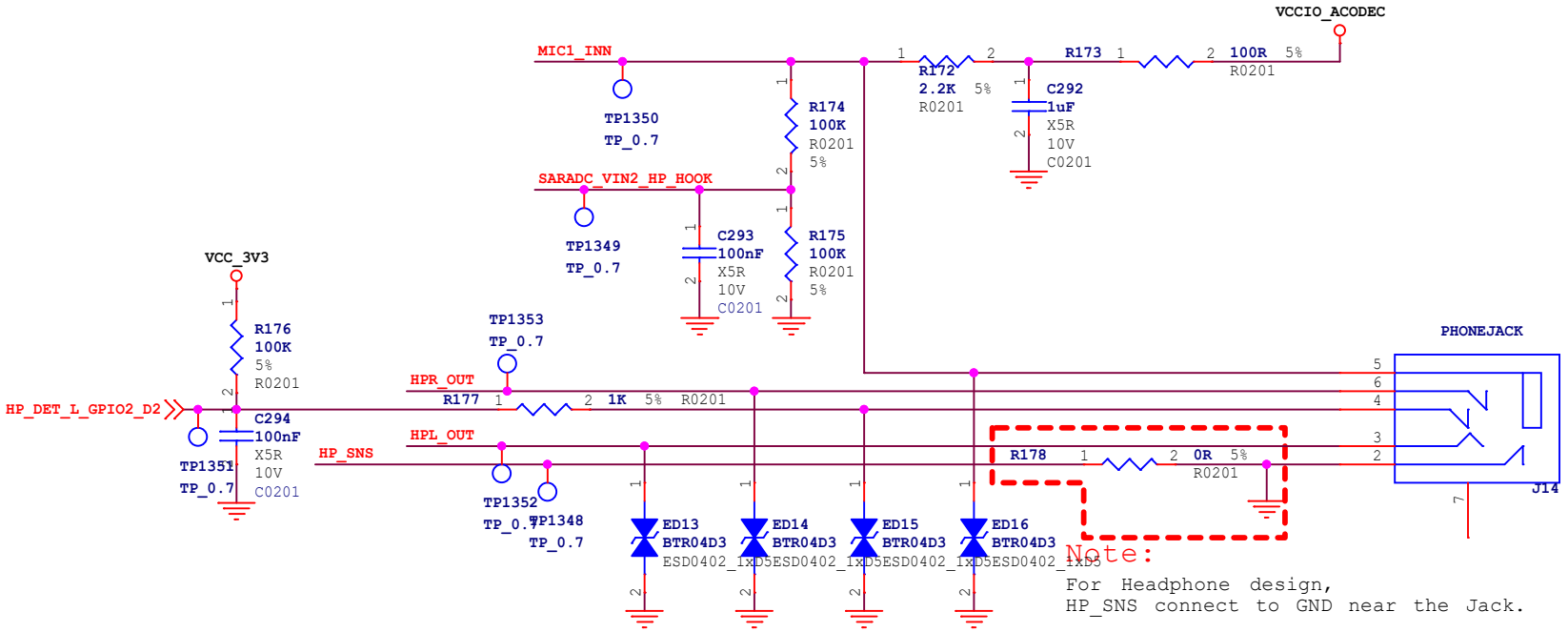
HPL_OUT
HP_SNS
HPR_OUT
HP_DET_L_GPIO2_D2
MIC1_INN
SARADC_VIN2_HP_HOOK

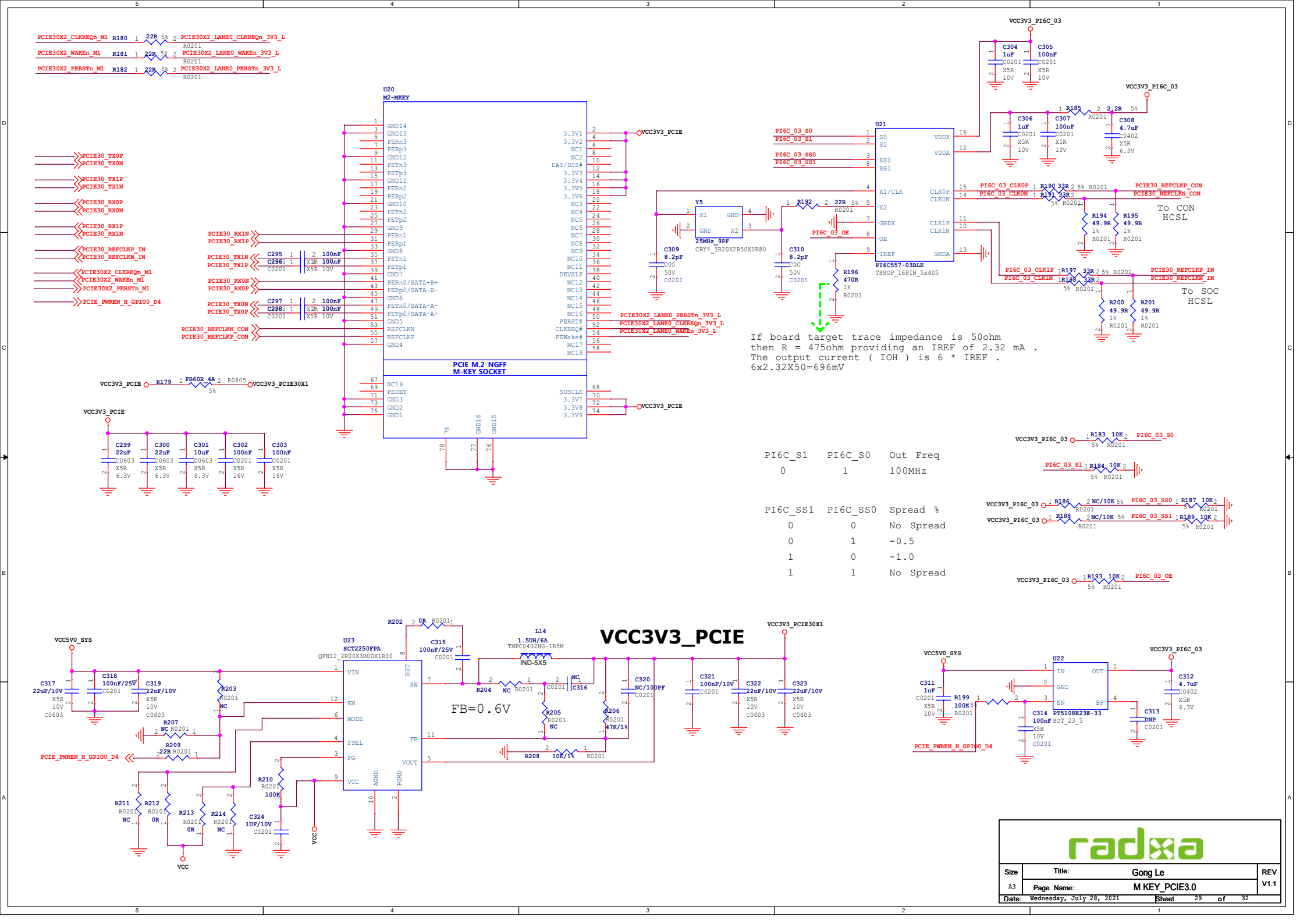
Headphone Jack(4-pole with DET & MIC)

Option



Note:
For Headphone design,
HP_SNS connect to GND near the Jack.

Size: A4	Title: Gong Le	REV: V1.1
	Page Name: Headphone	
Date: Wednesday, July 28, 2021	Sheet 28 of 32	


PCIE30X2_CLKREQn_M1
PCIE30X2_WAKEn_M1
PCIE30X2_PERSTn_M1
PCIE30X2_LANE0_CLKREQn_3V3_L
PCIE30X2_LANE0_WAKEn_3V3_L
PCIE30X2_LANE0_PERSTn_3V3_L
PCIE30_TX0P
PCIE30_TX0N
PCIE30_TX1P
PCIE30_TX1N
PCIE30_RX0P
PCIE30_RX0N
PCIE30_RX1P
PCIE30_RX1N
PCIE30_REFCLKP_IN
PCIE30_REFCLKN_IN
PCIE30X2_CLKREQn_M1
PCIE30X2_WAKEn_M1
PCIE30X2_PERSTn_M1
PCIE_PWREN_H_GPIO0_D4
PCIE30_REFCLKN_CON
PCIE30_REFCLKP_CON
U20
M2-MKEY
PCIE M.2 NGFF
M-KEY SOCKET
VCC3V3_PCIE
VCC3V3_PCIE30X1
U21
PI6C557-03BLE
TSSOP_16PIN_5x4D5
PI6C_03_S0
PI6C_03_S1
PI6C_03_SS0
PI6C_03_SS1
PI6C_03_OE
PI6C_03_CLK0P
PI6C_03_CLK0N
PI6C_03_CLK1P
PI6C_03_CLK1N
To CON HCSL
To SOC HCSL
Y5
25MHz_9PF
CRY4_3R20X2R50X0R80
If board target trace impedance is 50ohm
then R = 475ohm providing an IREF of 2.32 mA .
The output current (IOH) is 6 * IREF .
6x2.32X50=696mV
PI6C_S1 PI6C_S0 Out Freq
0 1 100MHz
PI6C_SS1 PI6C_SS0 Spread %
0 0 No Spread
0 1 -0.5
1 0 -1.0
1 1 No Spread
VCC5V0_SYS
U23
SCT2250FPA
QFN12_2R00X3R00X1R00
L14
1.5UH/6A
TMPC0402HG-1R5M
IND-5X5
FB=0.6V
VCC3V3_PCIE
U22
PT5108E23E-33
SOT_23_5
PCIE_PWREN_H_GPIO0_D4
Size A3
Title: Gong Le
Page Name: M KEY_PCIE3.0
REV V1.1
Date: Wednesday, July 28, 2021
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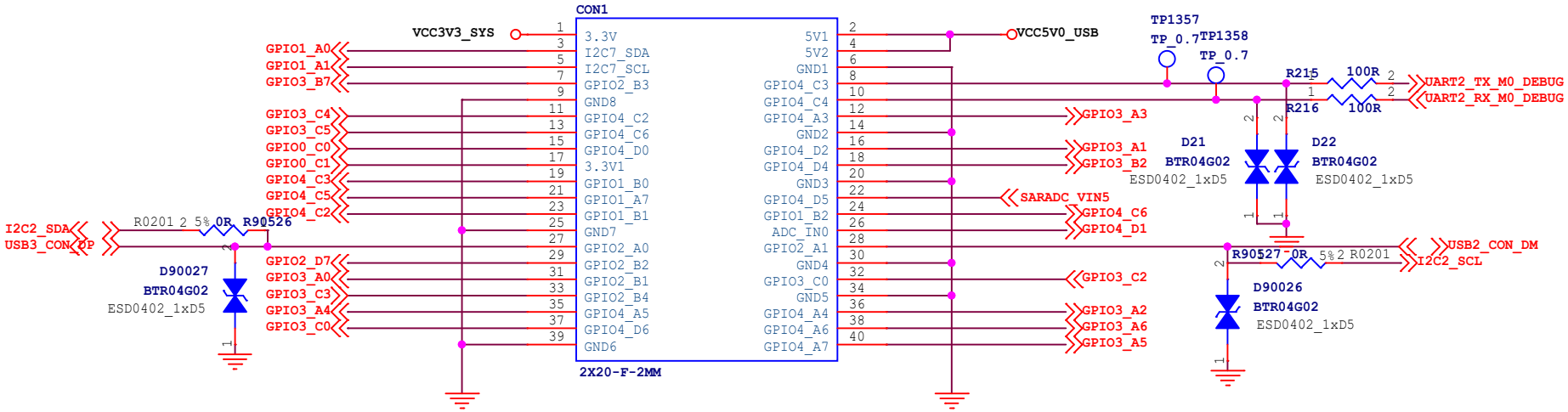
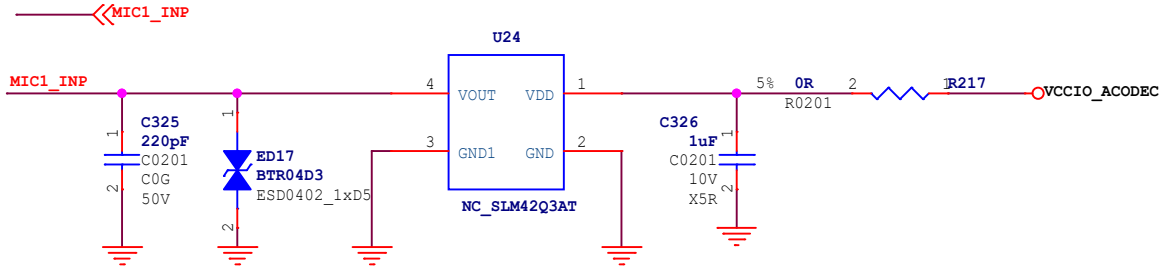


MIC



Size A4	Title: Gong Le		REV V1.1
	Page Name: CONNECT		
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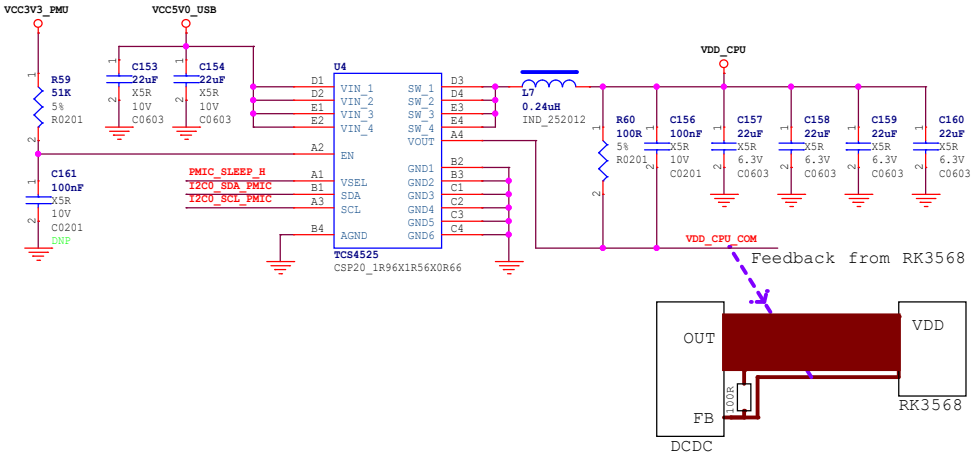
I2C0_SCL_PMIC
I2C0_SDA_PMIC
PMIC_SLEEP_H
VDD_CPU_COM
RTCIC_INT_L_GPIO0_D3
RTCIC_32KOUT
I2C5_SCL_M0
I2C5_SDA_M0
LCD0_PWREN_H_GPIO0_C7
RK809_PWRON

VDD_CPU

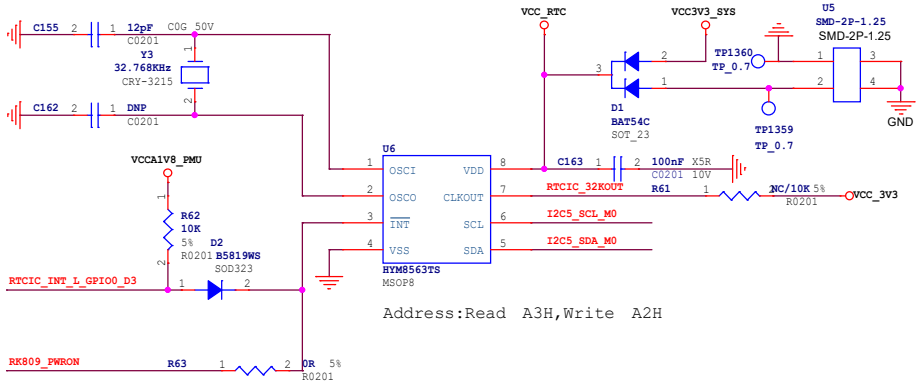


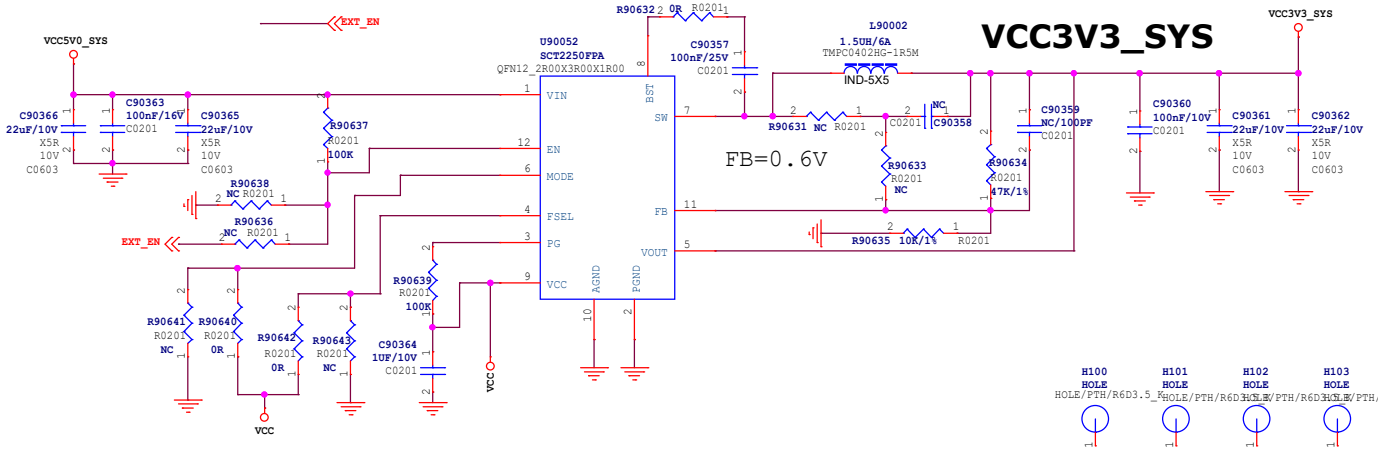
RTC IC --Option

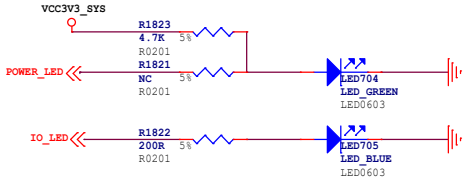
Note:

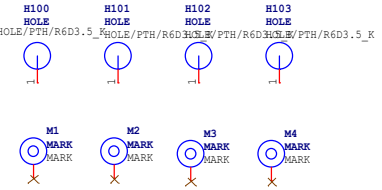
The power off hold time scheme is required,
It is recommended to use external RTC IC

But, it will not support the timing poweron function









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Size	Title:	Gong Le	REV
A3	Page Name:	Power_CPU_RTC	V1.1
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I2C0_SCL_PMIC
I2C0_SDA_PMIC
PMIC_INT_L
PMIC_SLEEP_H
RK809_32KOUT_WIFI
RESETn
RK809_PWRON
I2S1_MCLK_M0_RK809
I2S1_SCLK_TX_M0_RK809
I2S1_LRCK_TX_M0_RK809
I2S1_SDO0_M0_RK809
I2S1_SDI0_M0/PDM_SDI0_M0_RK809
PDM_CLK0_M0_RK809
EXT_EN
HPL_OUT
HP_SNS
HPR_OUT
MIC1_INP
MIC1_INN

OUT
VDD
FB
100R
RK3568
BUCK4

PMIC RK809 DCDC

VCC3V3_SYS
U3A
VDD_LOGIC
C103 2 1 22uF X5R 6.3V C0603
C104 1 2 10uF X5R 10V C0603
VDD_NPU
C108 100nF X5R 10V C0201
R46 100R 5% R0201
C109 22uF X5R 6.3V C0603
C110 22uF X5R 6.3V C0603
L2 470nH SW1 IND_252010 DCR<50mohm ON 0.9V
L3 470nH SW4 IND_252010 DCR<50mohm OFF 0.9V
C111 22uF X5R 6.3V C0603
C112 22uF X5R 6.3V C0603
R47 100R 5% R0201
C114 100nF X5R 10V C0201
VDD_LOGIC
Feedback from RK3568
VDD_GPU
L4 470nH SW2 IND_252010 DCR<50mohm ON 0.9V
C118 1 2 10uF X5R 10V C0603
VCC_DDR
C120 100nF X5R 10V C0201
R48 100R 5% R0201
C121 22uF X5R 6.3V C0603
C122 22uF X5R 6.3V C0603
L5 470nH SW3 IND_252010 DCR<50mohm
C123 22uF X5R 6.3V C0603
C124 10uF X5R 10V C0603
VDD_GPU
Feedback from RK3568
VCC1 BUCK1 SW1 FB1 2.5A 0.5-2.4V
BUCK4 VCC4 SW4 FB4 1.5A 0.5-3.4V
VCC2 BUCK2 SW2 FB2 2.5A 0.5-2.4V
BUCK3 VCC3 SW3 FB3 1.5A 0.5-2.4V
VBUCK3
FB3=0.8V
RK809-5
QFN68_7R00X7R00X0R80_T
R49 47K 1% R0201
Default DDR4
FB=0.8V
R50 120K 1% R0201

DDR4	1.21V	62K 1%
LPDDR4/4x	1.11V	47K 1%
DDR3	1.53V	110K 1%
DDR3L	1.35V	82K 1%
LPDDR3	1.25V	68K 1%

VDD Pin
OUT
FB
100R
RK3568
BUCK1/BUCK2

PMIC RK809 LDO

U3B
VCC3V3_SYS
400mA LDO: 400mA@Vin>3V 200mA@Vin>2V
Default ON/OFF
VCC5 LDO1 400mA
VCC6 LDO2 400mA
Low noise LDO3 100mA
Codec vddio LDO4 400mA
LDO5 400mA
VCC7 LDO6 400mA
LDO7 400mA
LDO8 400mA
LDO9 400mA
VCC8 2.1A SWOUT2
2.1A SWOUT1
VCC8\9: 2.7V-5.5V
VCC9 BUCK5 1.5V-3.6V 2.5A SW5 FB5
RK809-5
QFN68_7R00X7R00X0R80_T
OFF 0.9V
ON 0.9V
OFF 3.3V
ON 3.3V
ON 1.8V
OFF 1.8V
C98 1uF X5R 6.3V C0201 VDDA0V9_IMAGE
C100 1uF X5R 6.3V C0201 VDDA_0V9
C101 1uF X5R 6.3V C0201 VDDA0V9_PMU
C102 4.7uF X5R 6.3V C0402 VCCIO_ACODEC
C106 1uF X5R 6.3V C0201 VCCIO_SD
C107 1uF X5R 6.3V C0201 VCC3V3_PMU
C113 1uF X5R 6.3V C0201 VCCA_1V8
C116 1uF X5R 6.3V C0201 VCCA1V8_PMU
C117 1uF X5R 6.3V C0201 VCCA1V8_IMAGE
C119 1uF X5R 6.3V C0201 VCC3V3_SD
C126 10uF X5R 10V C0603 VCC_3V3
C99 1uF X5R 6.3V C0201
C105 1uF X5R 6.3V C0201
C115 1uF X5R 10V C0201
C125 1uF X5R 6.3V C0201
C129 10uF X5R 10V C0603
L6 470nH IND_252010 DCR<50mohm
VCC_1V8
C127 22uF X5R 6.3V C0603
C128 22uF X5R 6.3V C0603
R51 2 1 DNP R0201
R52 2 1 0R 5% R0201
C130 2 1 1uF X5R 6.3V C0201 VDDA_0V9 FB1 0.030ohm L0402 120R-100MHz USB_AVDD_0V9
C131 2 1 1uF X5R 6.3V C0201 VCCA_1V8 FB2 0.030ohm L0402 120R-100MHz USB_AVDD_1V8
C132 2 1 1uF X5R 6.3V C0201 VDDA0V9_IMAGE FB3 0.030ohm L0402 120R-100MHz MIPI_AVDD_0V9
C133 2 1 1uF X5R 6.3V C0201 VCCA1V8_IMAGE FB4 0.030ohm L0402 120R-100MHz MIPI_AVDD_1V8

PMIC RK809 Management

U3C
VCC3V3_SYS
C134 2 1 1uF X5R 10V C0201 RK809_VREF
C135 1 2 1uF X5R 10V C0201
VREF VCC_RTC
GNDREF
ePAD
XIN
XOUT
BATDIV
Gas Gauge
SNSP
SNSN
SDA
SCL
INT
SLEEP
CLK32K
RESETB
EXT_EN
VDC
PWRON
30K
VCC12V_DCIN
R55 100K 5% R0201
R57 27K 5% R0201
1.2V
C148 100nF X5R 10V C0201
RK809_VDC
RK809_PWRON
C150 100nF X5R 10V C0201
RK809-5
QFN68_7R00X7R00X0R80_T
Note:
If the external RTC IC is used,
Can choose not mounted
C137 2 1 22pF C0G 50V C0201
Y2 32.768KHz CRY-3215
C142 2 1 22pF C0G 50V C0201
I2C0_SDA_PMIC R53 22R 5% R0201 SDA_809
I2C0_SCL_PMIC R54 22R 5% R0201 SCL_809
PMIC_INT_L
PMIC_SLEEP_H
RK809_32KOUT_WIFI R56 0R 5% R0201 RK809_CLK32KOUT
VCC3V3_PMU R58 10K 5% R0201 RESETn
C149 100nF X5R 10V C0201

PMIC RK809 CODEC

VCC5V0_USB
FB5 1 2 120R-100MHz L0603 2A
U3D
C136 2 1 10uF X5R 10V C0603
C138 2 1 2.2uF X5R 10V C0201
C139 2 1 1uF X5R 6.3V C0201 VCC_CPVDD
C141 2 1 2.2uF X5R 10V C0201 VCC_CPVSS
C143 2 1 1uF X5R 6.3V C0201 VCC_1P8D
C144 2 1 1uF X5R 6.3V C0201 VCC_1P8A
VCC_SPK_HP
CPn
CPp
VCC_CPVDD
VCC_CPVSS
VCC_1P8D
Power from VCC_RTC
VCC_1P8A
I2S1_MCLK_M0_RK809
I2S1_SCLK_TX_M0_RK809
I2S1_LRCK_TX_M0_RK809
I2S1_SDO0_M0_RK809
I2S1_SDI0_M0/PDM_SDI0_M0_RK809
PDM_CLK0_M0_RK809
MCLK
BCLK
LRCLK
SDI
SDO/PDMDATA
PDMCLK
IO Power =LDO4
HPL_OUT
HP_SNS
HPR_OUT
SPK_OUTn
SPK_OUTp
MIC1p MIC_L
MIC1n MIC_R
HPL_OUT
HP_SNS
HPR_OUT
SPKN
SPKP
C140 NC C0G 50V C0201
C145 NC C0G 50V C0201
C146 2 1 100nF X5R 10V C0201 MIC1_INP
C147 27pF C0G 50V C0201
C151 2 1 100nF X5R 10V C0201 MIC1_INN
C152 27pF C0G 50V C0201
RK809-5
QFN68_7R00X7R00X0R80_T
Note:
If RK809-5 codec is not used,
then Pin 14,15,16,17,19,40 Tie VSS
Pin 18,36,37,38,35,39,41,34,32,43,42
Leave floating

radxa

Size	Title:	Gong Le	REV
A3	Page Name:	Power_PMIC	V1.1
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