Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2021-06-01		1:Revision preliminary version	
V1.1	2021-06-29			
V1.2	2021-07-24			
V1.3	2021-09-13			

Size: A4	Title: Gong Le	REV: V1.3
	Page Name: Revision History	
Date: Friday, September 10, 2021	Sheet 01 of 33	

Table of Content

Description

Note

Option

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Notes

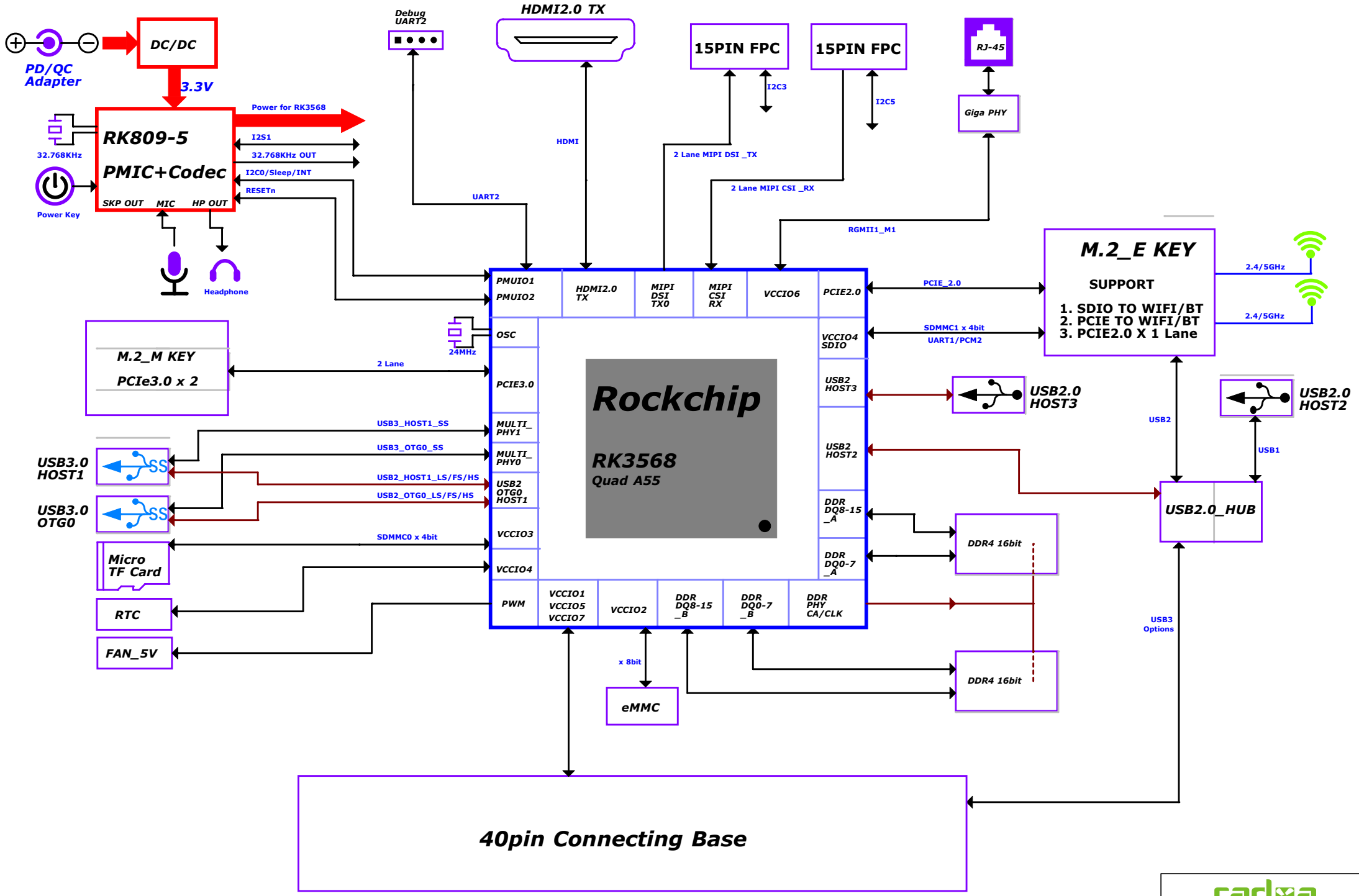
NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

radxa

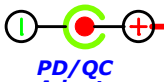
Size	Title:	Gong Le	REV
A3	Page Name:	Index and Notes	V1.3
Date: Friday, September 10, 2021	Sheet 02 of 33		

Gong Le Ref Block Diagram



Size A2	Title: Gong Le Page Name: Block Diagram	REV V1.3
Date: Friday, September 10, 2021	Sheet 03 of 33	

Default Power Diagram



PD/QC Adapter

DC/DC 3000mA Seq:0 Max:

VCC3V3_SYS

RK809-5

Power on Sequence

VCC1	BUCK1 0.5V~2.4V, 2.5A max	Seq:1	VDD_LOGIC Max:	RK3568_Logic	
VCC2	BUCK2 0.5V~2.4V, 2.5A max	Seq:2	VDD_GPU Max:	RK3568_GPU	
VCC3	BUCK3 0.5V~2.4V, 1.5A max	Seq:3	VCC_DDR Max:	RK3568_DDRC DRAM	
VCC4	BUCK4 0.5V~3.4V, 1.5A max	OFF	VDD_NPU Max:	RK3568_NPU	
	LDO1 0.6V~3.4V, 400mA max	OFF	VDDA0V9_IMAGE Max:	MIPI_CSI_RX_AVDD_0V9 Max: MIPI_DSI_TX0/LVDS_TX0_AVDD_0V9 Max: MIPI_DSI_TX1_AVDD_0V9 Max: EDP_TX_AVDD_0V9 Max: HDMI_TX_AVDD_0V9 Max:	
VCC5	LDO2 0.6V~3.4V, 400mA max	Seq:1	VDDA_0V9 Max:	SYSPLL_AVDD_0V9 Max: USB2_AVDD_0V9 Max: USB3_AVDD_0V9 Max: MULTI_PHY_AVDD_0V9 Max: PCIE30_AVDD_0V9 Max:	
	LDO3 0.6V~3.4V, 100mA max	Seq:1	VDDA0V9_PMU Max:	PMU_VDD_LOGIC_0V9 Max: PMUPLL_AVDD_0V9 Max:	
	LDO4(Codec VDDIO) 0.6V~3.4V, 400mA max	OFF	VCCIO_ACODEC Max:	VCCIO1--I2S1/PDM MIC/PDM ADC	
VCC6	LDO5 0.6V~3.4V, 400mA max	Seq:4	VCCIO_SD Max:	VCCIO3--SDMMC0	
	LDO6 0.6V~3.4V, 400mA max	Seq:2	VCC3V3_PMU Max:	PMUIO1/ PMUIO2	
	LDO7 0.6V~3.4V, 400mA max	Seq:2	VCCA_1V8 Max:	SYSPLL_AVDD_1V8 Max: USB2_AVDD_1V8 Max: USB3_AVDD_1V8 Max: MULTI_PHY_AVDD_1V8 Max: PCIE30_AVDD_1V8 Max: SARADC_AVDD_1V8 Max:	
VCC7	LDO8 0.6V~3.4V, 400mA max	Seq:2	VCCA1V8_PMU Max:	PMUPLL_AVDD_1V8 VCC1V8_DDR	
	LDO9 0.6V~3.4V, 400mA max	OFF	VCCA1V8_IMAGE Max:	MIPI_CSI_RX_AVDD_1V8 Max: MIPI_DSI_TX0/LVDS_TX0_AVDD_1V8 Max: MIPI_DSI_TX1_AVDD_1V8 Max: EDP_TX_AVDD_1V8 Max: HDMI_TX_AVDD_1V8 Max: VCC18_LCD(Option) Max:	
VCC8	Switch2 2.1 A max, Rdson=100mΩ	Seq:4	VCC3V3_SD Max:	Micro SD Card	
	Switch1 2.1 A max, Rdson=90mΩ	Seq:4	VCC_3V3 Max:	USB3_AVDD_3V3 Max: USB2_AVDD_3V3 Max: VCCIO5,VCCIO7 Max: eMMC_VCC / Nand_VCC Max: VCC3V3_PHY0/1/2 Max: VCC3V3_TP Max: IR Receiver Max: UART Device Max: RS485 Device Max: CAN IC Max:	
VCC9	BUCK5: 1.5V~3.6V, 2.5 A max	Seq:2	VCC_1V8 Max:	OTP_VCC18 Max: VCCIO2(Default) --eMMC/Nand IO Max: VCCIO4(Default) Max: VCCIO6(Default) Max: GiGa PHY0/1 IO-Option Max: WIFI/BT IO Max:	
VCC_RTC					

VCC5V0_SYS

EXT DC/DC ,5A Seq:2A VDD_CPU Max: RK3568_CPU

EXT LDO ,0.3A Seq:2A VCC2V5_DDR Max: DDR4 DRAM

VCC3V3_SYS

Mos-->LCD Panel Max:
Mos-->VCC3V3_VGA Max:
Mos-->RK628D Max:
WIFI/BT VBAT Max:
LDO-->Camera 1.2V Max:
LDO-->Camera 1.8V Max:
RTC IC Max:

MOS OFF

PCIe Slot Max:
SATA Max:

DC/DC 3000mA Seq:0 VCC5V0_USB Max:

SATA Max:
USB HOST Max:

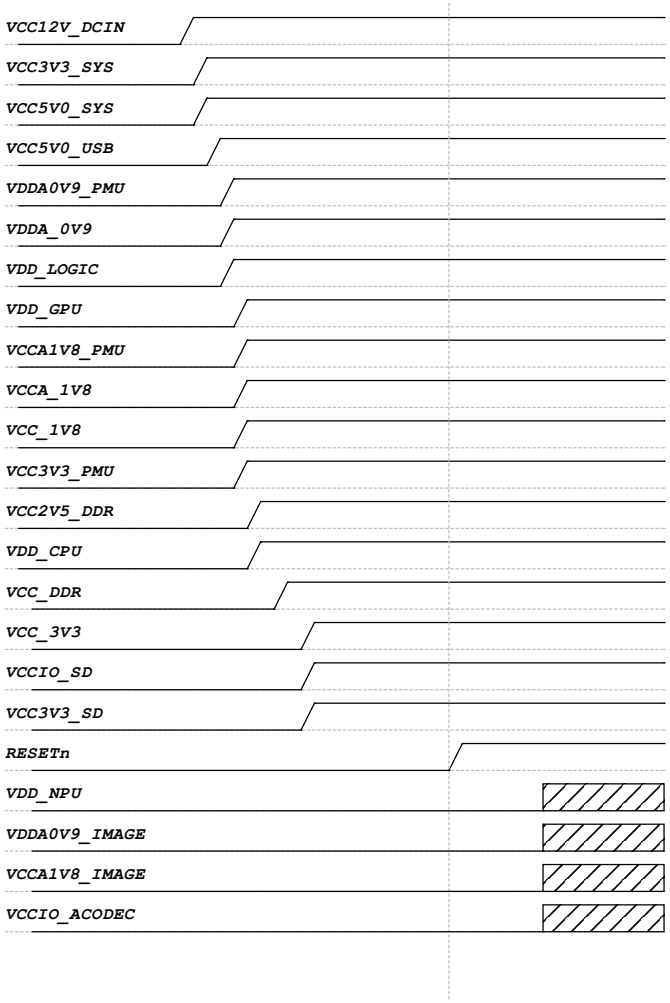
DC/DC 3000mA Seq:0 VCC5V0_SYS Max:

RK809_SPK_PA Max:
MOS → VCC5V0_VGA Max:
LDO → VCC3V3_PI6C Max:
LDO → Camera 2.8V Max:
DDR VTT Max:
LCM Backlight Max:
MOS → VCC5V_HDMI_TX Max:
CAN transceiver IC Max:
EXT SPK PA Max:

DC/DC 3000mA VCC3V3_PCIE Max:

DC/DC 3000mA VCC3V3_MINIPCIE Max:

Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC3V3_SYS	RK809_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	0.9V	TBD	TBD
VCC3V3_SYS	RK809_BUCK2	2.5A	VDD_GPU	Slot:2	0.9V	ON	DVFS	TBD	TBD
VCC3V3_SYS	RK809_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	1.2V (DDR4)	TBD	TBD
VCC3V3_SYS	RK809_BUCK4	1.5A	VDD_NPU	N/A	0V	OFF	DVFS	TBD	TBD
VCC3V3_SYS	RK809_LDO1	0.4A	VDDA0V9_IMAGE	N/A	0V	OFF	0.9V	TBD	TBD
	RK809_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	0.9V	TBD	TBD
	RK809_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	0.9V	TBD	TBD
VCC3V3_SYS	RK809_LDO4	0.4A	VCCIO_ACODEC	N/A	0V	OFF	3.3V	TBD	TBD
	RK809_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	3.3V or 1.8V (SD2.0=3.3V,SD3.0=1.8V)	TBD	TBD
	RK809_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	3.3V	TBD	TBD
VCC3V3_SYS	RK809_LDO7	0.4A	VCCA_1V8	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_LDO8	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_LDO9	0.4A	VCCA1V8_IMAGE	N/A	0V	OFF	1.8V	TBD	TBD
VCC3V3_SYS	RK809_SW2 100mohm	2.1A	VCC3V3_SD	Slot:4	3.3V	ON	3.3V	TBD	TBD
VCC3V3_SYS	RK809_SW1 90mohm	2.1A	VCC_3V3	Slot:4	3.3V	ON	3.3V	TBD	TBD
	RK809_BUCK5	2.5A	VCC_1V8	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_RESETn			Slot:4+5					
VCC12V_DCIN	EXT BUCK	3.0A	VCC3V3_SYS	Slot:0	3.3V	ON	3.3V	TBD	TBD
VCC12V_DCIN	EXT BUCK	3.0A	VCC5V0_SYS	Slot:0	5.0V	ON	5.0V	TBD	TBD
VCC5V0_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	DVFS	TBD	TBD
VCC3V3_SYS	EXT LDO	0.3A	VCC2V5_DDR	Slot:2A	2.5V	ON	2.5V	TBD	TBD

Default IO Power Domain Map

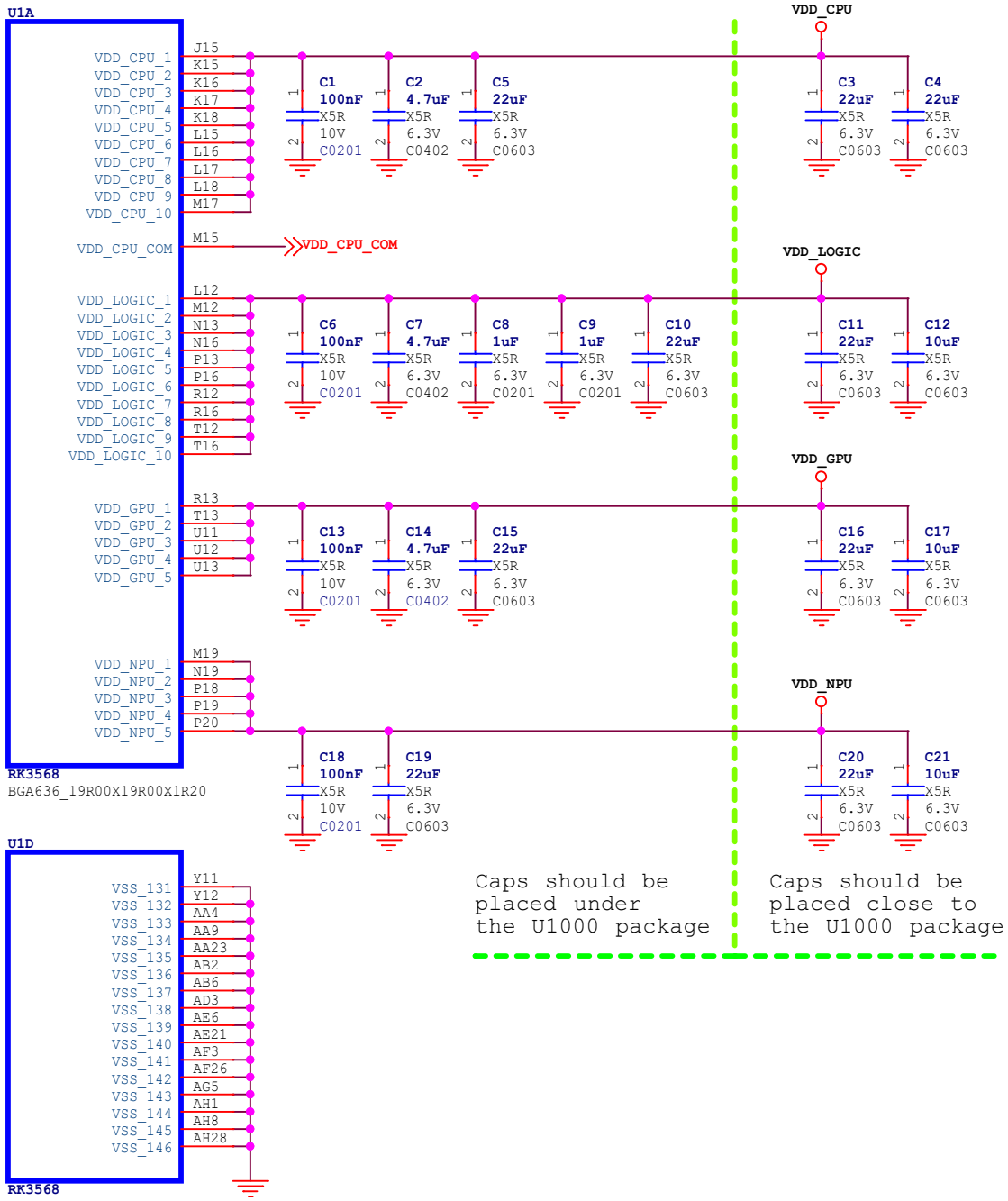
IO Domain	Pin Num	Support IO Voltage		Actual assigned IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	Pin Y20	✓	✗	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	Pin W19	✓	✓	VCC3V3_PMU	VCC3V3_PMU	3.3V	
VCCIO1	Pin H17	✓	✓	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	Pin H18	✓	✓	VCCIO_FLASH	VCC_1V8	1.8V	PIN "FLASH_VOL_SEL" must be logic High if VCCIO_FLASH=3.3V,FLASH_VOL_SEL must be logic low
VCCIO3	Pin L22	✓	✓	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	Pin J21	✓	✓	VCCIO4	VCC_1V8	1.8V	
VCCIO5	Pin V10 Pin V11	✓	✓	VCCIO5	VCC_3V3	3.3V	
VCCIO6	Pin R9 Pin U9	✓	✓	VCCIO6	VCC_1V8	1.8V	
VCCIO7	Pin V12	✓	✓	VCCIO7	VCC_3V3	3.3V	

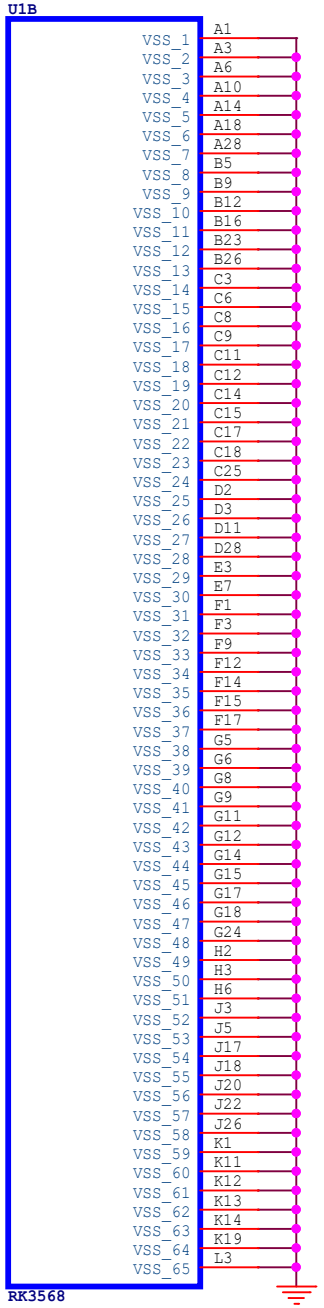
If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

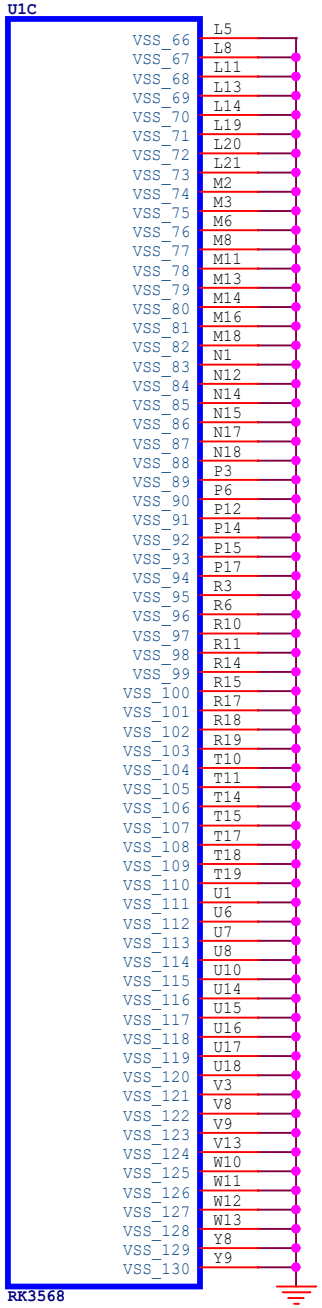
radxa

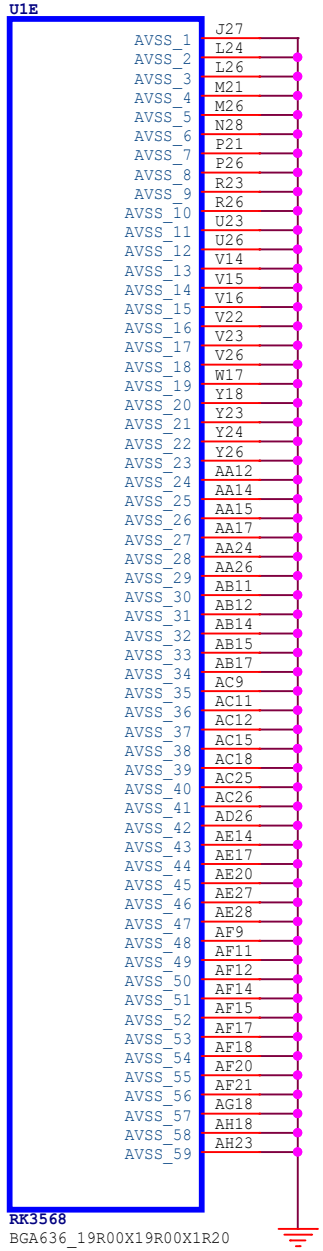
Size	Title:	Gong Le	REV
A3	Page Name:	Power Sequence/IO Domain Map	V1.3
Date:	Friday, September 10, 2021	Sheet 05 of 33	

RK3568_ABCDE (Power&Gnd)





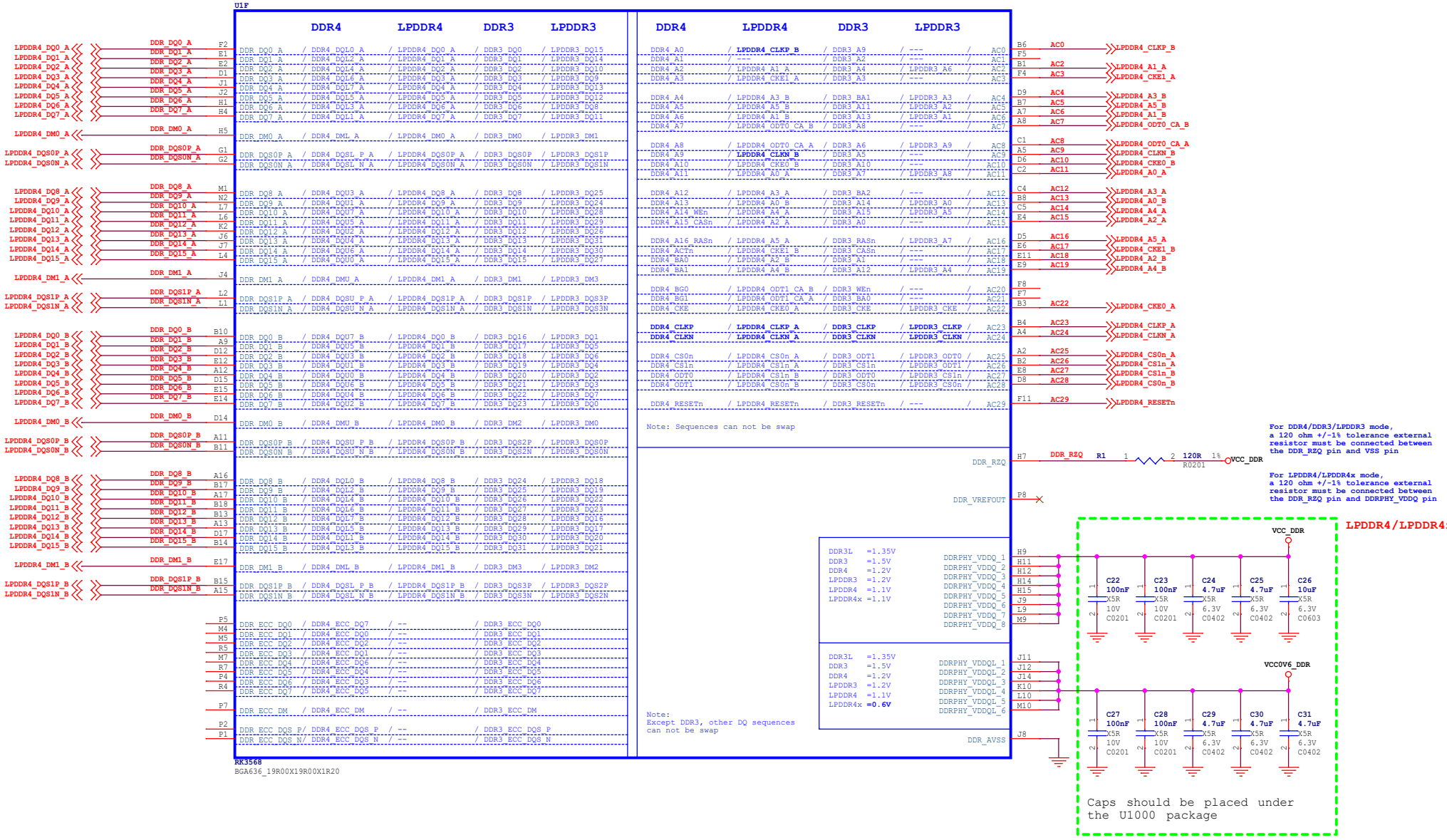




radxa

Size	Title:	Gong Le	REV
A4	Page Name:	RK3568_Power/GND	V1.3
Date:	Friday, September 10, 2021	Sheet 06 of 33	

RK3568_F (DDR PHY)

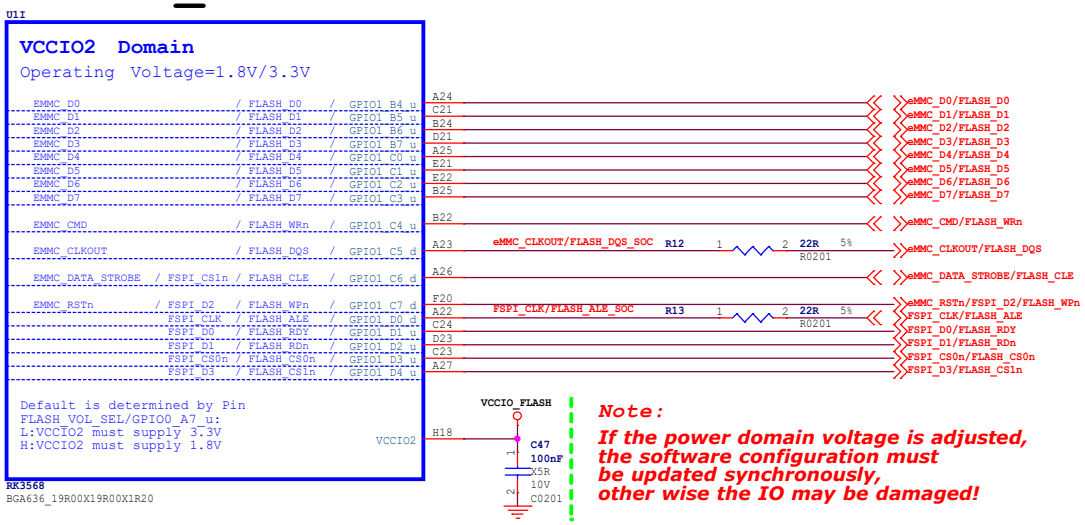


For DDR4/DDR3/LPDDR3 mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_RZQ pin and VSS pin

For LPDDR4/LPDDR4x mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_RZQ pin and DDRPHY_VDDQ pin

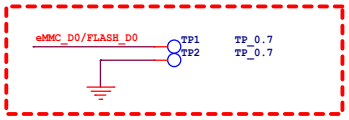
Size A3	Title: Gong Le		REV V1.3
	Page Name: RK3568_DDR PHY		
Date: Friday, September 10, 2021	Sheet 07 of 33		

RK3568_I(VCCIO2 Domain)



Note:

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

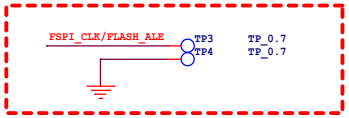


Note:

For eMMC or Nand Flash:
If eMMC_D0/FLASH_D0=0V at after power on and reset, then system will enter into Maskrom mode.

Layout note:

Test point must be placed on the line, and no branch can be added



Note:

For SPI Flash:
If FSPI_CLK=0V at after power on and reset, then system will enter into Maskrom mode.

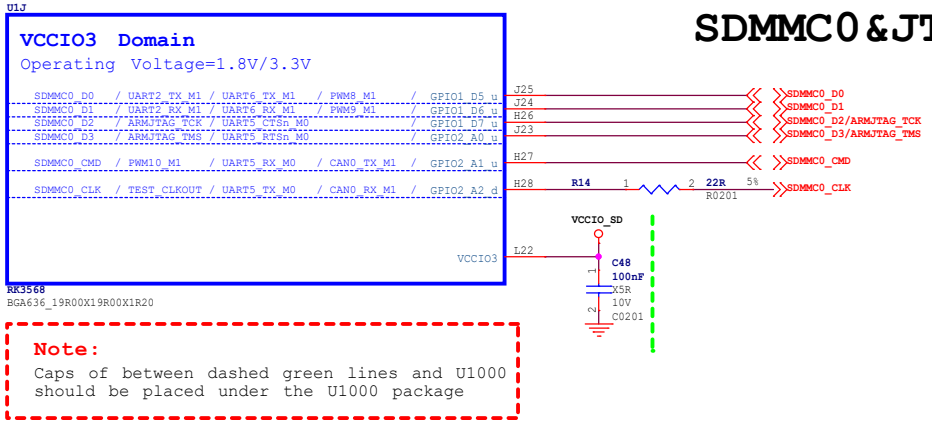
Note:
Reserve TestPoint for put the system into Maskrom mode to update the firmware When writing mismatched firmware or other conditions result in boot failure, use this test point

Except in this case, please use Recovery Key
Put the system into loader mode to update the firmware

RK3568_J(VCCIO3 Domain)

Default

SDMMC0&JTAG



Note:

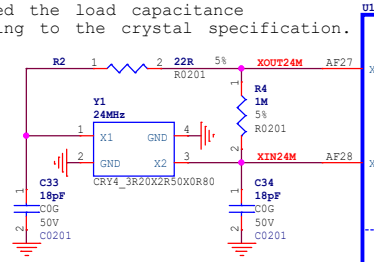
Caps of between dashed green lines and U1000 should be placed under the U1000 package

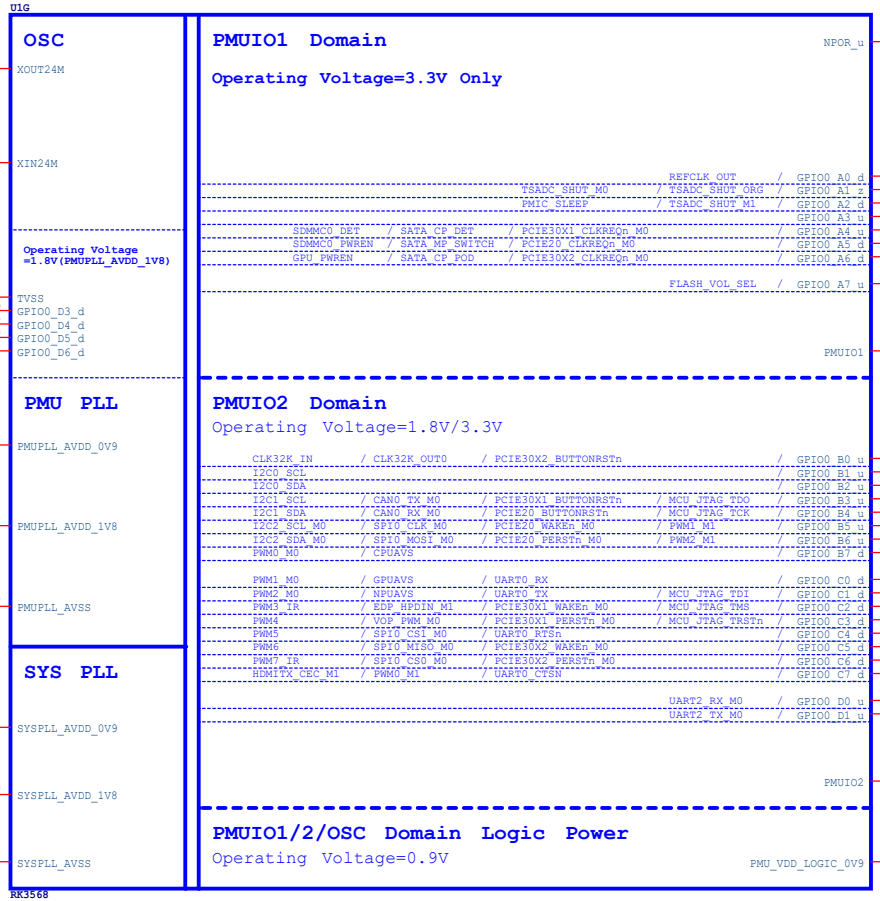
Size: A3	Title: Gong Le	REV: V1.3
	Page Name: RK3568_Flash/SD Controller	
Date: Friday, September 10, 2021	Sheet 08 of 33	

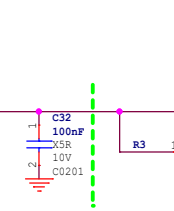
RK3568_G(OSC/PLL/PMUIO1/2)

Note:

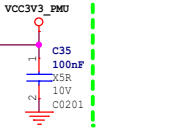
Adjusted the load capacitance according to the crystal specification.

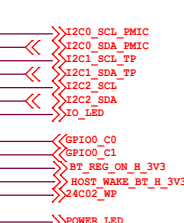


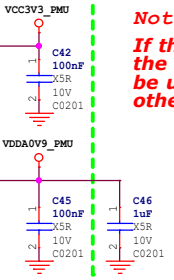


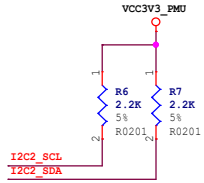


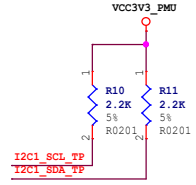
Default:24MHz





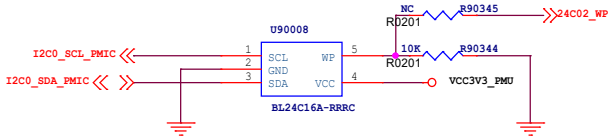






Note:

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

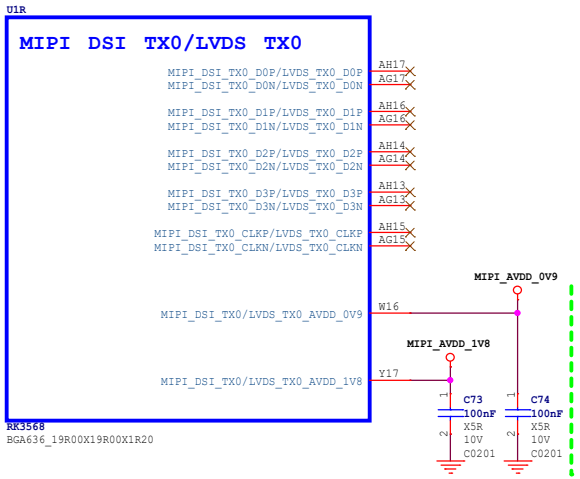


Note:

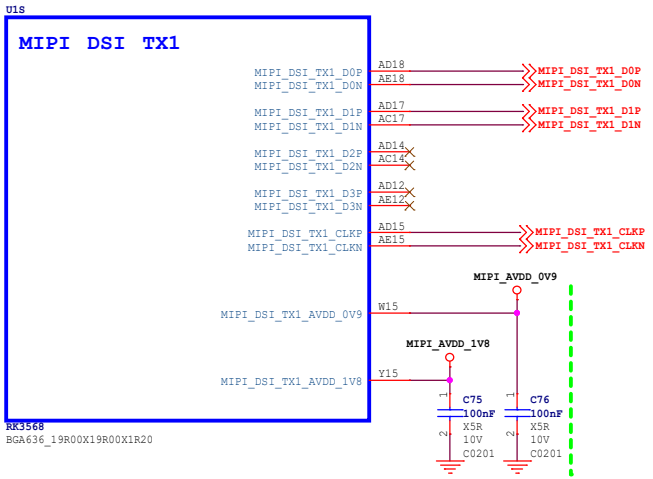
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Size	Title: Gong Le		REV
A3	Page Name: RK3568_OSC/PLL/PMUIO		V1.3
Date: Friday, September 10, 2021	Sheet 09 of 33		

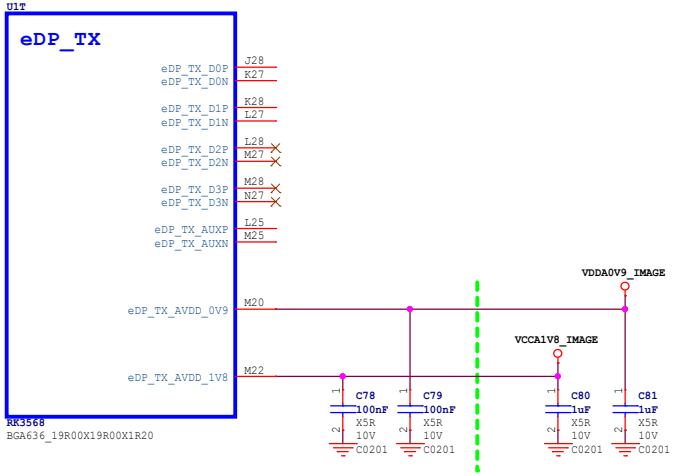
RK3568_R(MIPI_DSI_TX0/LVDS_TX0)



RK3568_S(MIPI_DSI_TX1)

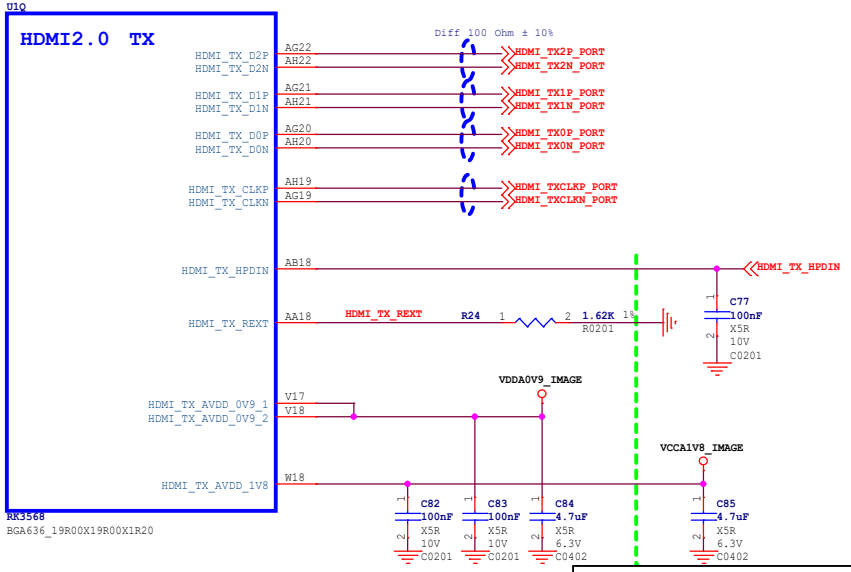


RK3568_T(eDP TX)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3568_Q(HDMI2.0 TX)



Size A3	Title: Gong Le	REV V1.3
	Page Name: RK3568_VO Interface_1	
Date: Friday, September 10, 2021	Sheet 10 of 33	

RK3568_L(VCCIO5 Domain)

U1L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC_D0	/ VOP_BT656_D0_M0	/ SPI0_MISO_M1	/ PCIE20_CLKREQn_M1	/ I2S1_MCLK_M2	/ GPIO2_D0_d
LCDC_D1	/ VOP_BT656_D1_M0	/ SPI0_MOSI_M1	/ PCIE20_WAKEn_M1	/ I2S1_SCLK_TX_M2	/ GPIO2_D1_d
LCDC_D2	/ VOP_BT656_D2_M0	/ SPI0_CS0_M1	/ PCIE30X1_CLKREQn_M1	/ I2S1_LRCK_TX_M2	/ GPIO2_D2_d
LCDC_D3	/ VOP_BT656_D3_M0	/ SPI0_CLK_M1	/ PCIE30X1_WAKEn_M1	/ I2S1_SDI0_M2	/ GPIO2_D3_d
LCDC_D4	/ VOP_BT656_D4_M0	/ SPI2_CS1_M1	/ PCIE30X2_CLKREQn_M1	/ I2S1_SDI1_M2	/ GPIO2_D4_d
LCDC_D5	/ VOP_BT656_D5_M0	/ SPI2_CS0_M1	/ PCIE30X2_WAKEn_M1	/ I2S1_SDI2_M2	/ GPIO2_D5_d
LCDC_D6	/ VOP_BT656_D6_M0	/ SPI2_MOSI_M1	/ PCIE30X2_PERSTn_M1	/ I2S1_SDI3_M2	/ GPIO2_D6_d
LCDC_D7	/ VOP_BT656_D7_M0	/ SPI2_MISO_M1	/ UART8_TX_M1	/ I2S1_SDO0_M2	/ GPIO2_D7_d
LCDC_CLK	/ VOP_BT656_CLK_M0	/ SPI2_CLK_M1	/ UART8_RX_M1	/ I2S1_SDO1_M2	/ GPIO3_A0_d
LCDC_D8	/ VOP_BT1120_D0	/ SPI1_CS0_M1	/ PCIE30X1_PERSTn_M1	/ SDMMC2_D0_M1	/ GPIO3_A1_d
LCDC_D9	/ VOP_BT1120_D1	/ GMAC1_TXD2_M0	/ I2S3_MCLK_M0	/ SDMMC2_D1_M1	/ GPIO3_A2_d
LCDC_D10	/ VOP_BT1120_D2	/ GMAC1_TXD3_M0	/ I2S3_SCLK_M0	/ SDMMC2_D2_M1	/ GPIO3_A3_d
LCDC_D11	/ VOP_BT1120_D3	/ GMAC1_RXD2_M0	/ I2S3_LRCK_M0	/ SDMMC2_D3_M1	/ GPIO3_A4_d
LCDC_D12	/ VOP_BT1120_D4	/ GMAC1_RXD3_M0	/ I2S3_SDO_M0	/ SDMMC2_CMD_M1	/ GPIO3_A5_d
LCDC_D13	/ VOP_BT1120_CLK	/ GMAC1_TXCLK_M0	/ I2S3_SDI_M0	/ SDMMC2_CLK_M1	/ GPIO3_A6_d
LCDC_D14	/ VOP_BT1120_D5	/ GMAC1_RXCLK_M0		/ SDMMC2_DET_M1	/ GPIO3_A7_d
LCDC_D15	/ VOP_BT1120_D6	/ ETH1_REFCLKO_25M_M0		/ SDMMC2_PWREN_M1	/ GPIO3_B0_d
LCDC_D16	/ VOP_BT1120_D7	/ GMAC1_RXD0_M0	/ UART4_RX_M1	/ PWM8_M0	/ GPIO3_B1_d
LCDC_D17	/ VOP_BT1120_D8	/ GMAC1_RXD1_M0	/ UART4_TX_M1	/ PWM9_M0	/ GPIO3_B2_d
LCDC_D18	/ VOP_BT1120_D9	/ GMAC1_RXDV_CRS_M0	/ I2C5_SCL_M0	/ PDM_SDI0_M2	/ GPIO3_B3_d
LCDC_D19	/ VOP_BT1120_D10	/ GMAC1_RXER_M0	/ I2C5_SDA_M0	/ PDM_SDI1_M2	/ GPIO3_B4_d
LCDC_D20	/ VOP_BT1120_D11	/ GMAC1_TXD0_M0	/ I2C3_SCL_M1	/ PWM10_M0	/ GPIO3_B5_d
LCDC_D21	/ VOP_BT1120_D12	/ GMAC1_TXD1_M0	/ I2C3_SDA_M1	/ PWM11_IR_M0	/ GPIO3_B6_d
LCDC_D22	/ PWM12_M0	/ GMAC1_TXEN_M0	/ UART3_TX_M1	/ PDM_SDI2_M2	/ GPIO3_B7_d
LCDC_D23	/ PWM13_M0	/ GMAC1_MCLKINOUT_M0	/ UART3_RX_M1	/ PDM_SDI3_M2	/ GPIO3_C0_d
LCDC_HSYNC	/ VOP_BT1120_D13	/ SPI1_MOSI_M1	/ PCIE20_PERSTn_M1	/ I2S1_SDO2_M2	/ GPIO3_C1_d
LCDC_VSYNC	/ VOP_BT1120_D14	/ SPI1_MISO_M1	/ UART5_TX_M1	/ I2S1_SDO3_M2	/ GPIO3_C2_d
LCDC_DEN	/ VOP_BT1120_D15	/ SPI1_CLK_M1	/ UART5_RX_M1	/ I2S1_SCLK_RX_M2	/ GPIO3_C3_d
PWM14_M0	/ VOP_PWM_M1	/ GMAC1_MDC_M0	/ UART7_TX_M1	/ PDM_CLK1_M2	/ GPIO3_C4_d
PWM15_IR_M0	/ SPDIF_TX_M1	/ GMAC1_MDIO_M0	/ UART7_RX_M1	/ I2S1_LRCK_RX_M2	/ GPIO3_C5_d

RK3568

BGA636_19R00X19R00X1R20

AG6 PCIE20_CLKREQn_M1
AD7 PCIE20_WAKEn_M1
AC8 HP_DET_L_GPIO2_D2
AC7
AF5 PCIE30X2_CLKREQn_M1
AF6 PCIE30X2_WAKEn_M1
AD6 PCIE30X2_PERSTn_M1
AH5 GPIO2_D7
AH4 GPIO3_A0
AB8
AE5 GPIO3_A2
AG4 GPIO3_A3
AF4 GPIO3_A4
AH3 GPIO3_A5
AG3 GPIO3_A6
AH2 GMAC1_INT/PMEB_GPIO3_A7
AG2 GMAC1_RSTn_GPIO3_B0
AG1 PWM_FAN
AF2 GPIO3_B2
AF1 I2C5_SCL_M0
AE1 I2C5_SDA_M0
AE2 I2C3_SCL_M1
AE3 I2C3_SDA_M1
AD4
AD2 LCD0_PWREN_H_GPIO3_C0
AD1 PCIE20_PERSTn_M1
AA7 GPIO3_C2
AC4 GPIO3_C3
AC3 GPIO3_C4
AC2 GPIO3_C5

V10 VCCIO5_1
V11 VCCIO5_2

VCC_3V3
C86 100nF X5R 10V C0201

VCC_3V3
R25 10K 5% R0201
od
GMAC1_INT/PMEB_GPIO3_A7

VCC_3V3
R26 2.2K 5% R0201
R27 2.2K 5% R0201
I2C5_SCL_M0
I2C5_SDA_M0

VCC_3V3
R28 2.2K 5% R0201
R29 2.2K 5% R0201
I2C3_SCL_M1
I2C3_SDA_M1

Note:

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

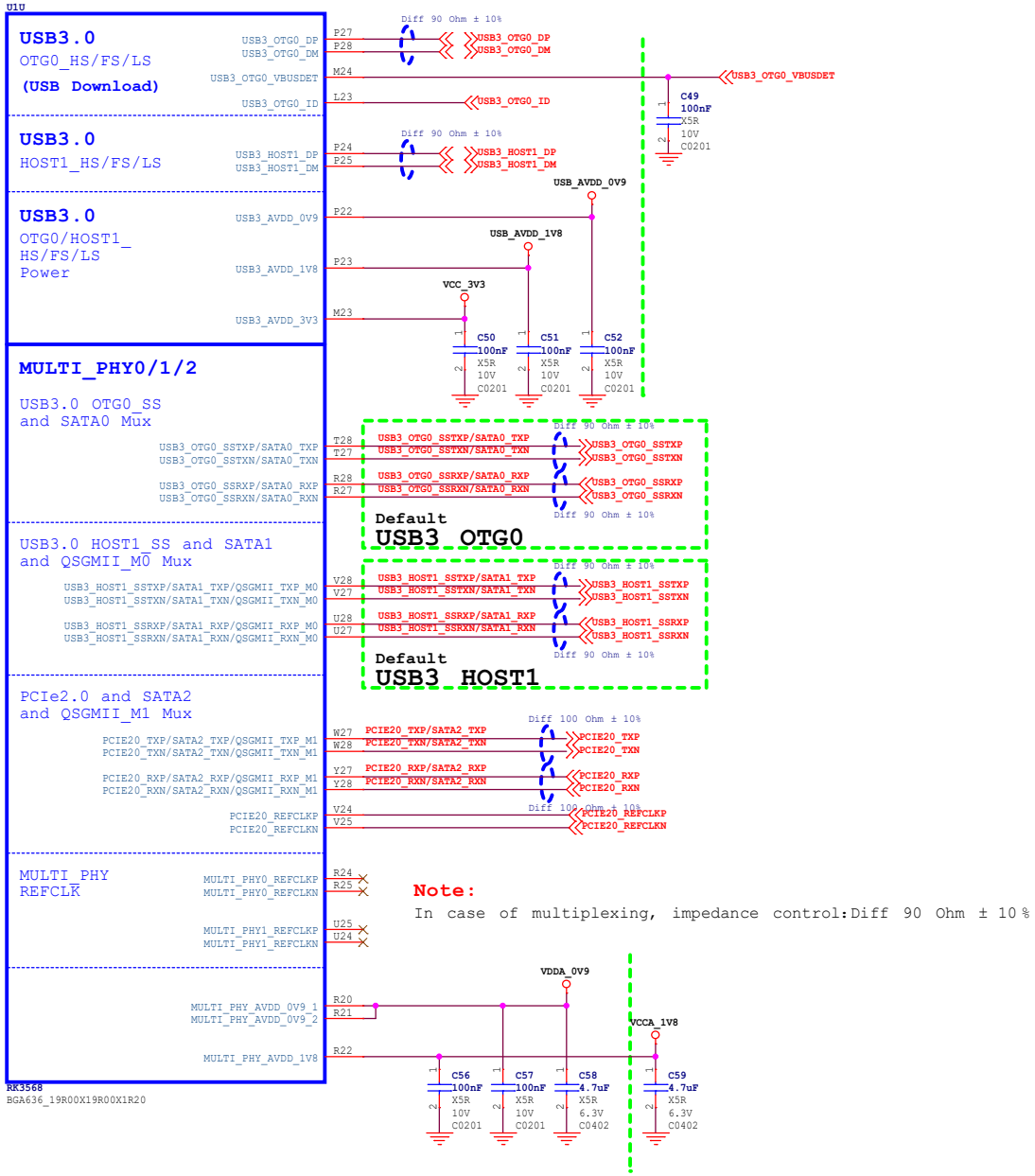
Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

radxa

Size	Title:	Gong Le	REV
A4	Page Name:	RK3568_VO Interface_2	V1.3
Date:	Friday, September 10, 2021	Sheet 11 of 33	

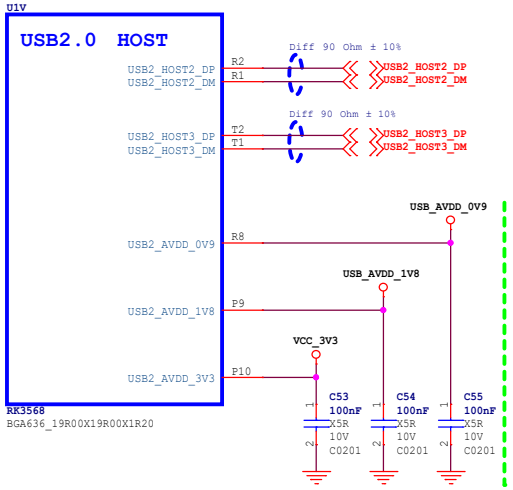
RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)



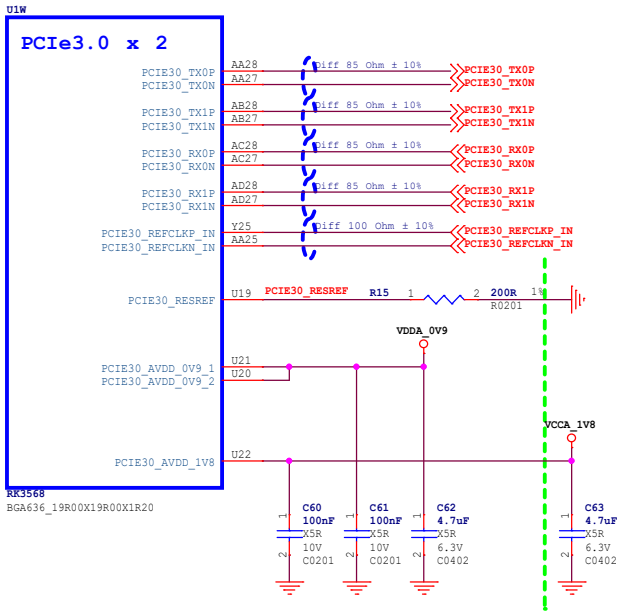
Note:
In case of multiplexing, impedance control:Diff 90 Ohm ± 10%

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3568_V(USB2.0 HOST)



RK3568_W(PCIe3.0 x2)



Size A3	Title: Gong Le		REV V1.3
	Page Name: RK3568_USB/PCIe/SATA PHY		
Date: Friday, September 10, 2021	Sheet 12 of 33		

RK3568_H(VCCIO1 Domain)

U1H

VCCIO1 Domain

Operating Voltage=1.8V/3.3V

I2C3_SDA_M0	/ UART3_RX_M0	/ CAN1_RX_M0		/ AUDIOPWM_LOUT_P	/ ACODEC_ADC_DATA	/	GPIO1_A0_u
I2C3_SCL_M0	/ UART3_TX_M0	/ CAN1_TX_M0		/ AUDIOPWM_LOUT_N	/ ACODEC_ADC_CLK	/	GPIO1_A1_u
I2S1_MCLK_M0	/ UART3_RTSn_M0	/ SCR_CLK	/ PCIE30X1_PERSTn_M2			/	GPIO1_A2_d
I2S1_SCLK_TX_M0	/ UART3_CTSn_M0	/ SCR_IO	/ PCIE30X1_WAKEn_M2		/ ACODEC_DAC_CLK	/	GPIO1_A3_d
I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0		/ SPDIF_TX_M0		/	GPIO1_A4_d
I2S1_LRCK_TX_M0	/ UART4_RTSn_M0	/ SCR_RST	/ PCIE30X1_CLKREQn_M2		/ ACODEC_DAC_SYNC	/	GPIO1_A5_d
I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0		/ AUDIOPWM_ROUT_P		/	GPIO1_A6_d
I2S1_SDO0_M0	/ UART4_CTSn_M0	/ SCR_DET		/ AUDIOPWM_ROUT_N	/ ACODEC_DAC_DATAL	/	GPIO1_A7_d
I2S1_SDO1_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0	/ PCIE20_CLKREQn_M2		/ ACODEC_DAC_DATAR	/	GPIO1_B0_d
I2S1_SDO2_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0	/ PCIE20_WAKEn_M2		/ ACODEC_ADC_SYNC	/	GPIO1_B1_d
I2S1_SDO3_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0	/ PCIE20_PERSTn_M2			/	GPIO1_B2_d
	I2S1_SDI0_M0	/ PDM_SDI0_M0				/	GPIO1_B3_d

VCCIO1

RK3568

BGA636_19R00X19R00X1R20

D18 — GPIO1_A0
E18 — GPIO1_A1
A19 — I2S1_MCLK_M0_RK809
B19 — I2S1_SCLK_TX_M0_RK809
F18
A20 — I2S1_LRCK_TX_M0_RK809
C20 — PDM_CLK0_M0_RK809
B20 — I2S1_SDO0_M0_RK809
D20
E20 — MIPI_CAM0_PDN_L_GPIO1_B1
A21
B21 — I2S1_SDI0_M0/PDM_SDI0_M0_RK809

VCCIO_ACODEC

H17

C87
100nF
X5R
10V
C0201

Default 3.3V

Note:

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

radxa

Size	Title:	Gong Le	REV
A4	Page Name:	RK3568_Audio Interface	V1.3
Date:	Friday, September 10, 2021	Sheet 13 of 33	

RK3568_K(VCCIO4 Domain)

U1K

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

SDMMC1_D0	/ GMAC0_RXD2	/ UART6_RX_M0	/	GPIO2_A3_u
SDMMC1_D1	/ GMAC0_RXD3	/ UART6_TX_M0	/	GPIO2_A4_u
SDMMC1_D2	/ GMAC0_RXCLK	/ UART7_RX_M0	/	GPIO2_A5_u
SDMMC1_D3	/ GMAC0_TXD2	/ UART7_TX_M0	/	GPIO2_A6_u
SDMMC1_CMD	/ GMAC0_TXD3	/ UART9_RX_M0	/	GPIO2_A7_u
SDMMC1_CLK	/ GMAC0_TXCLK	/ UART9_TX_M0	/	GPIO2_B0_d
SDMMC1_PWREN	/ I2C4_SDA_M1	/ UART8_RTSn_M0 / CAN2_RX_M1	/	GPIO2_B1_d
SDMMC1_DET	/ I2C4_SCL_M1	/ UART8_CTSn_M0 / CAN2_TX_M1	/	GPIO2_B2_u
	GMAC0_TXD0	/ UART1_RX_M0	/	GPIO2_B3_u
	GMAC0_TXD1	/ UART1_TX_M0	/	GPIO2_B4_u
	GMAC0_TXEN	/ UART1_RTSn_M0 / SPI1_CLK_M0	/	GPIO2_B5_u
	GMAC0_RXD0	/ UART1_CTSn_M0 / SPI1_MISO_M0	/	GPIO2_B6_u
I2S2_SCLK_RX_M0	/ GMAC0_RXD1	/ UART6_RTSn_M0 / SPI1_MOSI_M0	/	GPIO2_B7_d
I2S2_LRCK_RX_M0	/ GMAC0_RXDV_CRS	/ UART6_CTSn_M0 / SPI1_CS0_M0	/	GPIO2_C0_d
I2S2_MCLK_M0	/ ETH0_REFCLKO_25M	/ UART7_RTSn_M0 / SPI2_CLK_M0	/	GPIO2_C1_d
I2S2_SCLK_TX_M0	/ GMAC0_MCLKINOUT	/ UART7_CTSn_M0 / SPI2_MISO_M0	/	GPIO2_C2_d
I2S2_LRCK_TX_M0	/ GMAC0_MDC	/ UART9_RTSn_M0 / SPI2_MOSI_M0	/	GPIO2_C3_d
I2S2_SDO_M0	/ GMAC0_MDIO	/ UART9_CTSn_M0 / SPI2_CS0_M0	/	GPIO2_C4_d
I2S2_SDI_M0	/ GMAC0_RXER	/ UART8_TX_M0 / SPI2_CS1_M0	/	GPIO2_C5_d
CLK32K_OUT1		/ UART8_RX_M0 / SPI1_CS1_M0	/	GPIO2_C6_d

E27, E28, B28, C27, C28, D27, D26, E25, F28, G27, G28, F27, H25, F24, G23, F25, H24, H23, F26, E26, J21 — VCCIO4

D27 — WIFI_LED

D26 — I2C4_SDA_M1

E25 — I2C4_SCL_M1

F28 — UART1_RX_M0

G27 — UART1_TX_M0

G28 — UART1_RTS_M0

F27 — UART1_CTS_M0

F25 — SOC_PCM_CLK

H24 — SOC_PCM_SYNC

H23 — SOC_PCM_OUT

F26 — SOC_PCM_IN

VCC_1V8

C64 100nF X5R 10V C0201

RK3568
BGA636_19R00X19R00X1R20

RGMII0

Note:

If Ethernet PHY uses other models, please note whether the default pull-up and pull-down of GPIO affect Ethernet PHY function

At present, TXEN will be affected if it defaults to high level need to add a 4.7K resistance to ground

Note:

According to the actual choice of mounted Cannot be mounted at the same time
Default:1.8V
Select the voltage according to the application

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

RK3568_N(VCCIO7 Domain)

Note:

When use HDMI, HDMITX_SCL/SDA cannot be shared with other devices

U1N

VCCIO7 Domain

Operating Voltage=1.8V/3.3V

PWM14_M1	/ SPI3_CLK_M1	/ CAN1_RX_M1 / PCIE30X2_CLKREQn_M2	/ I2S3_MCLK_M1	/ GPIO4_C2_d
PWM15_IR_M1	/ SPI3_MOSI_M1	/ CAN1_TX_M1 / PCIE30X2_WAKEn_M2	/ I2S3_SCLK_M1	/ GPIO4_C3_d
EDP_HPDIN_M0	/ SPDIF_TX_M2	/ SATA2_ACT_LED / PCIE30X2_PERSTn_M2	/ I2S3_LRCK_M1	/ GPIO4_C4_d
PWM12_M1	/ SPI3_MISO_M1	/ SATA1_ACT_LED / UART9_TX_M1	/ I2S3_SDO_M1	/ GPIO4_C5_d
PWM13_M1	/ SPI3_CS0_M1	/ SATA0_ACT_LED / UART9_RX_M1	/ I2S3_SDI_M1	/ GPIO4_C6_d
HDMITX_SCL	/ I2C5_SCL_M1			/ GPIO4_C7_u
HDMITX_SDA	/ I2C5_SDA_M1			/ GPIO4_D0_u
HDMITX_CEC_M0	/ SPI3_CS1_M1			/ GPIO4_D1_u
				GPIO4_D2_d

AF8, AA11, AH7, AD8, AE8, AG8, AG7, AH6, AB9, V12 — VCCIO7

AF8 — GPIO4_C2

AA11 — GPIO4_C3

AD8 — GPIO4_C5

AE8 — GPIO4_C6

AG8 — HDMITX_SCL

AG7 — HDMITX_SDA

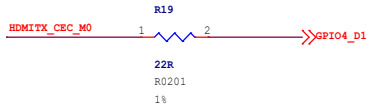
AH6 — HDMITX_CEC_M0

AB9 — CAMERAB_PDN_L_GPIO4_D2 [26]

VCC_3V3

C66 100nF X5R 10V C0201

RK3568
BGA636_19R00X19R00X1R20



Note:

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

RK3568_O(SARADC/OTP)

U1O

SARADC

Recovery/ SARADC_VIN0	B27	SARADC_VIN0_KEY/RECOVERY
SARADC_VIN1	C26	SARADC_VIN1
SARADC_VIN2	D24	SARADC_VIN2_HP_HOOK
SARADC_VIN3	E23	SARADC_VIN3
SARADC_VIN4	G21	ADC_IN4 [26]
SARADC_VIN5	F22	SARADC_VIN5
SARADC_VIN6	G20	
SARADC_VIN7	F21	
SARADC_AVDD_1V8	H22	

C65 1 2 1nF X5R 50V C0201

VCCA_1V8

C67 100nF X5R 10V C0201

OTP

OTP_VCC18 — H20

VCC_1V8

C68 100nF X5R 10V C0201

RK3568
BGA636_19R00X19R00X1R20

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

Note:

Must be mounted

VCCA_1V8

R18 10K 1% R0201

SARADC_VIN0_KEY/RECOVERY

TP5 TP_0.7

TP6 TP_0.7

Note:

If there is no Key requirement, two test points must be reserved to facilitate firmware update

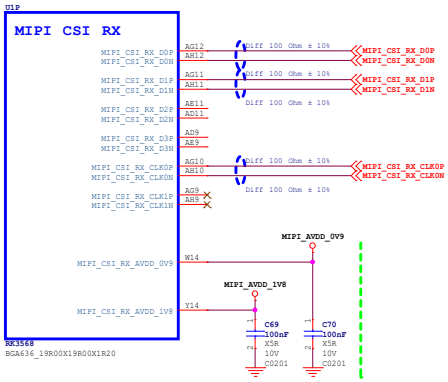
It is suggested to reserve a Key to facilitate the development debug

If SARADC_VIN0=0V at after power on and reset, then system will enter into loader mode.

SARADC_VIN0_KEY/RECOVERY

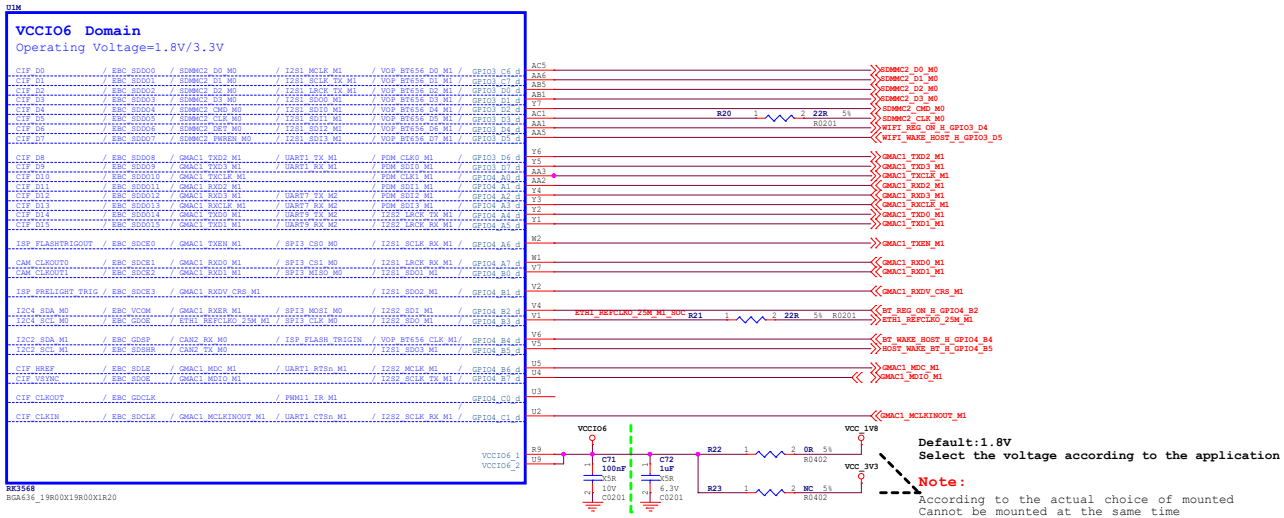
Size	Title:	Gong Le	REV
A3	Page Name:	RK3568_SARADC/GPIO	V1.3
Date:	Friday, September 10, 2021	Sheet 14 of 33	

RK3568_P(MIPI_CSI_RX)



Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0
		MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

RK3568_M(VCCIO6 Domain)



Default:1.8V
Select the voltage according to the application

Note:
According to the actual choice of mounted
Cannot be mounted at the same time

Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

BT1120 16bit Mode:
Default: D0-D7 <--> Y0-Y7 , D8-D15 <--> C0-C7
Swap ON: D0-D7 <--> C0-C7 , D8-D15 <--> Y0-Y7

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Note:
If the power domain voltage is adjusted,
the software configuration must
be updated synchronously,
other wise the IO may be damaged!

Note:
Camera MCLK can select the following clock:
1:CAM_CLKOUT0
2:CAM_CLKOUT1
3:CIF_CLKOUT
4:REFCLK_OUT

Attention to the voltage matching

GMAC	Direction	GEPHY	GMAC	Direction	FEPHY
GMACx_TXD0	------->	PHYx_TXD0	GMACx_TXD0	------->	PHYx_TXD0
GMACx_TXD1	------->	PHYx_TXD1	GMACx_TXD1	------->	PHYx_TXD1
GMACx_TXD2	------->	PHYx_TXD2			
GMACx_TXD3	------->	PHYx_TXD3			
GMACx_TXEN	------->	PHYx_TXEN	GMACx_TXEN	------->	PHYx_TXEN
GMACx_TXCLK	------->	PHYx_TXCLK			
GMACx_RXD0	<-------	PHYx_RXD0	GMACx_RXD0	<-------	PHYx_RXD0
GMACx_RXD1	<-------	PHYx_RXD1	GMACx_RXD1	<-------	PHYx_RXD1
GMACx_RXD2	<-------	PHYx_RXD2			
GMACx_RXD3	<-------	PHYx_RXD3			
GMACx_RXDV	<-------	PHYx_RXDV	GMACx_RXDV	<-------	PHYx_RXDV
GMACx_RXCLK	<-------	PHYx_RXCLK			
GMACx_RXER			GMACx_RXER	<-------	PHYx_RXER
GMACx_MDC	------->	PHYx_MDC	GMACx_MDC	------->	PHYx_MDC
GMACx_MDIO	<------->	PHYx_MDIO	GMACx_MDIO	<------->	PHYx_MDIO
ETHx_REFCLKO_25M	------->	PHYx_XTALIN PHYx_CLKOUT125(Option)			
GMACx_MCLKINOUT	<-------		GMACx_MCLKINOUT	------->	PHYx_XTALIN/REFCLK
GPIO	------->	PHYx_RSTn	GPIO	------->	PHYx_RSTn
GPIO	<-------	PHYx_INT/PMEB	GPIO	<-------	PHYx_INT/PMEB

radxa

Size	Title:	Gong Le	REV
A2	Page Name:	RK3568_VI Interface	V1.3
Date:	Friday, September 10, 2021	Sheet 15 of 33	

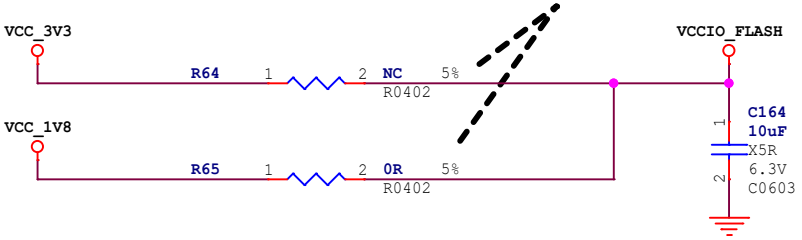
FLASH_VOL_SEL

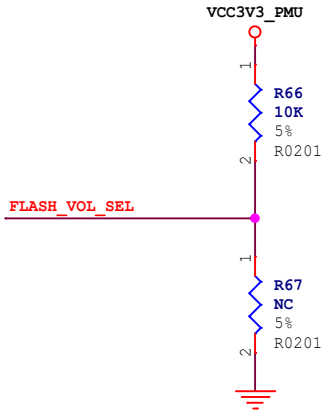
Flash Power Manage

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Optional 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 1.8V, Optional 3.3V	FLASH_VOL_SEL --> Logic=H(Default)

Note:

According to the actual choice of mounted
Cannot be mounted at the same time

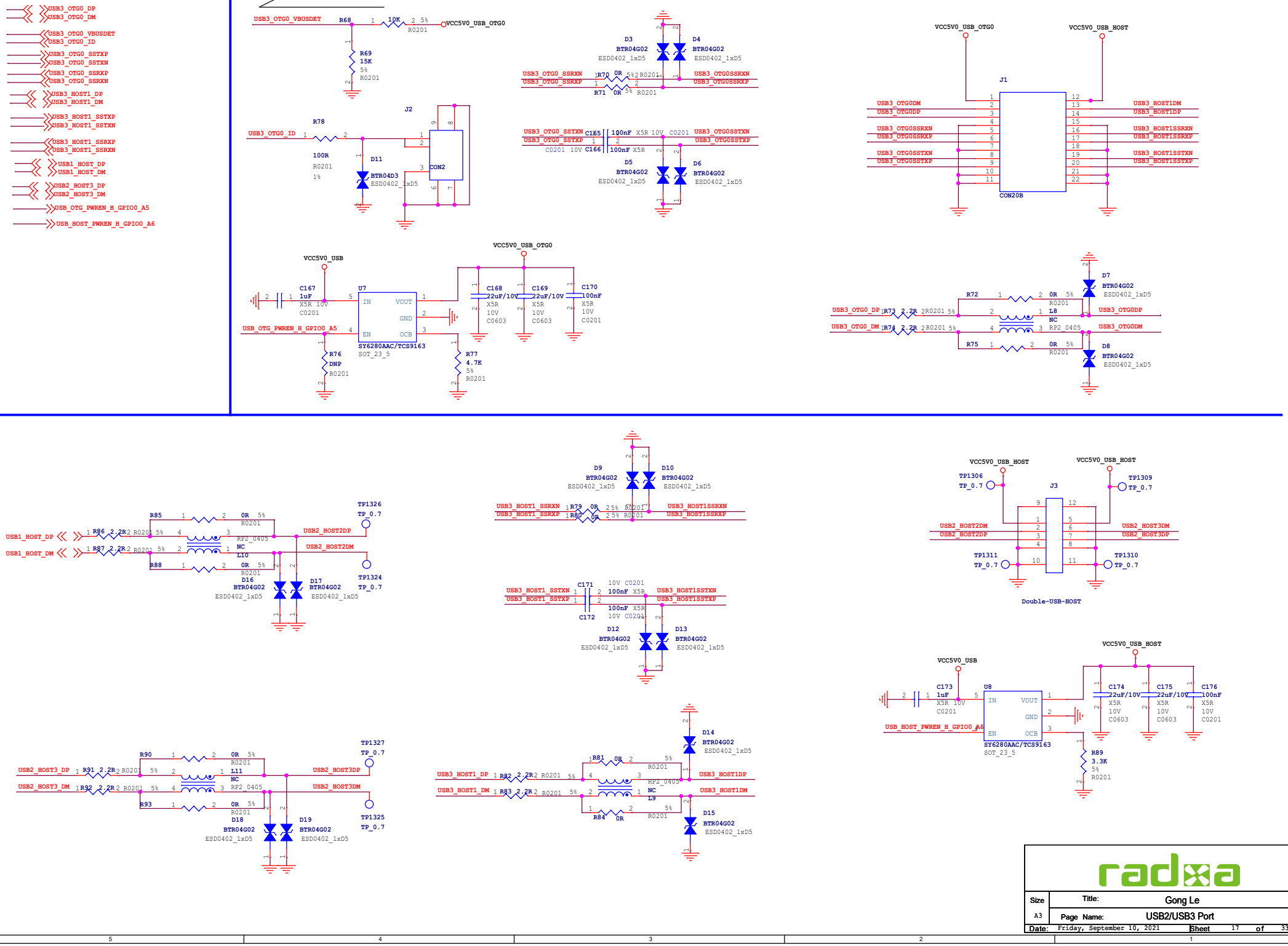




Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L:3.3V IO driven
Logic=H:1.8V IO driven

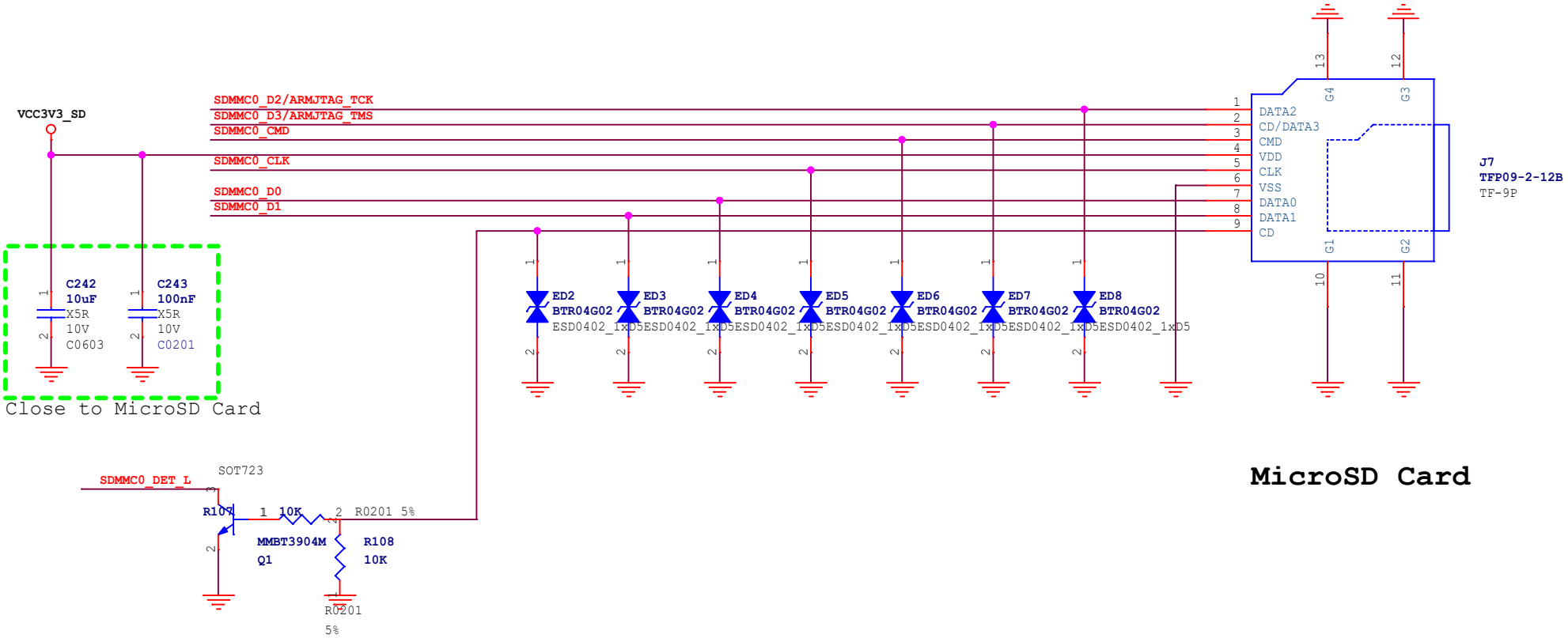
radxa

Size	Title:	Gong Le	REV
A4	Page Name:	Flash Power Manage	V1.3
Date:	Friday, September 10, 2021	Sheet 16 of 33	


USB3_OTG0_DP
USB3_OTG0_DM
USB3_OTG0_VBUSDET
USB3_OTG0_ID
USB3_OTG0_SSTXP
USB3_OTG0_SSTXN
USB3_OTG0_SSRXP
USB3_OTG0_SSRXN
USB3_HOST1_DP
USB3_HOST1_DM
USB3_HOST1_SSTXP
USB3_HOST1_SSTXN
USB3_HOST1_SSRXP
USB3_HOST1_SSRXN
USB1_HOST_DP
USB1_HOST_DM
USB2_HOST3_DP
USB2_HOST3_DM
USB_OTG_PWREN_H_GPIO0_A5
USB_HOST_PWREN_H_GPIO0_A6
USB3_OTG0_VBUSDET
R68
10K
R0201
VCC5V0_USB_OTG0
R69
15K
R78
USB3_OTG0_ID
100R
D11
BTR04D3
ESD0402_1xD5
J2
CON2
D3
D4
BTR04G02
R70
R71
0R
C165
C166
100nF
C0201
D5
D6
VCC5V0_USB_OTG0
VCC5V0_USB_HOST
J1
CON20B
USB3_OTG0DM
USB3_OTG0DP
USB3_OTG0SSRXN
USB3_OTG0SSRXP
USB3_OTG0SSTXN
USB3_OTG0SSTXP
USB3_HOST1DM
USB3_HOST1DP
USB3_HOST1SSRXN
USB3_HOST1SSRXP
USB3_HOST1SSTXN
USB3_HOST1SSTXP
VCC5V0_USB
C167
1uF
C0201
U7
SY6280AAC/TCS9163
SOT_23_5
IN
VOUT
GND
EN
OCB
C168
22uF/10V
C0603
C169
C170
R76
DNP
R77
4.7K
D7
D8
R72
R73
R74
R75
2.2R
NC
RP2_0405
L8
D9
D10
R79
R80
TP1326
TP1324
TP_0.7
USB1_HOST_DP
USB1_HOST_DM
USB2_HOST2DP
USB2_HOST2DM
R85
R86
R87
R88
L10
D16
D17
TP1306
TP1309
TP1311
TP1310
J3
Double-USB-HOST
USB2_HOST2DM
USB2_HOST2DP
USB2_HOST3DM
USB2_HOST3DP
C171
C172
D12
D13
R89
3.3K
C173
C174
C175
C176
R90
R91
R92
R93
L11
D18
D19
TP1327
TP1325
USB2_HOST3DP
USB2_HOST3DM
D14
D15
R81
R82
R83
R84
L9
USB3_HOST1DP
USB3_HOST1DM
radxa
Size
A3
Title:
Gong Le
REV
V1.3
Page Name:
USB2/USB3 Port
Date:
Friday, September 10, 2021
Sheet
17
of
33

MicroSD Card

SDMMC0_D0
SDMMC0_D1
SDMMC0_D2/ARMJTAG_TCK
SDMMC0_D3/ARMJTAG_TMS
SDMMC0_CMD
SDMMC0_CLK
SDMMC0_DET_L



MicroSD Card

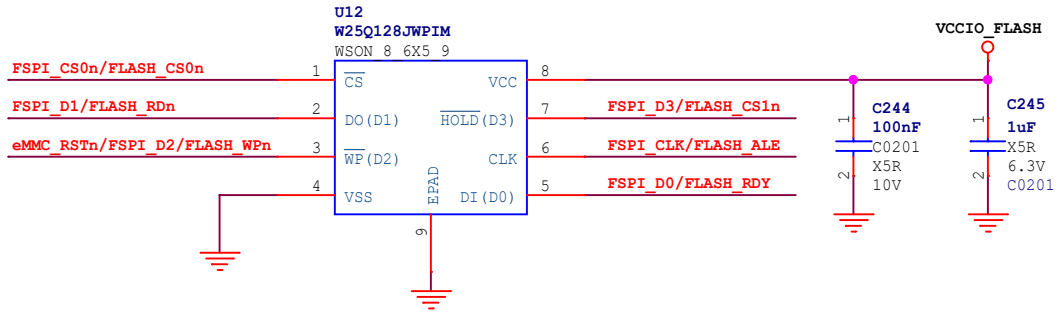
Size: A4	Title: Gong Le	REV: V1.3
	Page Name: MicroSD Card	
Date: Friday, September 10, 2021	Sheet 18 of 33	

SPI Flash

FSPI_CLK/FLASH_ALE

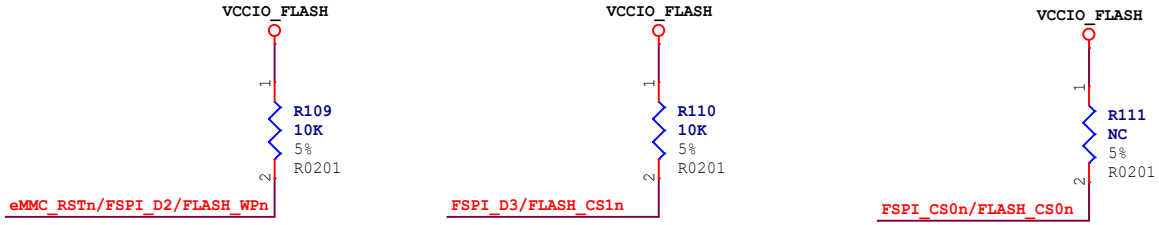
FSPI_D0/FLASH_RDY
FSPI_D1/FLASH_RDn
eMMC_RSTn/FSPI_D2/FLASH_WPn
FSPI_D3/FLASH_CS1n

FSPI_CS0n/FLASH_CS0n



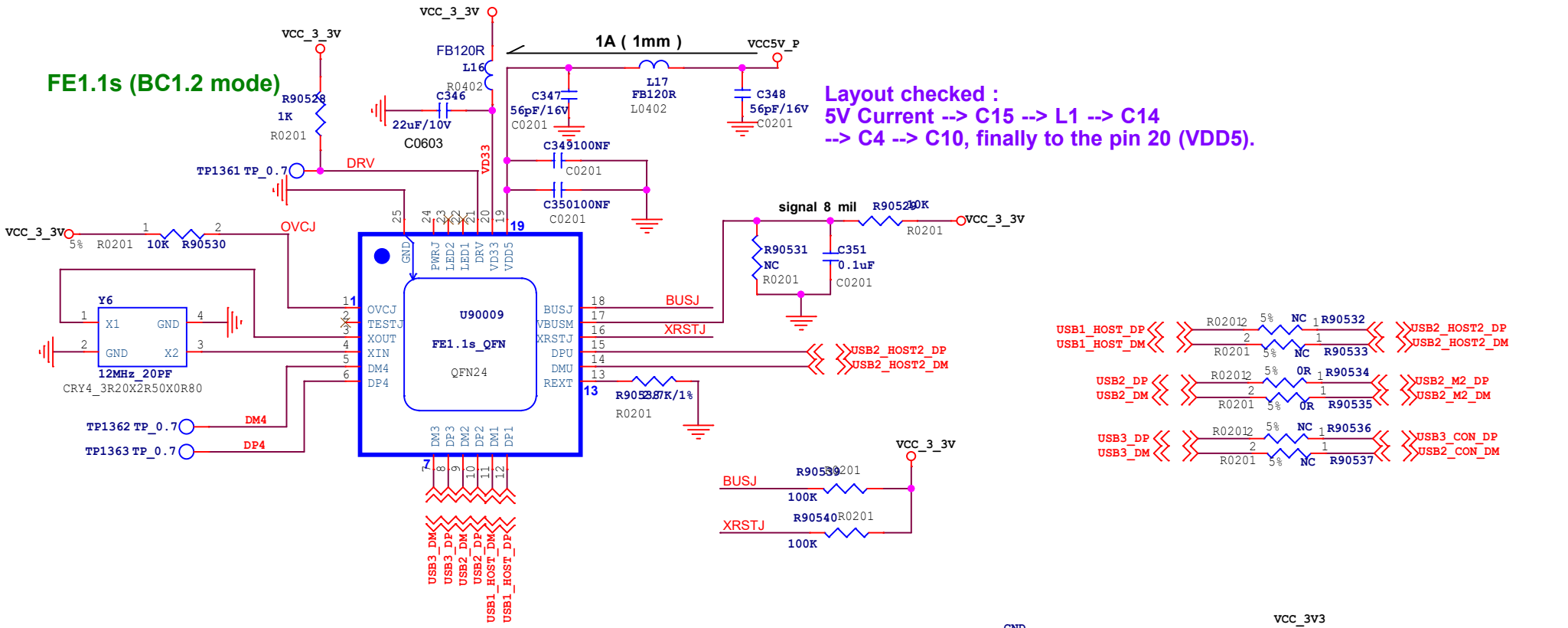
Note:
Default: 1.8V

Support:
1bit SPI NOR or SPI NAND
4bit SPI NOR or SPI NAND

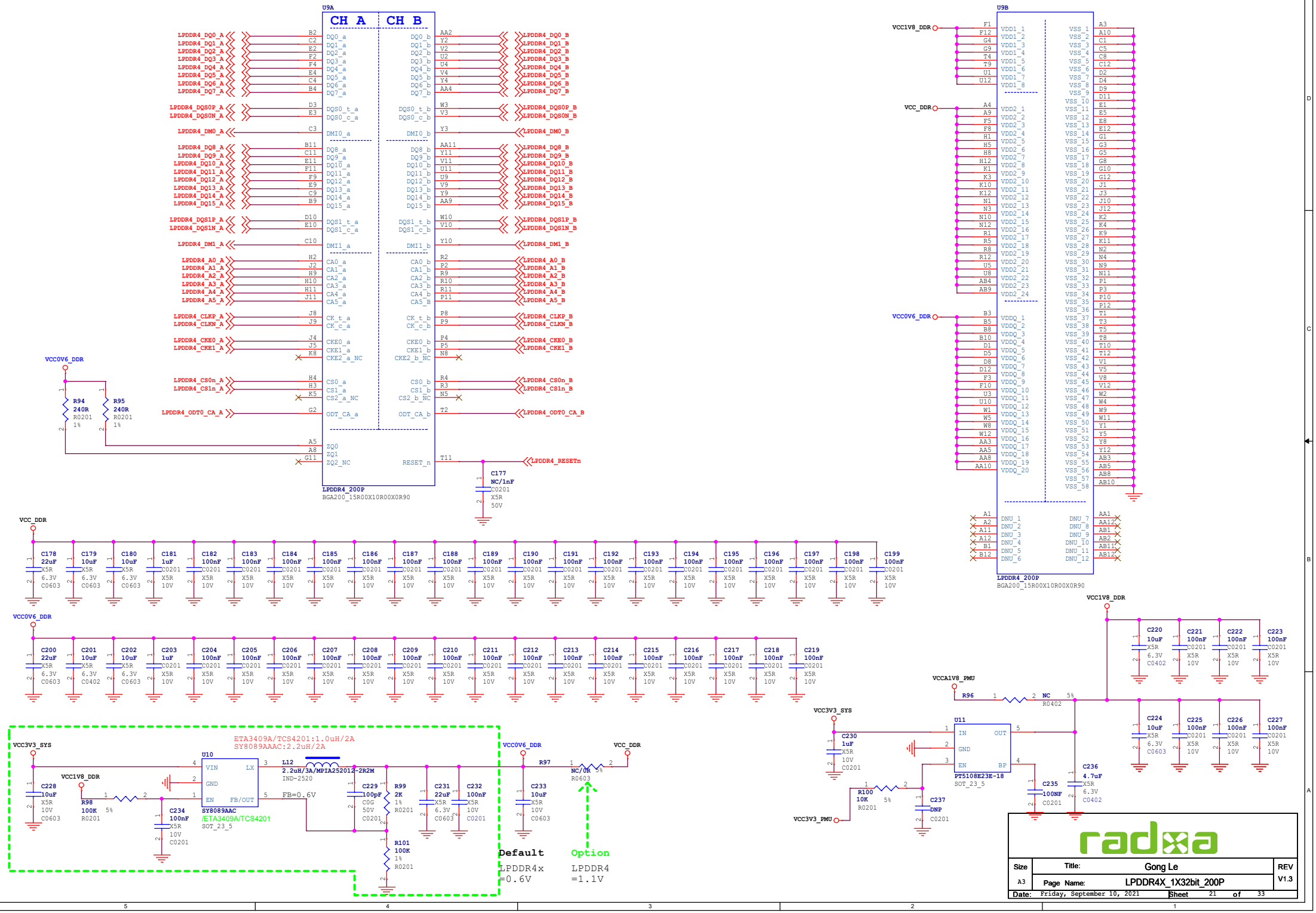


Note:
If Flash is compatible, please notice
when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted,@SPI Flash is not mounted
when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted,@SPI Flash is not mounted
when SPI Flash is used, the option is that SPI Flash is mounted, @eMMC is not mounted,@Nand is not mounted

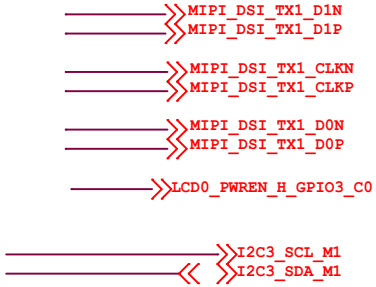
Size	Title:	Gong Le	REV
A4	Page Name:	SPI FLASH(Option)	V1.3
Date:	Friday, September 10, 2021	Sheet 19 of 33	

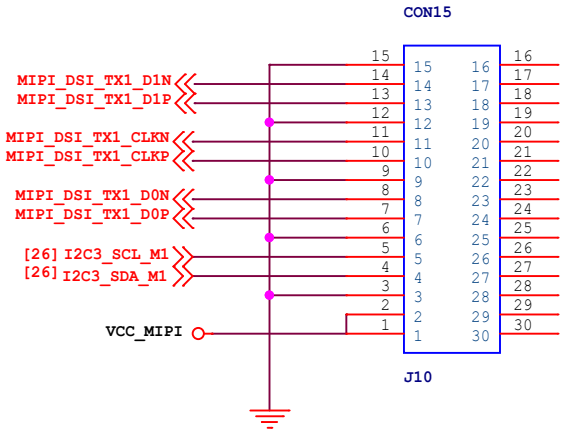


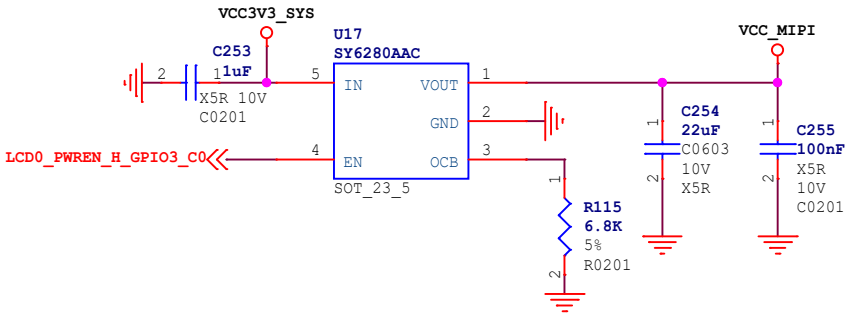
Size	Title:	Gong Le	REV
A4	Page Name:	USB HUB_FAN	V1.3
Date:	Friday, September 10, 2021	Sheet 20 of 33	


U9A
CH A
CH B
LPDDR4_200P
BGA200_15R00X10R00X0R90
U9B
LPDDR4_200P
BGA200_15R00X10R00X0R90
VCC1V8_DDR
VCC_DDR
VCC0V6_DDR
R94 240R R0201 1%
R95 240R R0201 1%
C177 NC/1nF C0201 X5R 50V
LPDDR4_RESETn
VCC_DDR
VCC0V6_DDR
VCC1V8_DDR
VCCA1V8_PMU
VCC3V3_SYS
VCC3V3_PMU
U10
SY8089AAC
/ETA3409A/TCS4201
SOT_23_5
ETA3409A/TCS4201:1.0uH/2A
SY8089AAC:2.2uH/2A
L12
2.2uH/3A/MPIA252012-2R2M
IND-2520
FB=0.6V
R97 NC/0R R0603
U11
PTS108E23E-18
SOT_23_5
Default
LPDDR4x
=0.6V
Option
LPDDR4
=1.1V
radxa
Size A3
Title: Gong Le
Page Name: LPDDR4X_1X32bit_200P
REV V1.3
Date: Friday, September 10, 2021
Sheet 21 of 33

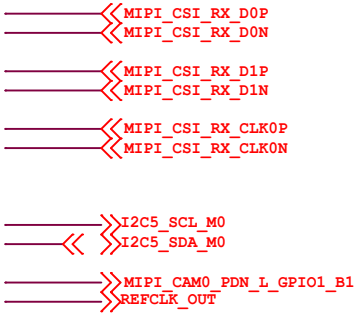
MIPI_DSI_TX 2Lanes

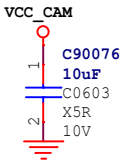


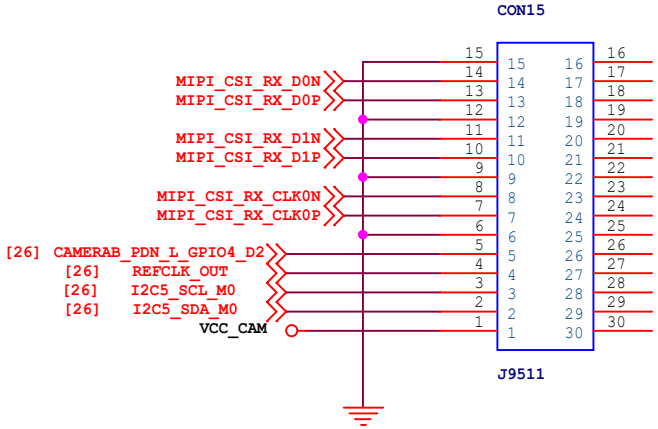


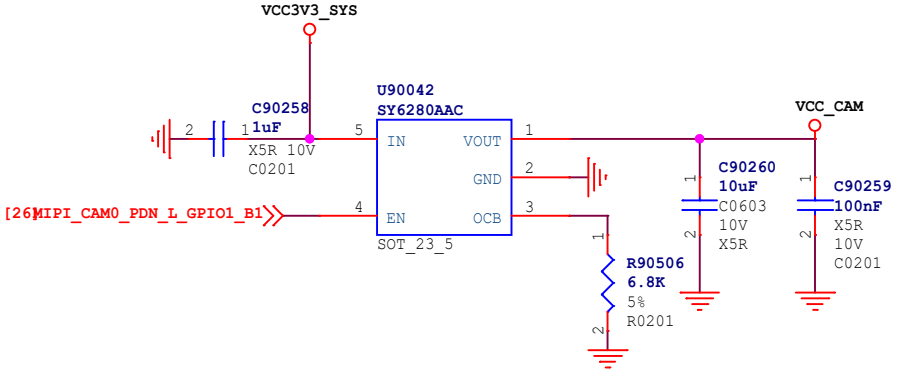


MIPI_CSI_RX 2Lanes



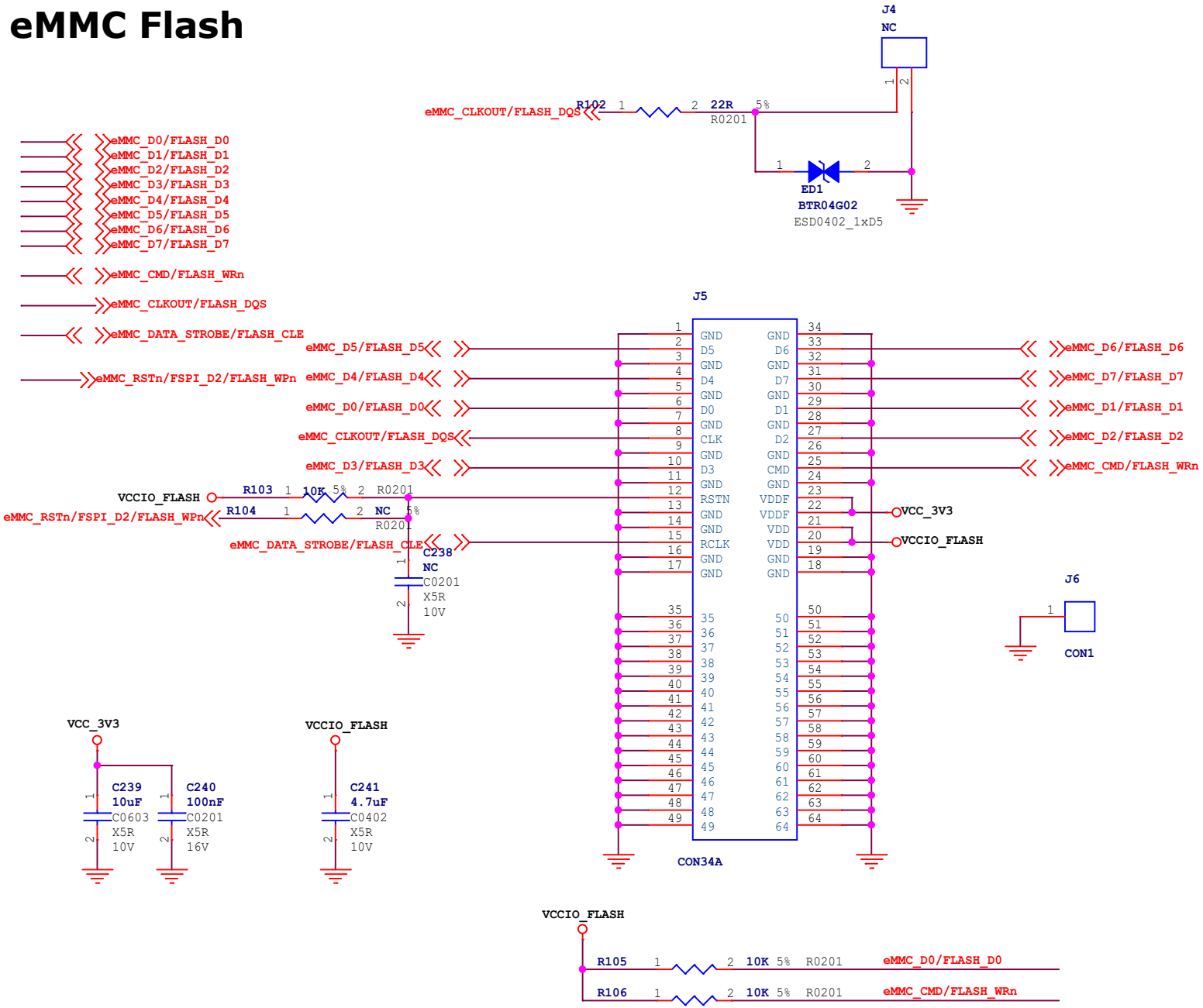




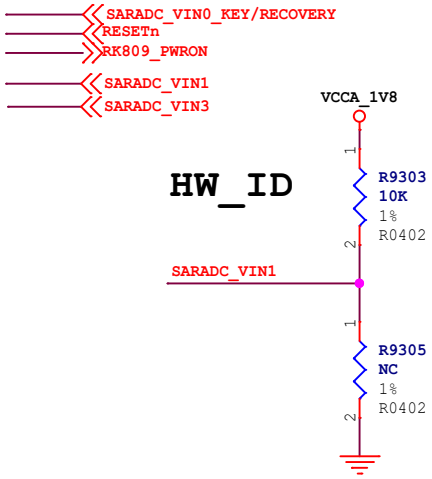


Size A4	Title: Gong Le		REV V1.3
	Page Name: MIPI_DSI_CSI		
Date: Friday, September 10, 2021		Sheet 22 of 33	

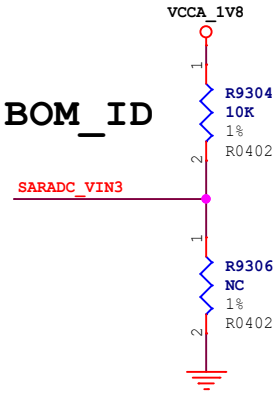
eMMC Flash



Size A4	Title: Gong Le	REV V1.3
	Page Name: eMMC Flash	
Date: Friday, September 10, 2021	Sheet 23 of 33	

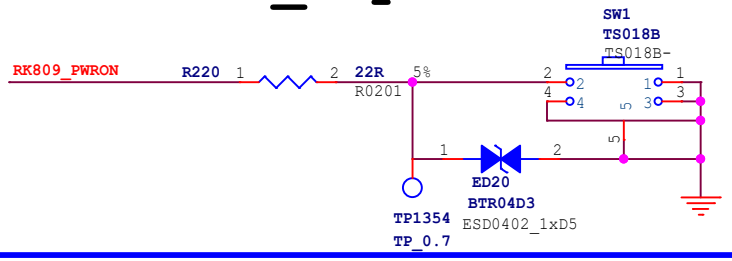


SARADC_VIN1	Up Resistance	Down Resistance
HW_ID0	10K	DNP
HW_ID1	10K	110K
HW_ID2	20K	100K
HW_ID3	33K	100K
HW_ID4	18K	36K
HW_ID5	36K	51K
HW_ID6	51K	51K
HW_ID7	51K	36K
HW_ID8	36K	18K
HW_ID9	100K	33K
HW_ID10	100K	20K
HW_ID11	110K	10K
HW_ID12	DNP	10K

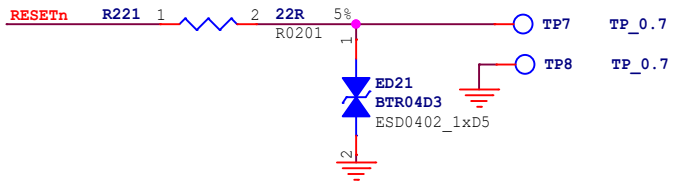


SARADC_VIN3	Up Resistance	Down Resistance
BOM_ID0	10K	DNP
BOM_ID1	10K	110K
BOM_ID2	20K	100K
BOM_ID3	33K	100K
BOM_ID4	18K	36K
BOM_ID5	36K	51K
BOM_ID6	51K	51K
BOM_ID7	51K	36K
BOM_ID8	36K	18K
BOM_ID9	100K	33K
BOM_ID10	100K	20K
BOM_ID11	110K	10K
BOM_ID12	DNP	10K

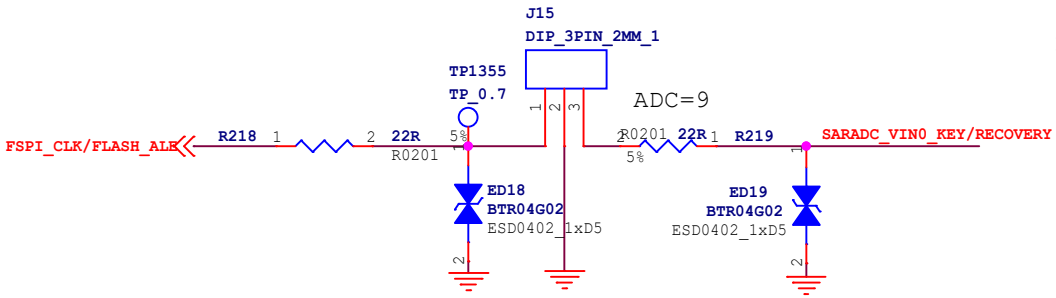
PowerOn/OFF_Key



Reset_Key



RECOVERY



Note:

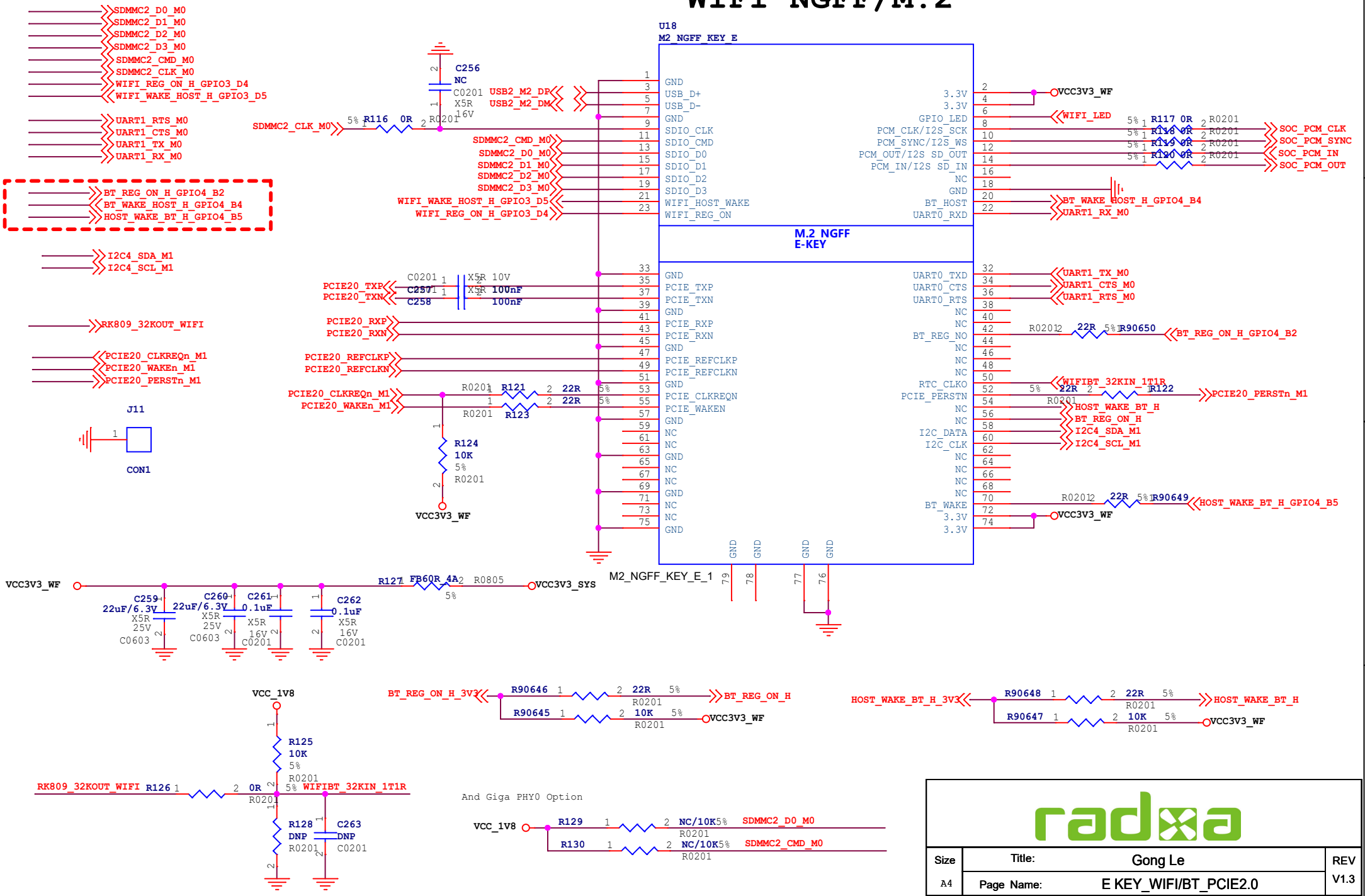
If there is no Key requirement,
It is suggested to reserve a
SW9200 Key to facilitate the
development debug

RECOVERY_Key function:
If SARADC_VIN0=0V
at after power on and reset,
then system will
enter into loader mode.

Size	Title:	Gong Le	REV
A4	Page Name:	SARADC_KEY	V1.3
Date:	Friday, September 10, 2021	Sheet 24 of 33	

SDIO WIFI/BT MODULE

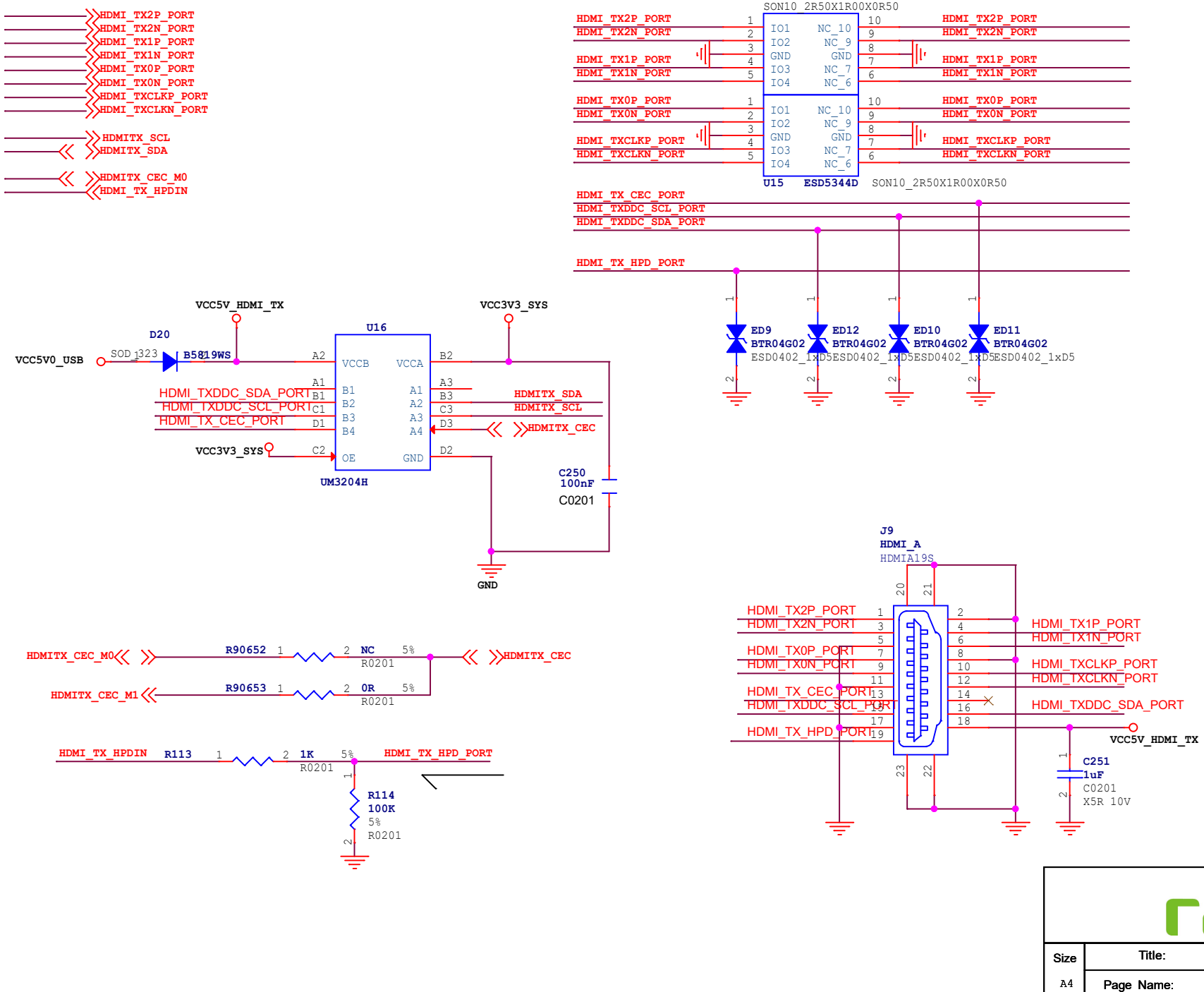
WIFI NGFF/M.2



Size	Title:	Gong Le	REV
A4	Page Name:	E KEY_WIFI/BT_PCIE2.0	V1.3
Date:	Friday, September 10, 2021	Sheet 25 of 33	

HDMI2.0 TX

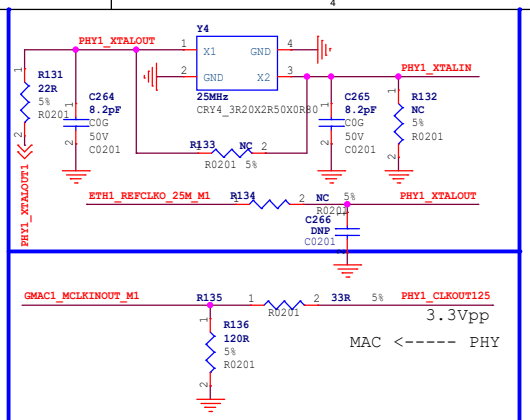
Cj<=0.4pF

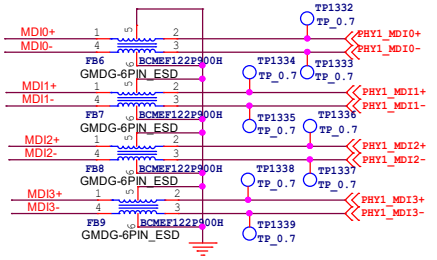


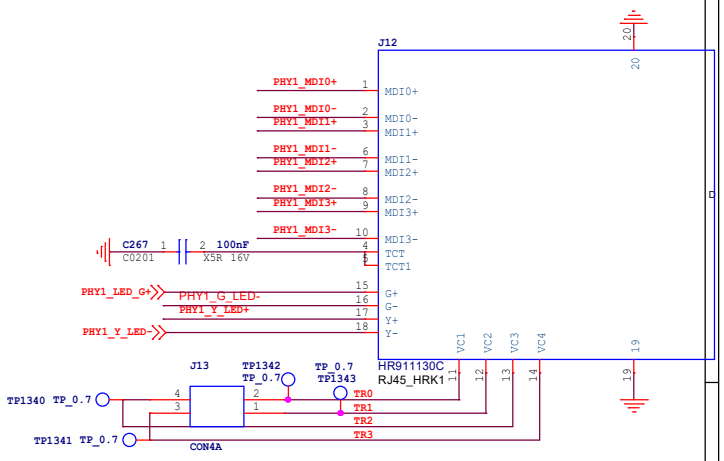
Size	Title:	Gong Le	REV
A4	Page Name:	HDMI	V1.3
Date:	Friday, September 10, 2021	Sheet 26 of 33	

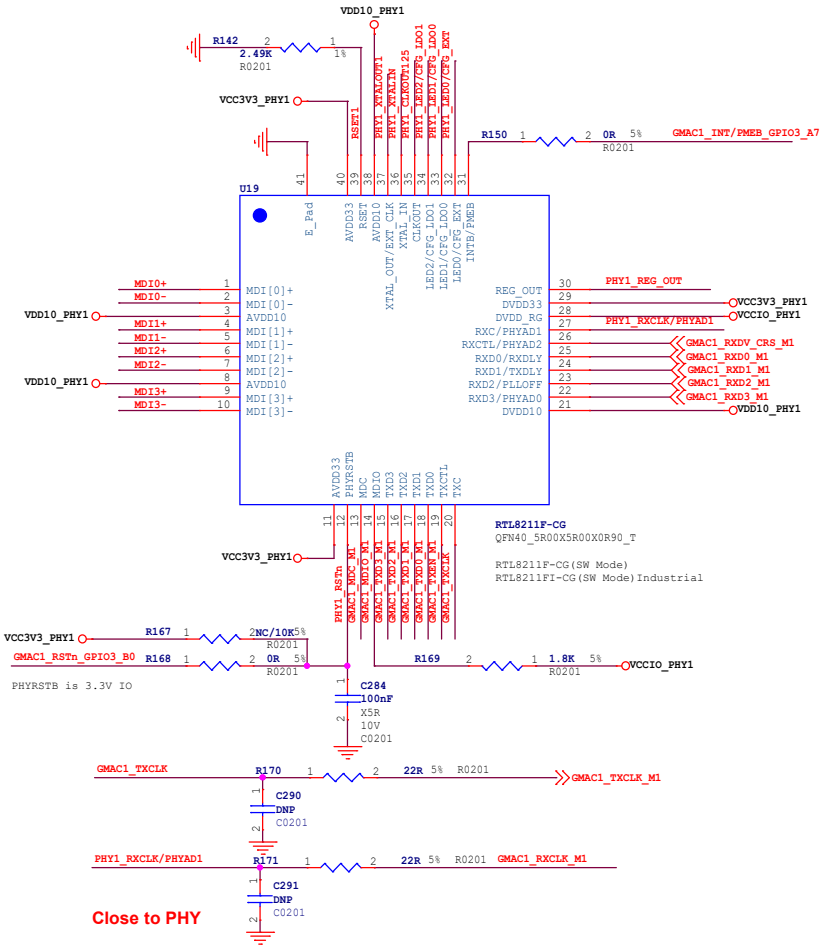
Giga PHY1

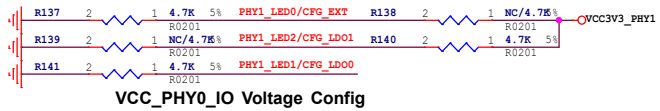
GMAC1_TXD0_M1
GMAC1_TXD1_M1
GMAC1_TXD2_M1
GMAC1_TXD3_M1
GMAC1_TXEN_M1
GMAC1_TXCLK_M1
GMAC1_RXD0_M1
GMAC1_RXD1_M1
GMAC1_RXD2_M1
GMAC1_RXD3_M1
GMAC1_RXDV_CRS_M1
GMAC1_RXCLK_M1
ETH1_REFCLKO_25M_M1
GMAC1_MCLKINOUT_M1
GMAC1_MDC_M1
GMAC1_MDIO_M1
GMAC1_RSTn_GPIO3_B0
GMAC1_INT/PMEB_GPIO3_A7



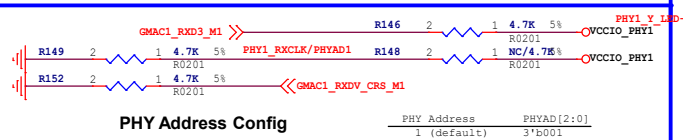






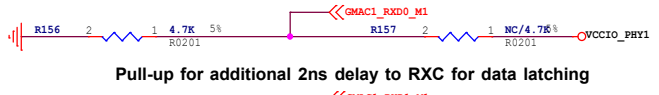


VCC_PHY0_IO Voltage Config

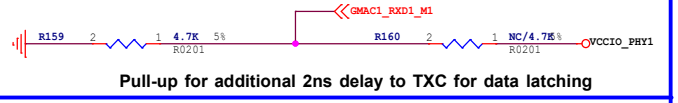


PHY Address Config

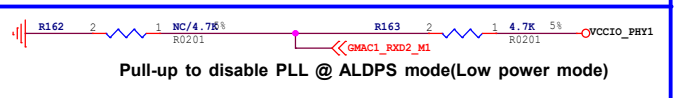
PHY Address	PHYAD[2:0]
1 (default)	3'b001



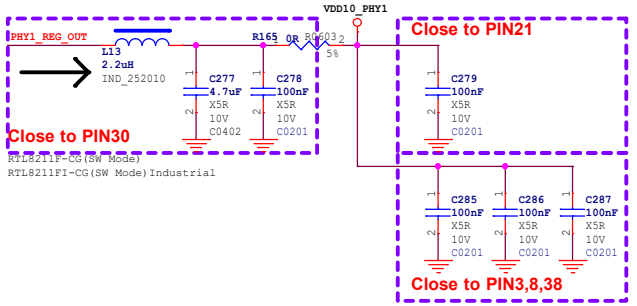
Pull-up for additional 2ns delay to RXC for data latching



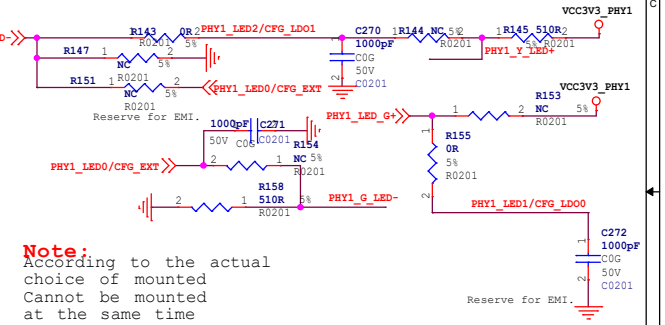
Pull-up for additional 2ns delay to TXC for data latching



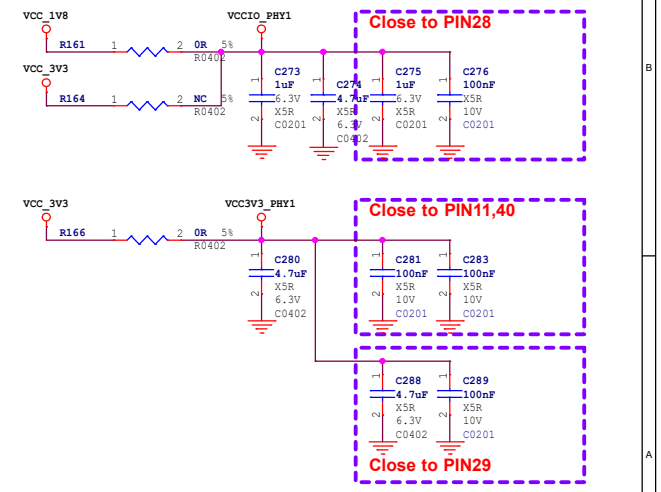
Pull-up to disable PLL @ ALDPS mode(Low power mode)



RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V	1'b1	2'b00	
External 1.8V	1'b1	2'b10	
Internal 1.8V(default)	1'b0	2'b10	



Note:
According to the actual choice of mounted Cannot be mounted at the same time



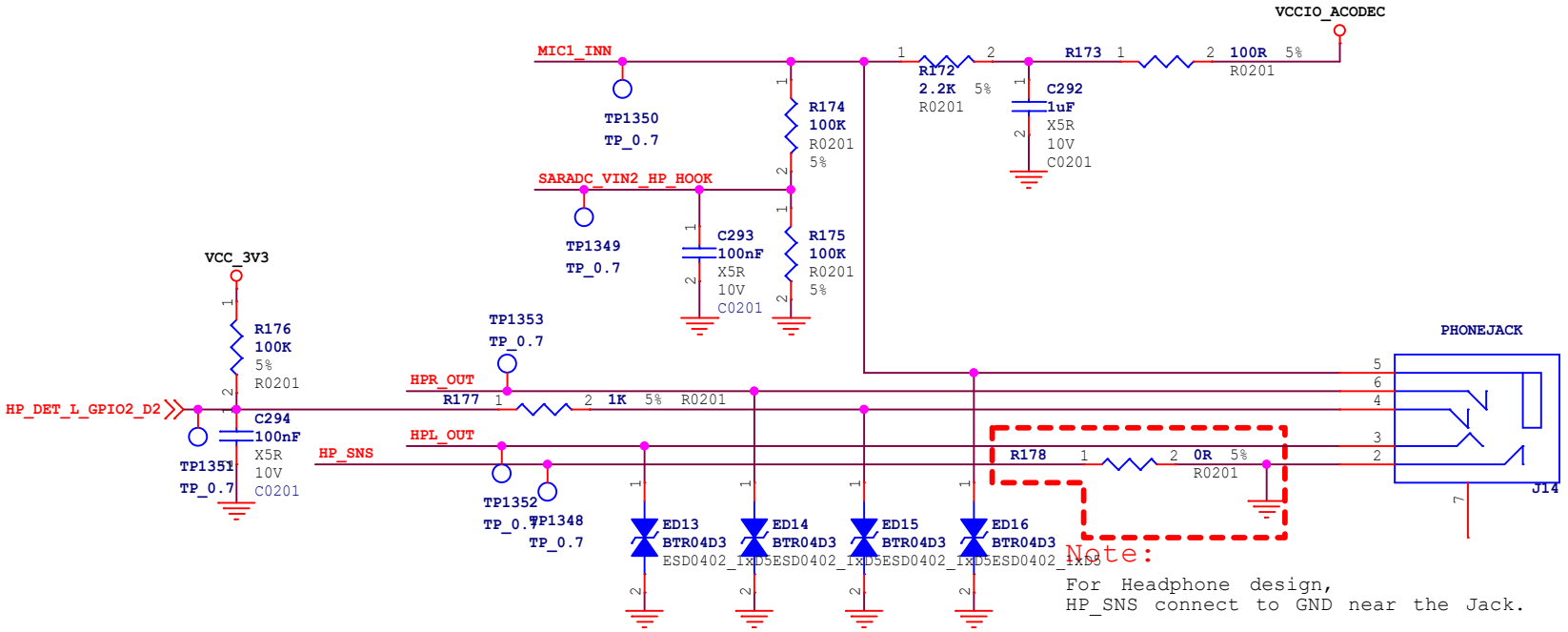
radxa

Size	Title:	Gong Le	REV
A3	Page Name:	Ethernet	V1.3
Date:	Friday, September 10, 2021	Sheet 27 of 33	

HPL_OUT
HP_SNS
HPR_OUT
HP_DET_L_GPIO2_D2
MIC1_INN
SARADC_VIN2_HP_HOOK

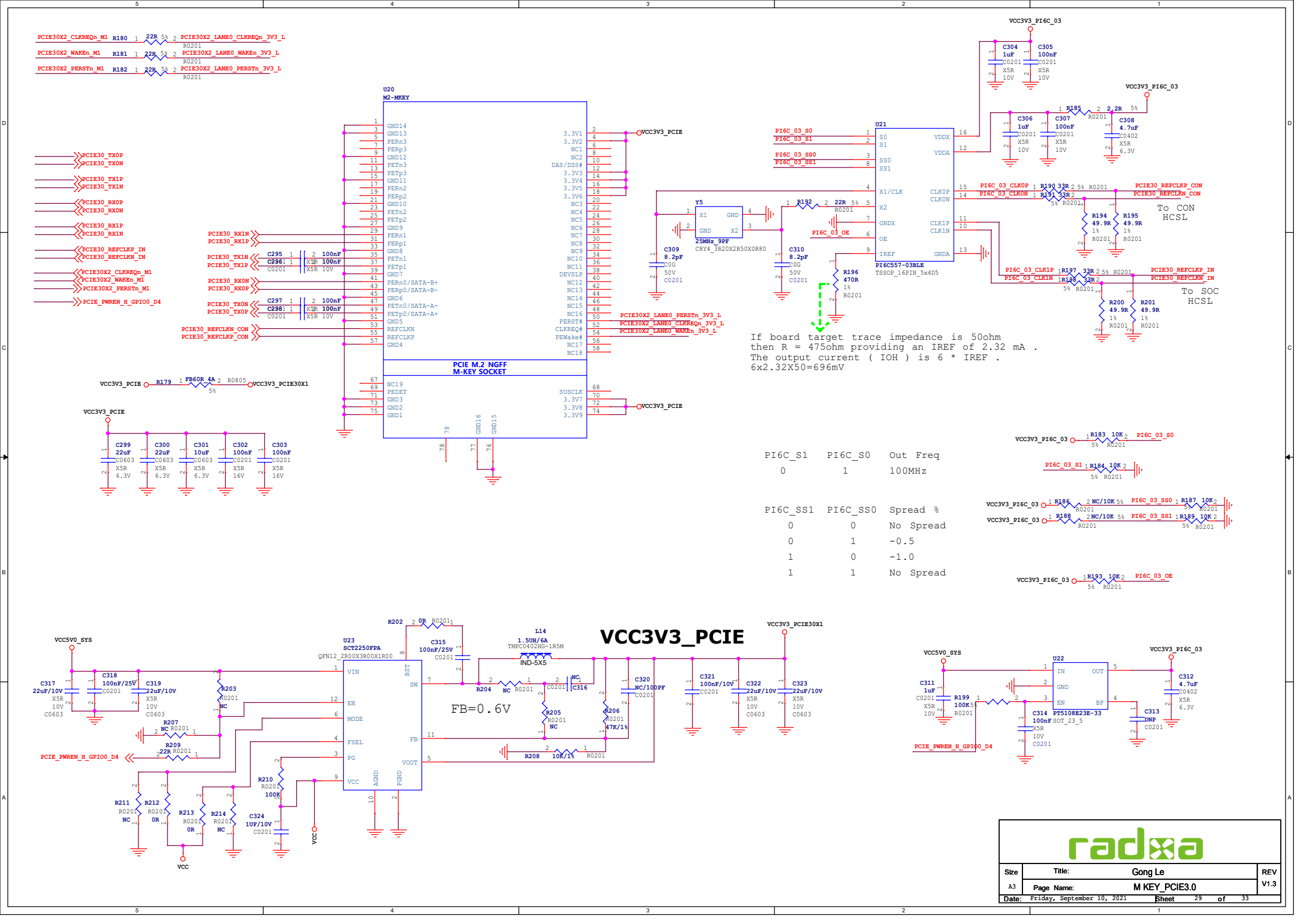
Headphone Jack(4-pole with DET & MIC)

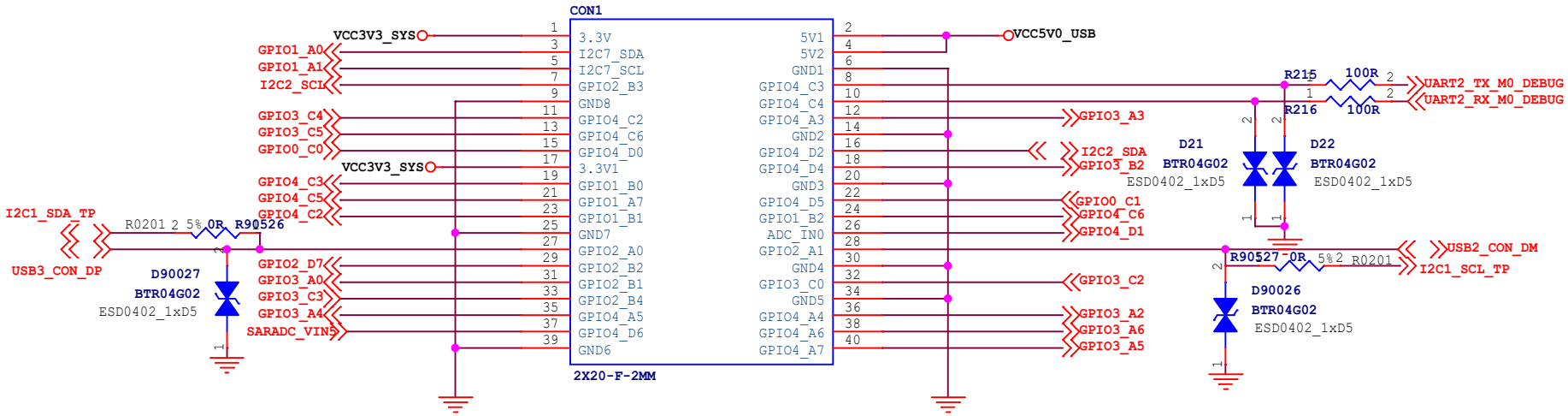
Option



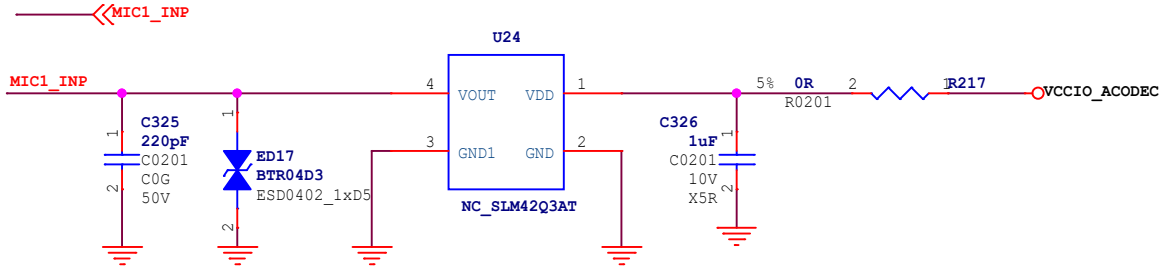
Note:
For Headphone design,
HP_SNS connect to GND near the Jack.

Size: A4	Title: Gong Le	REV: V1.3
	Page Name: Headphone	
Date: Friday, September 10, 2021	Sheet 28 of 33	


PCIE30X2_CLKREQn_M1
PCIE30X2_WAKEn_M1
PCIE30X2_PERSTn_M1
PCIE30X2_LANE0_CLKREQn_3V3_L
PCIE30X2_LANE0_WAKEn_3V3_L
PCIE30X2_LANE0_PERSTn_3V3_L
PCIE30_TX0P
PCIE30_TX0N
PCIE30_TX1P
PCIE30_TX1N
PCIE30_RX0P
PCIE30_RX0N
PCIE30_RX1P
PCIE30_RX1N
PCIE30_REFCLKP_IN
PCIE30_REFCLKN_IN
PCIE30_REFCLKP_CON
PCIE30_REFCLKN_CON
PCIE_PWREN_H_GPIO0_D4
U20
M2-MKEY
PCIE M.2 NGFF
M-KEY SOCKET
VCC3V3_PCIE
VCC3V3_PCIE30X1
U21
PI6C557-03BLE
TSSOP_16PIN_5x4D5
PI6C_03_S0
PI6C_03_S1
PI6C_03_SS0
PI6C_03_SS1
PI6C_03_OE
PI6C_03_CLK0P
PI6C_03_CLK0N
PI6C_03_CLK1P
PI6C_03_CLK1N
Y5
25MHz_9PF
CRY4_3R20X2R50X0R80
To CON
HCSL
To SOC
HCSL
If board target trace impedance is 50ohm
then R = 475ohm providing an IREF of 2.32 mA .
The output current (IOH) is 6 * IREF .
6x2.32X50=696mV
PI6C_S1 PI6C_S0 Out Freq
0 1 100MHz
PI6C_SS1 PI6C_SS0 Spread %
0 0 No Spread
0 1 -0.5
1 0 -1.0
1 1 No Spread
VCC5V0_SYS
U23
SCT2250FPA
QFN12_2R00X3R00X1R00
L14
1.5UH/6A
TMPC0402HG-1R5M
IND-5X5
FB=0.6V
VCC3V3_PCIE
U22
PT5108E23E-33
SOT_23_5
Size A3
Title: Gong Le
Page Name: M KEY_PCIE3.0
REV V1.3
Date: Friday, September 10, 2021
Sheet 29 of 33



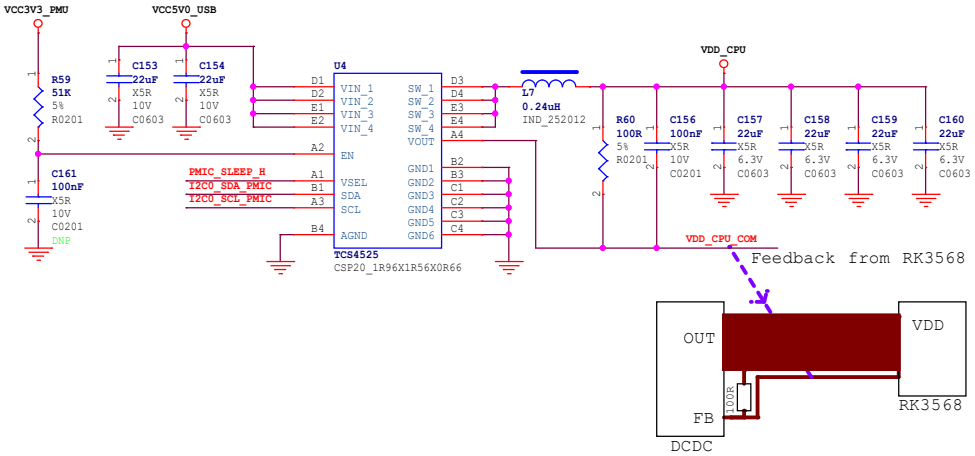
MIC



Size	Title:	Gong Le	REV
A4	Page Name:	CONNECT	V1.3
Date:	Friday, September 10, 2021	Sheet 30 of 33	

I2C0_SCL_PMIC
I2C0_SDA_PMIC
PMIC_SLEEP_H
VDD_CPU_COM
RTCIC_INT_L_GPIO0_D3
RTCIC_32KOUT
I2C5_SCL_M0
I2C5_SDA_M0
RK809_PWRON

VDD_CPU

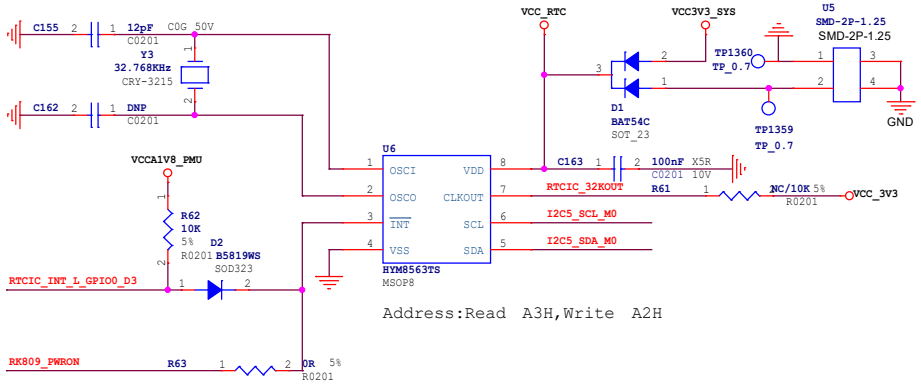


RTC IC --Option

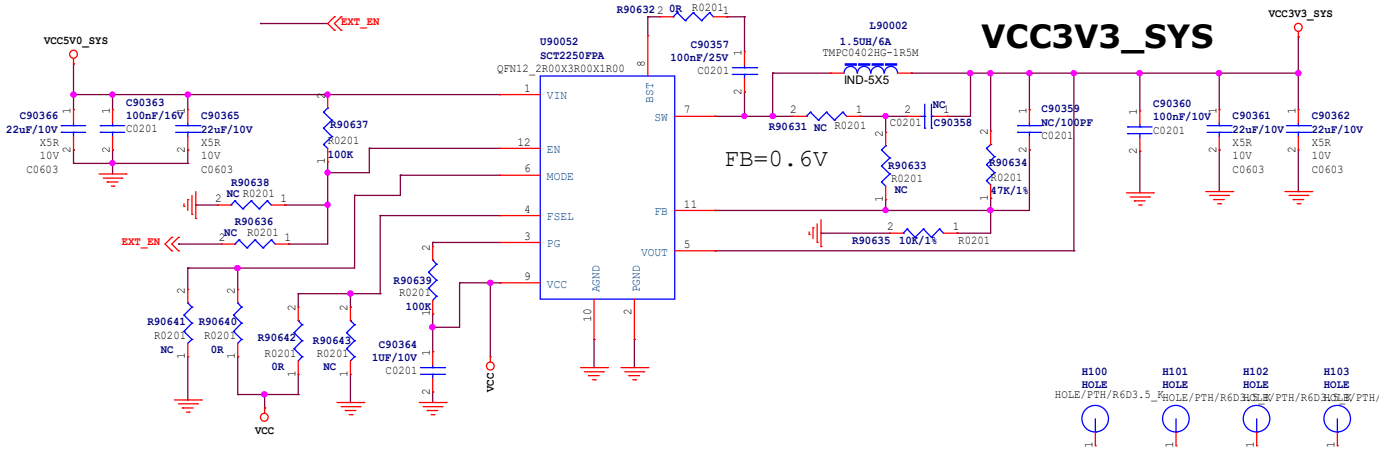
Note:

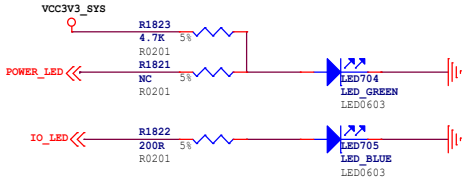
The power off hold time scheme is required,
It is recommended to use external RTC IC

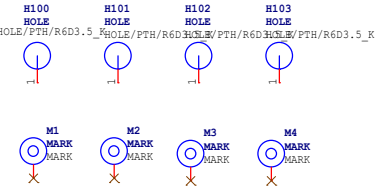
But, it will not support the timing poweron function



VCC3V3_SYS

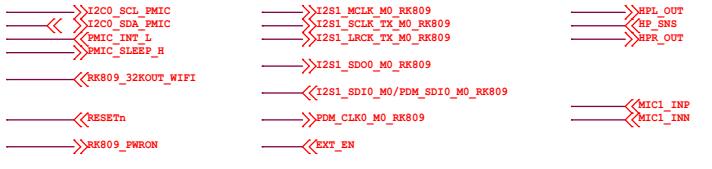


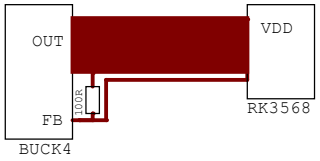




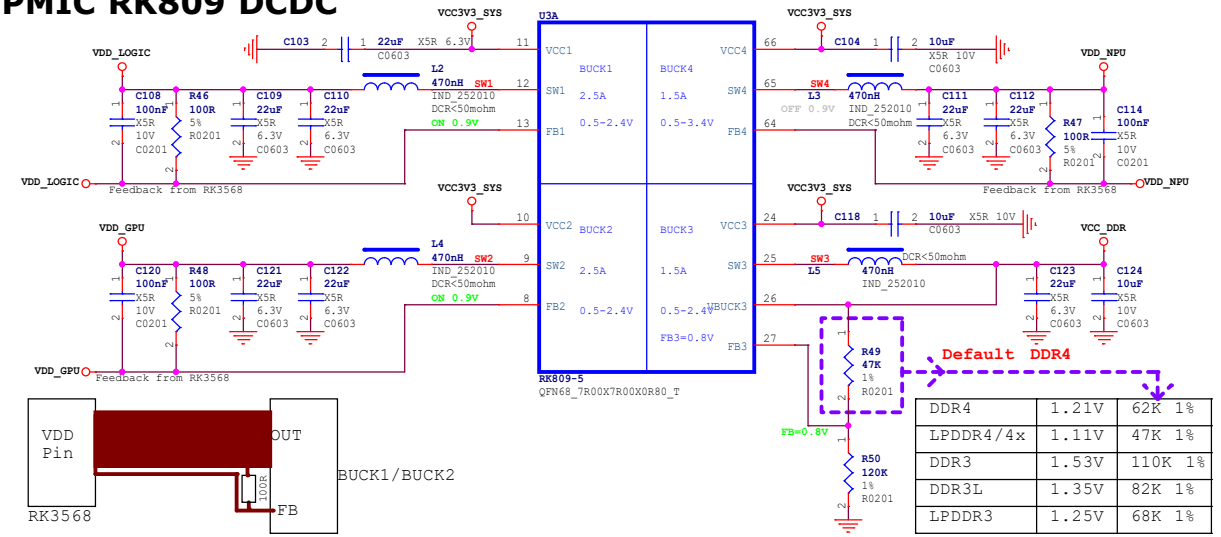
radxa

Size	Title:	Gong Le	REV
A3	Page Name:	Power_CPU_RTC	V1.3
Date:	Friday, September 10, 2021	Sheet 31 of 33	



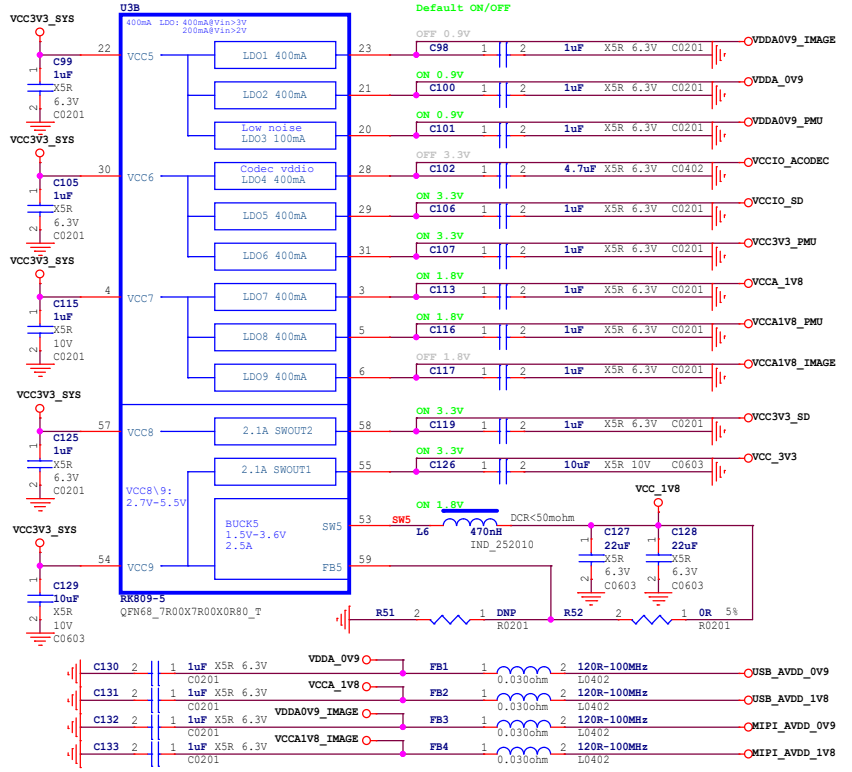


PMIC RK809 DCDC

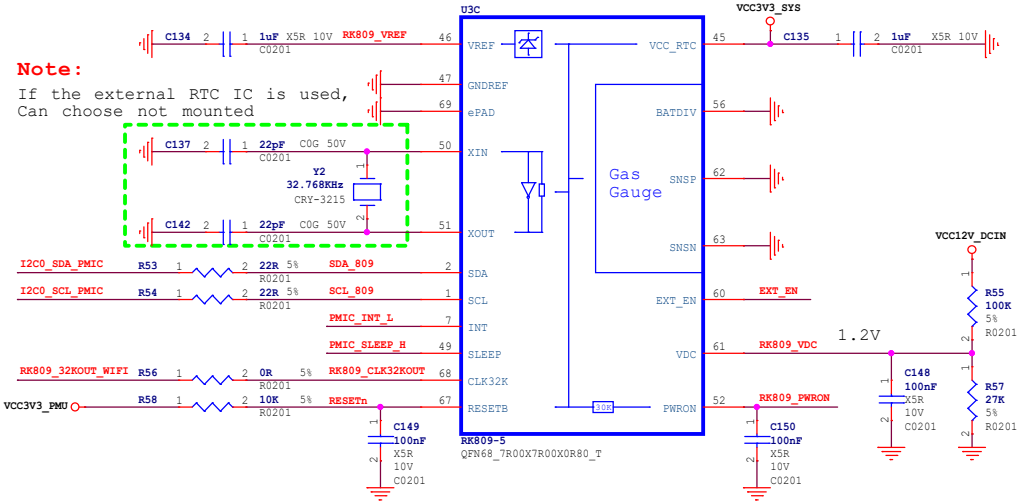


DDR4	1.21V	62K 1%
LPDDR4/4x	1.11V	47K 1%
DDR3	1.53V	110K 1%
DDR3L	1.35V	82K 1%
LPDDR3	1.25V	68K 1%

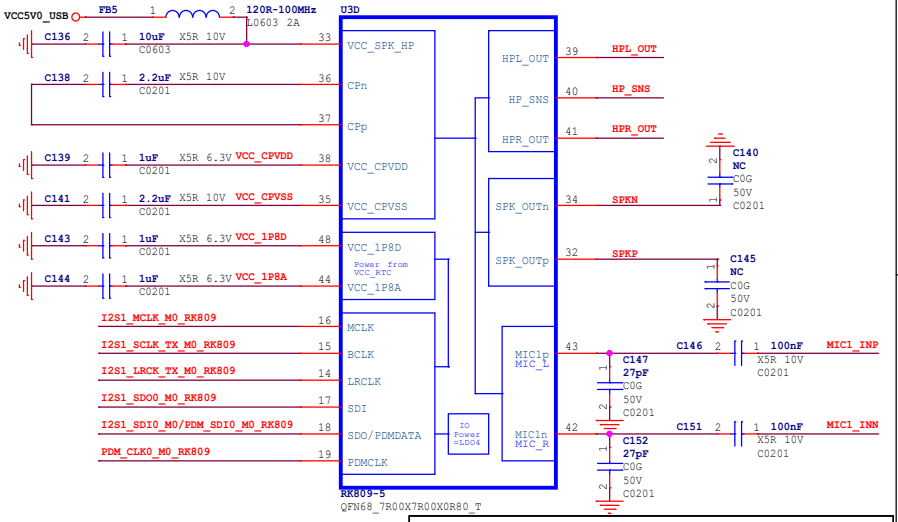
PMIC RK809 LDO



PMIC RK809 Management



PMIC RK809 CODEC



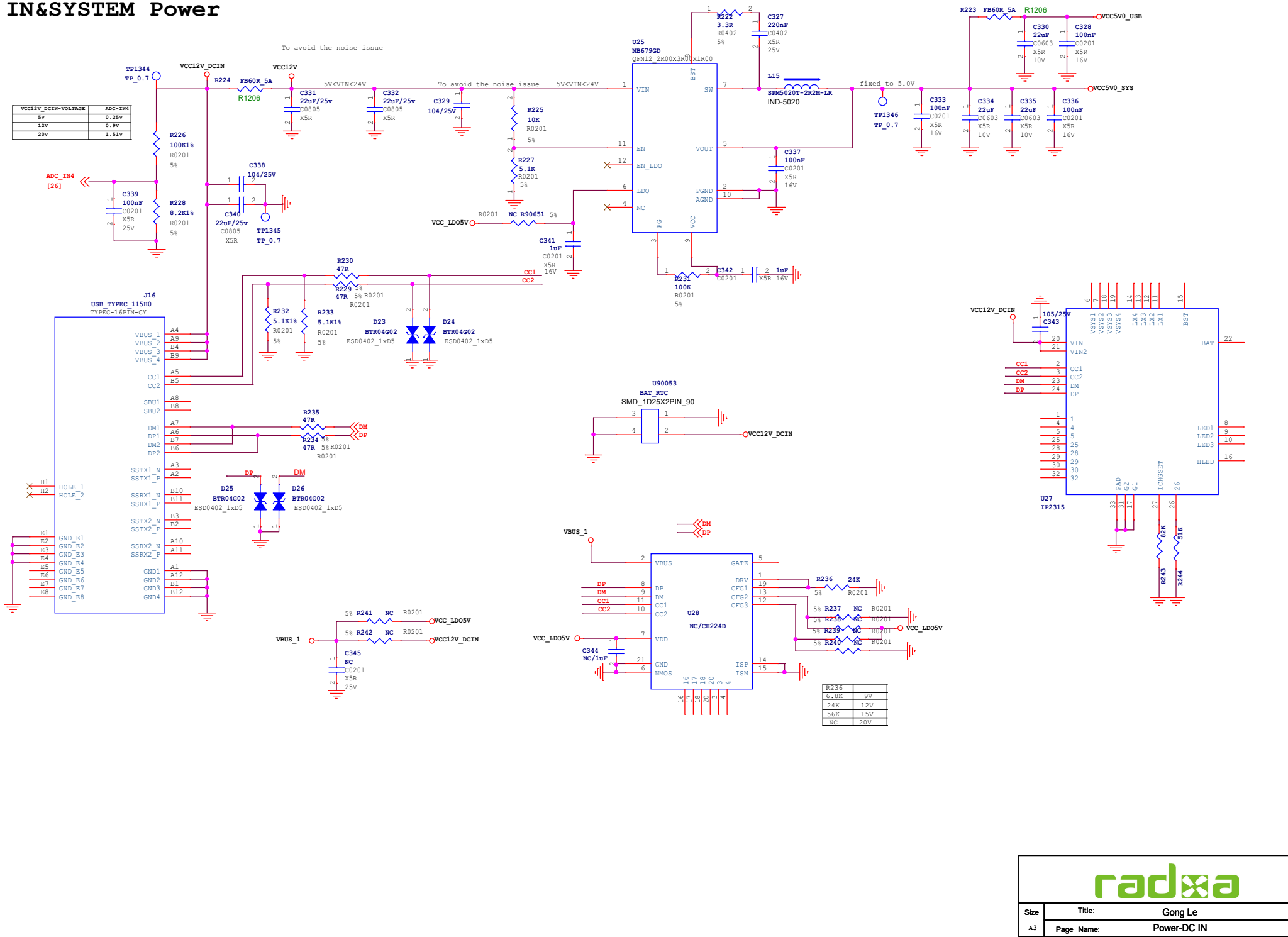
Note:

If RK809-5 codec is not used,
then Pin 14,15,16,17,19,40 Tie VSS
Pin 18,36,37,38,35,39,41,34,32,43,42
Leave floating

radxa

Size A3	Title: Gong Le	REV V1.3
	Page Name: Power_PMIC	
Date: Friday, September 10, 2021	Sheet 32 of 33	

DC IN&SYSTEM Power



VCC12V_DCIN-VOLTAGE	ADC-IN4
5V	0.25V
12V	0.9V
20V	1.51V

R236	
6.8K	9V
24K	12V
56K	15V
NC	20V

radxa

Size	Title:	REV
A3	Gong Le	V1.3
	Page Name: Power-DC IN	
Date: Friday, September 10, 2021	Sheet 33 of 33	